Document Number:MC56F82XXXPB
Rev 3.1, 11/2013

MC56F82XXX Product Brief

Supports 56F827xx and 56F823xx

Contents

1 Introduction

The 56F827xx microcontroller is a member of the 32-bit 56800EX core-based Digital Signal Controllers (DSCs). Each device in the family combines, on a single chip, the processing power of a 32-bit DSP and the functionality of a microcontroller with a flexible set of peripherals. Due to its cost-effectiveness, configuration flexibility, and compact program code, 56F827xx is well-suited for many consumer and industrial applications.

The 56800EX core is based on a dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications. Additionally, memory resource protection (MRP) is provided to protect supervisor programs and resources from user programs.

The on-chip flash memory and RAM can be mapped into both the program and data memory spaces. Two data operands can be accessed from the on-chip data RAM per instruction cycle.

1.1 Core Overview

The 56F827xx family is based on an 56800EX core, which updates the 56800E core. The 56800EX core has all 56800E core features and adds new enhancements, including:

- 32-bit x 32-bit MUL/MAC operations
- all registers in the Address Generation Unit (AGU) have shadowed registers that effectively reduce the context save/restore time during exception processing, reducing latency.
- bit-reverse address mode supporting Fast Fourier Transform
- new bit manipulation instruction that integrates a Test bitfield and a Set/Clear (BFSC) bitfield into a single instruction

With all existing 32-bit arithmetic operations, the 56800EX core is truly 32-bit compatible.

1.2 Memory Overview

Devices in the 56F827xx family include multiple blocks of on-chip memory:

- Up to 64 KB (32 KW) program flash memory
- Up to 8 KB (4 KW) RAM

Both bulk erasing and erasing in pages are supported.

1.3 Peripheral Overview

A full set of programmable peripherals—including PWM, ADC, QSCIs, QSPIs, I2C, an MSCAN, Inter-Module Crossbars, Quad Timers, a CRC block, DACs, Analog Comparators, and on-chip/off-chip clock sources—supports various applications. Each peripheral's clock can be independently gated to save power. Any pin in these peripherals can also be used as General Purpose Input/Outputs (GPIOs).

2 Application Examples

With numerous, highly integrated peripherals and powerful processing capabilities, 56F827xx is a low-cost family especially useful for switched-mode power supplies (SMPSs), advanced motor control (including dual motor control), smart appliances, uninterruptible power supplies (UPSs), photovoltaic systems, power distribution systems, wireless charging, and medical monitoring applications.

Table 1. Sample Applications

Application	Examples
Switched-mode power supplies (SMPSs)	• Multi-output digital SMPSs • Interleaving Power Factor Correction (PFC) • Multiple phase converters • LLC DC to DC converters
Advanced motor control	• Universal motors • DC motors • AC Induction Motors (ACIMs) • Brushless DC (BLDC) motors • Permanent Magnet Synchronous Motors (PMSMs) • Switched Reluctance (SR) motors • Stepper motors

Table continues on the next page...

Table 1. Sample Applications (continued)

Application	Examples
	• Linear motors • Actuators • Poly-phase motors • Dual motor control
Smart appliances	• Washing machines • Dryers • Dishwashers • Induction cookers
Photovoltaic systems	• Residential solar inverter • Grid-tied three phase solar inverter • Micro-inverter • Fuel cell generator
Power distribution systems	• Circuit breakers • Arc fault detectors • Power quality monitors
Wireless charging	
Uninterruptible power supplies (UPSs)	
Medical monitoring applications	
Lighting	

3 Features

The following list summarizes the superset of features across the entire 56F827xx family.

- 56800EX 32-bit DSC core
- Up to 50 MHz operation frequency in normal mode and 100 MHz in fast mode
- Up to 32 KW program flash memory
- Up to 4 KW dual port program/data RAM
- Memory resource protection (MRP) unit:
  - Partitions software into two modes—supervisor software and user software—with separate system address spaces and resources, for both program and data
  - Protects supervisor programs and resources from user programs
- Four-channel DMA
- One 8-channel eFlexPWM module with NanoEdge™ placement and enhanced capture
- 2 x 8-channel 12-bit cyclic ADC
- One windowed watchdog timer
- Cyclic Redundancy Check (CRC) generator
- On-chip 8 MHz/400 kHz relaxation oscillator, 200 kHz Relaxation Oscillator and 4 MHz to 16 MHz Crystal Oscillator (XOSC)
- Power Supervisor
- Inter-Module Crossbar with AND-OR-INVERT function
- Programmable Interrupt Controller (INTC)
- One Quad Timer
- Two Periodic Interval Timers
- Two 12-bit DAC modules
- Four High Speed Comparators with integrated 6-bit DAC references
- Two Queued SPI modules
- Two Queued SCI modules

- One I2C/SMBus module
- One MSCAN module
- 5 V tolerant I/O (except for RESETB pin which is a 3.3 V pin)

3.1 MC56F827xx/3xx Product Family

The following table highlights features that differ among members of the family. Features not listed are shared in common by all members of the family.

Table 2. MC56F827xx/3xx Family

Part Number	MC56F82															
	748 VLH	**746 VLF**	**743 VLC**	**743 VFM**	**738 VLH**	**736 VLF**	**733 VLC**	**733 VFM**	**728 VLH**	**726 VLF**	**723 VLC**	**723 VFM**	**348 MLH**	**323 VFM**	**316 VLF**	**313 VLC**
Core frequency (MHz)	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	50	50	50	50
Flash memory (KB)	64	64	64	64	48	48	48	48	32	32	32	32	64	32	16	16
RAM (KB)	8	8	8	8	8	8	8	8	6	6	6	6	8	6	4	4
12-bit Cyclic ADC channels	2x8	2x5	2x3	2x3	2x8	2x5	2x3	2x3	2x8	2x5	2x3	2x3	2x8	2x3	2x5	2x3
PWMA with input capture:																
High-resolution channels	1x8	1x6	1x6	1x6	1x8	1x6	1x6	1x6	1x8	1x6	1x6	1x6	1x8	0	0	0
Standard channels	0	0	0	0	0	0	0	0	0	0	0	0	0	1x6	1x6	1x6
12-bit DAC	2	2	2	2	2	2	2	2	2	2	2	2	2	0	2	0
DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
CMP	4	4	3	3	4	4	3	3	4	4	3	3	4	2	4	2
QSCI	2	2	1	1	2	2	1	1	2	2	1	1	2	1	2	1
QSPI	2	1	1	1	2	1	1	1	2	1	1	1	2	1	1	1
I2C/SMBus	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
MSCAN	1	1	0	0	1	1	0	0	1	1	0	0	1	0	0	0
GPIO	54	39	26	26	54	39	26	26	54	39	26	26	54	26	39	26
Package pin count	64 LQFP	48 LQFP	32 LQFP	32 QFN	64 LQFP	48 LQFP	32 LQFP	32 QFN	64 LQFP	48 LQFP	32 LQFP	32 QFN	64 LQFP	32 QFN	48 LQFP	32 LQFP

3.2 Block Diagram

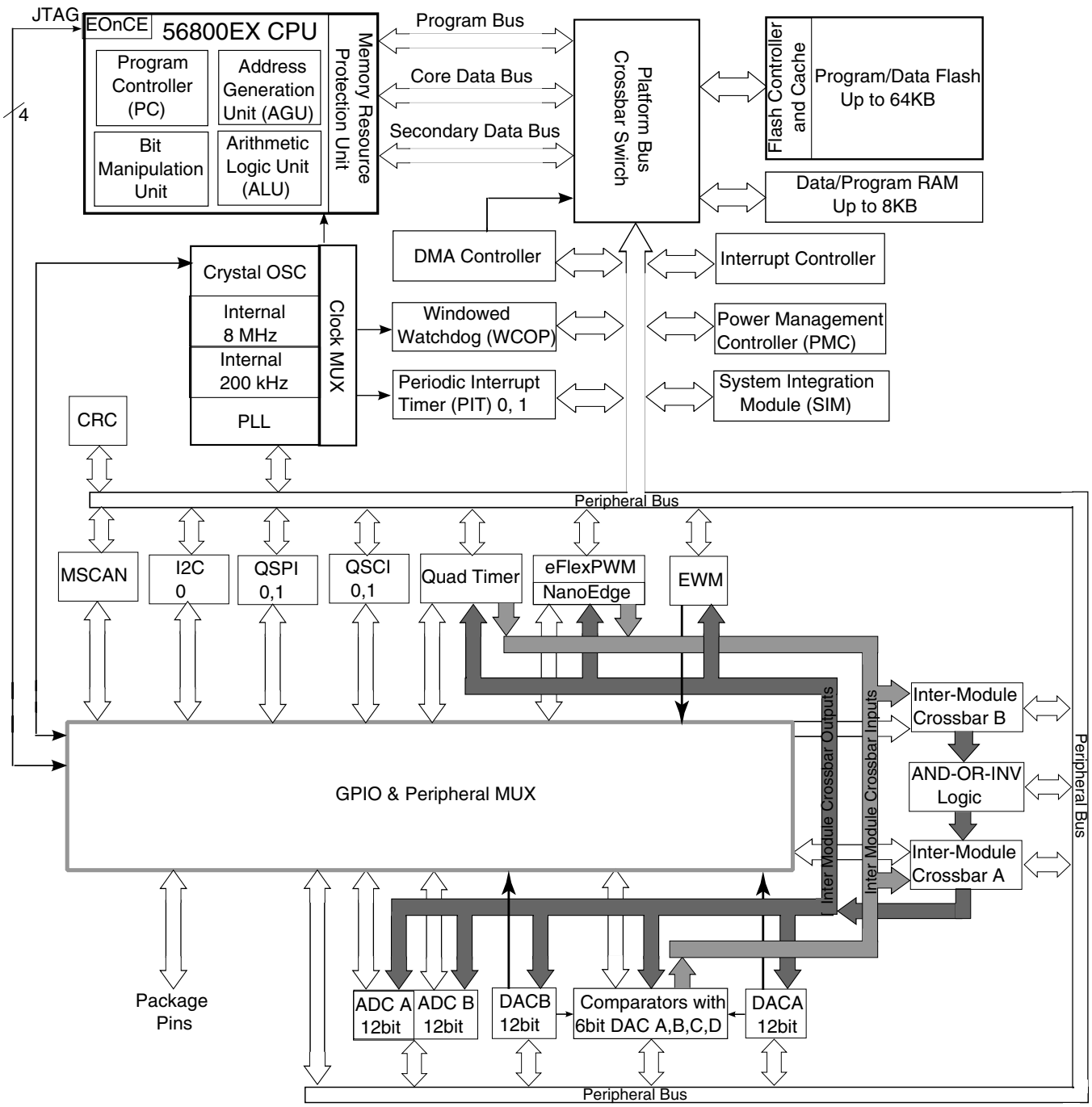

Figure 1. Block Diagram

3.3 56800EX 32-bit Digital Signal Controller (DSC) core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture:
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses
  - Supports concurrent instruction fetches in the same cycle, and dual data accesses in the same cycle
  - 20 addressing modes
- As many as 100 million instructions per second (MIPS) at 100 MHz core frequency
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses support 8-bit, 16-bit, and 32-bit data movement, plus addition, subtraction, and logical operations
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, which effectively supports DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers correspond to nine address registers (R0, R1, R2, R3, R4, R5, N, N3, M01)
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions enable compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack, with the stack's depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

3.4 Operation Parameters

- Up to 50 MHz operation in normal mode and 100 MHz operation in fast mode at -40 ºC to 105ºC ambient temperature
- Single 3.3 V power supply
- Supply range: V_{DD} - V_{SS} = 2.7 V to 3.6 V, V_{DDA} - V_{SSA} = 2.7 V to 3.6 V

3.5 Packages

- 32QFN
- 32LQFP
- 48LQFP
- 64LQFP

3.6 On-Chip Memory and Memory Protection

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming

- The dual-port RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses by the core.
  - Concurrent accesses provide increased performance.
  - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory
  - Up to 64 KB program/data flash memory
  - Up to 8 KB dual port data/program RAM

3.7 Peripherals

3.7.1 System Modules

3.7.1.1 Interrupt Controller

- Five interrupt priority levels
  - Three user-programmable priority levels for each interrupt source: level 0, level 1, level 2
  - Unmaskable level 3 interrupts include illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
  - Interrupt level 3 is highest priority and non-maskable. Its sources include:
    - Illegal instructions
    - Hardware stack overflow
    - SWI instruction
    - EOnce interrupts
    - Misaligned data accesses
  - Lowest-priority software interrupt: level LP
- Support for nested interrupts, so that a higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level is managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

3.7.1.2 Direct Memory Access (DMA) Controller

- Four independently programmable DMA controller channels
- Dual-address transfers via 32-bit master connection to the system bus
- Data transfers in 8-bit, 16-bit, or 32-bit blocks
- Continuous-mode or cycle-steal transfers from software or peripheral initiation
- One programmable input selected from 16 possible peripheral requests per channel
- Automatic hardware acknowledge/done indicator from each channel
- Independent source and destination address registers
- Optional modulo addressing and automatic updates of source and destination addresses
- Independent transfer sizes for source and destination
- Optional auto-alignment feature for source or destination accesses
- Optional automatic single or double channel linking
- Programming model accessed via 32-bit slave peripheral bus
- Channel arbitration on transfer boundaries using fixed priority scheme
- DMA peripherals:
  - Quad Timer
  - ADCs
  - QSPIs

- QSCIs
- I2Cs
- PWMs
- Crossbar
- 12-bit DAC

3.7.1.3 Inter-Module Crossbar and AND-OR-INVERT logic

- Provides generalized connections between and among on-chip peripherals: ADCs, 12-bit DAC, comparators, quad-timers, eFlexPWMs, EWM, and select I/O pins
- User-defined input/output pins for all modules connected to the crossbar
- DMA request and interrupt generation from the crossbar
- Write-once protection for all registers
- AND-OR-INVERT function provides a universal Boolean function generator that uses a four-term sum-of-products expression, with each product term containing true or complement values of the four selected inputs (A, B, C, D).

3.7.1.4 Cyclic Redundancy Check (CRC) Generator

- Hardware CRC generator circuit with 16-bit shift register
- High-speed hardware CRC calculation
- Programmable initial seed value
- CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial
- Error detection for all single, double, odd, and most multibit errors
- Option to transpose input data or output data (CRC result) bitwise, which is required for certain CRC standards

3.7.2 General Purpose I/O (GPIO)

- 5 V tolerance
- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins
- All pins (except JTAG and RESETB) default to be GPIO inputs
- 2 mA / 9 mA source/sink capability
- Controllable output slew rate

3.7.3 Timers and PWM modules

3.7.3.1 Enhanced Flex Pulse Width Modulator (eFlexPWM)

- PWM module contains four identical submodules, with up to three outputs per submodule
- 16 bits of resolution for center, edge-aligned, and asymmetrical PWMs
- High resolution NanoEdge placement
  - Fractional delay for enhanced resolution of the PWM period and edge placement
  - 390 ps PWM frequency and duty-cycle resolution when NanoEdge functionality is enabled.
- PWM outputs can be configured as complementary output pairs or independent outputs
- Dedicated time-base counter with period and frequency control per submodule
- Independent top and bottom deadtime insertion for each complementary pair
- Independent control of both edges of each PWM output
- Enhanced input capture and output compare functionality on each input:
  - Channels not used for PWM generation can be used for buffered output compare functions.
  - Channels not used for PWM generation can be used for input capture functions.
  - Enhanced dual edge capture functionality

- Synchronization of submodule to external hardware (or other PWM) is supported.
- Double-buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half-cycle reload capability
- Multiple output trigger events can be generated per PWM cycle via hardware.
- Support for double-switching PWM outputs
- Up to eight fault inputs can be assigned to control multiple PWM outputs
  - Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Individual software control of each PWM output
- All outputs can be programmed to change simultaneously via a FORCE_OUT event.
- PWMX pin can optionally output a third PWM signal from each submodule
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - Crossbar module outputs
  - External ADC input, taking into account values set in ADC high and low limit registers

3.7.3.2 Quad Timer

- Four 16-bit up/down counters, with a programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters
- Up to 100 MHz operation clock

3.7.3.3 Periodic Interrupt Timer (PIT) Modules

- 16-bit up-counter with programmable counter modulo
- Interrupt capability
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 200 kHz oscillator
  - System bus (IPBus up to 50 MHz)
  - 8 MHz / 400 kHz ROSC
- Can signal the device to exit powerdown mode
- Programmable master/slave selection between PIT instances

3.7.3.4 Windowed Computer Operating Properly (COP) Watchdog

- Programmable windowed timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 200 kHz oscillator
  - System bus (IPBus up to 50 MHz)
  - 8 MHz / 400 kHz ROSC
- Support for interrupt triggered when the counter reaches the timeout value

3.7.3.5 External Watchdog Monitor (EWM)

- Monitors external circuit as well as the software flow
- Programmable timeout period
- Interrupt capability prior to timeout

- Independent output (EWM_OUT_b) that places external circuit (but not CPU and peripheral) in a safe mode when EWM timeout occurs
- Selectable reference clock source in support of EN60730 and IEC61508
- Wait mode and Stop mode operation is not supported.
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 200 kHz oscillator
  - System bus (IPBus up to 50 MHz)
  - 8 MHz / 400 kHz ROSC

3.7.4 Clock Modules

3.7.4.1 On-chip oscillators

- Tunable 8 MHz relaxation oscillator with 400 kHz at standby mode (divide-by-two output)
- 200 kHz low frequency clock as secondary clock source for COP, EWM, PIT

3.7.4.2 Crystal oscillator

- Support for both high ESR crystal oscillator (ESR greater than 100 Ω) and ceramic resonator
- Operating frequency: 4–16 MHz

3.7.4.3 Phase-locked loop

- Wide programmable output frequency: 200 MHz to 400 MHz
- Input reference clock frequency: 8 MHz to 16 MHz
- Detection of loss of lock and loss of reference clock
- Ability to power down

3.7.5 Analog Modules

3.7.5.1 12-bit Analog-to-Digital Converter (Cyclic type)

- Two independent 12-bit analog-to-digital converters (ADCs):
  - 2 x 8-channel external inputs
  - Built-in x1, x2, x4 programmable gain pre-amplifier
  - Maximum ADC clock frequency up to 10 MHz, having period as low as 100-ns
  - Single conversion time of 10 ADC clock cycles
  - Additional conversion time of 8 ADC clock cycles
- Support of analog inputs for single-ended and differential, including unipolar differential, conversions
- Sequential, parallel, and independent scan mode
- First 8 samples have offset, limit and zero-crossing calculation supported
- ADC conversions can be synchronized by *any* module connected to the internal crossbar module, such as PWM, timer, GPIO, and comparator modules.
- Support for simultaneous triggering and software-triggering conversions
- Support for a multi-triggering mode with a programmable number of conversions on each trigger
- Each ADC has ability to scan and store up to 8 conversion results.
- Current injection protection

3.7.5.2 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode
- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms, including square, triangle, and sawtooth waveforms (for applications like slope compensation)
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally to an off-chip destination

3.7.5.3 Comparator

- Full rail-to-rail comparison range
- Support for high and low speed modes
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 6-bit programmable DAC as a voltage reference per comparator
  - 2.7 V to 3.3 V operation range
  - 64-tap resistor ladder
  - Selectable supply reference source
  - Powerdown mode to conserve power when not in use
  - Output routed to internal comparator input
  - Less than 20 µA power consumption
- Three programmable hysteresis levels
- Selectable interrupt on rising-edge, falling-edge, or toggle of a comparator output

3.7.6 Communication Interfaces

3.7.6.1 Queued Serial Peripheral Interface (QSPI) modules

- Maximum 12.5 Mbit/s baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers
- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

3.7.6.2 Queued Serial Communications Interface (QSCI) modules

- Operating clock can be up to two times the CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 16-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection
- Up to 6.25 Mbit/s baud rate at 100 MHz operation clock

3.7.6.3 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) modules

- Compatible with I2C bus standard
- Support for System Management Bus (SMBus) specification, version 2
- Multi-master operation
- General call recognition
- 10-bit address extension
- Start/Repeat and Stop indication flags
- Support for dual slave addresses or configuration of a range of slave addresses
- Programmable glitch input filter with option to clock up to 100 MHz

3.7.6.4 Modular/Scalable Controller Area Network (MSCAN) Module

- Clock source from PLL or oscillator.
- Implementation of the CAN protocol Version 2.0 A/B
- Standard and extended data frames
- 0-to-8 bytes data length
- Programmable bit rate up to 1 Mbit/s
- Support for remote frames
- Individual Rx Mask Registers per Message Buffer
- Internal timer for time-stamping of received and transmitted messages
- Listen-only mode capability
- Programmable loopback mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Low power modes, with programmable wakeup on bus activity

3.7.7 Power Management

3.7.7.1 On-Chip Voltage Regulator

- Input 2.7 V to 3.6 V (4.0 V absolute maximum rating)
- Provides 1.2 V ± 10% accuracy
- Separate large and small regulators
- Distributed type layout

3.7.7.2 Power supervisor

- Power-on reset (POR) to reset CPU, peripherals, and JTAG/EOnCE controllers (V_{DD} > 2.1 V)
- Brownout reset (V_{DD} < 1.9 V)
- Critical warn low-voltage interrupt (LVI2.0)
- Peripheral low-voltage interrupt (LVI2.7)

4 Developer Environment

The following table summarizes available development tools.

Tool	Description
TWR-56F82748	Cost-effective development board that is part of the Freescale Tower System, a modular development platform that enables rapid prototyping and re-use through reconfigurable hardware
TWR-MC-LV3PH	3-Phase Low Voltage Motor Control Module for TWR-56F84789 used to develop DC, BLDC, and PMSM motor control solutions using various algorithms provided by Freescale
TWR-MC-STEPPER	Low Voltage Motor Control Module for TWR-56F84789 used to develop stepper motor control solutions using various algorithms provided by Freescale
TWR-ELEV Elevator Module	Elevator modules are the basic building block of Freescale's Tower System. Designed to connect microcontroller and peripheral modules, Elevator modules provide the power regulation circuitry and structural integrity needed for all configurations of an assembled Tower System.
CodeWarrior Development Studio for Microcontrollers v10.2: CW-56800E-DSC Special Edition	This comprehensive integrated development environment (IDE), based in Eclipse,™ provides a highly visual and automated framework to accelerate the development of most complex embedded applications.
Processor Expert[1]	Rapid application design tool that combines easy-to-use component-based application creation with an expert knowledge system
FreeMASTER[1]	FreeMASTER software represents a sophisticated tool with intuitive navigation that can be used in any application development. This tool allows control of an application remotely from a user-friendly graphical environment running on a PC. It also provides the ability to view realtime application variables in both textual and graphical form.
MQX RTOS[1]	Accelerate design success with this complimentary RTOS, which simplifies fine tuning of custom applications and is scalable to fit requirements.
DSP and Motor Control Libraries[1] : FSLESL56F800ELIBSW	Freescale Embedded Software Library v1.0 for MC56FX84xx

1. Complimentary

5 Revision History

The following table summarizes changes to this document since the release of the previous version.

Table 4. Revision History

Rev. No.	Date	Substantial Changes
3	10/2013	First public release
3.1	11/2013	In Table 2, corrected MC56F82323VFM's package pin count to 32QFN

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number MC56F82XXXPB
Revision 3.1, 11/2013