SiT9386 PRELIMINARY

AEC-Q100, Ultra-low Jitter Differential Oscillator

Features

- AEC-Q100 with extended temperature range (-40°C to 105°C)
- Any frequency between 1 MHz and 220 MHz, accurate to 6 decimal places. For frequency between 220 and 725 MHz, see SiT9387
- LVPECL, LVDS and HCSL output signaling types
- 0.23 ps RMS (typ) phase jitter (random, 12 kHz to 20 MHz)
- Frequency stability as low as ±25 ppm – contact SiTime
- Industry-standard packages: 3.2 x 2.5, 7.0 x 5.0 mm Contact SiTime for 5.0 x 3.2 mm package

Applications

- Automotive, and other high reliability electronics
- Infotainment systems, collision detection devices and in-vehicle 10/40/100 Gbps Ethernet

Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output termination show in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

Table 1. Electrical Characteristics — Common to LVPECL, LVDS and HCSL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	1	–	220	MHz	Accurate to 6 decimal places
Frequency Stability						
Frequency Stability		-25	–	+25	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage and load variations. Contact SiTime for ± 25 ppm.
		-50	–	+50	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage and load variations.
First Year Aging	F_1y	–	±1	–	ppm	At 25°C
Temperature Range						
Operating Temperature Range	T_use	-40	–	+85	°C	Industrial
		-40	–	+105	°C	Extended Industrial
Supply Voltage						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.7	3.0	3.3	V	
		2.52	2.8	3.08	V	
		2.25	2.5	2.75	V	
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE
Input Pull-up Impedance	Z_in	–	100	-	kΩ	Pin 1, OE logic high or logic low
Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Startup and OE Timing						
Start-up Time	T_start	–	–	3.0	ms	Measured from the time Vdd reaches its rated minimum value.
OE Enable/Disable Time	T_oe	–	–	3.8	µs	f = 156.25 MHz.

Table 2. Electrical Characteristics – LVPECL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	89	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	58	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Maximum Output Current	I_driver	–	–	32	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	VOH	Vdd-1.1	–	Vdd-0.7	V	See Figure 2
Output Low Voltage	VOL	Vdd-1.9	–	Vdd-1.5	V	See Figure 2
Output Differential Voltage Swing	V_Swing	1.2	1.6	2.0	V	See Figure 3
Rise/Fall Time	Tr, Tf	–	225		ps	20% to 80%, see Figure 2
Jitter						
RMS Phase Jitter (random)	T_phj	–	0.220		ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, 7.0 x 5.0 mm package.
		–	0.225		ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, 3.2 x 2.5 mm package.
		–	0.1	–	ps	f = 156.25, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.
RMS Period Jitter[1]	T_jitt	–	1.0		ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V

Notes:

1. Measured according to JESD65B

Table 3. Electrical Characteristics – LVDS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	79	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	58	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Output Characteristics						
Differential Output Voltage	VOD	250	–	455	mV	See Figure 4
VOD Magnitude Change	ΔVOD	–	–	50	mV	See Figure 4
Offset Voltage	VOS	1.125	–	1.375	V	See Figure 4
VOS Magnitude Change	ΔVOS	–	–	50	mV	See Figure 4
Rise/Fall Time	Tr, Tf	–	400		ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 4
Jitter						
RMS Phase Jitter (random)	T_phj	–	0.215		ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, 7.0 x 5.0 mm package.
			0.235		ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, 3.2 x 2.5 mm package.
		–	0.1	–	ps	f = 156.25, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.
RMS Period Jitter[2]	T_jitt	–	1.0		ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V

Notes:

2. Measured according to JESD65B

Table 4. Electrical Characteristics – HCSL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	89	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	58	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Maximum Output Current	I_driver	–	–	35	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	VOH	0.60	–	0.90	V	See Figure 2
Output Low Voltage	VOL	-0.05	–	0.08	V	See Figure 2
Output Differential Voltage Swing	V_Swing	1.2	1.4	1.80	V	See Figure 3
Rise/Fall Time	Tr, Tf	–	360		ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 2
Jitter						
RMS Phase Jitter (random)	T_phj	–	0.220		ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, 7.0 x 5.0 mm package.
		–	0.230		ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, 3.2 x 2.5 mm package.
		–	0.1	–	ps	f = 156.25, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.
RMS Period Jitter[3]	T_jitt	–	1.0		ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V

Notes:

3. Measured according to JESD65B

Table 5. Pin Description

Pin	Map	Functionality	
1	OE/NC	Output Enable (OE)	H[4]: specified frequency output L: output is high impedance
		Non Connect (NC)	H or L or Open: No effect on output frequency or other device functions
2	NC	NA	No Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power	Vdd Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	Vdd	Power	Power supply voltage[5]

Top View

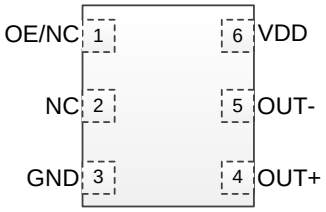


Figure 1. Pin Assignments

Notes:

4. In OE mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven.
5. A capacitor of value 0.1 µF or higher between Vdd and GND is required. An additional 10 µF capacitor between Vdd and GND is required for the best phase jitter performance

Table 6. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Vdd	-0.5	4.0	V
VIH		Vdd + 0.3V	V
VIL	-0.3		V
Storage Temperature	-65	150	ºC
Maximum Junction Temperature		130	ºC
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	ºC

Table 7. Thermal Considerations[6]

Package	θ_{JA}, 4 Layer Board (°C/W)	θ_{JC}, Bottom (°C/W)
3225, 6-pin	80	30
7050, 6-pin	52	19

Notes:

6. Refer to JESD51 for θ_{JA} and θ_{JC} definitions, and reference layout used to determine the θ_{JA} and θ_{JC} values in the above table.

Table 8. Maximum Operating Junction Temperature[7]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	95°C
85°C	110°C
105°C	-

Notes:

7. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 9. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	*g*
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	*g*
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

Waveform Diagrams

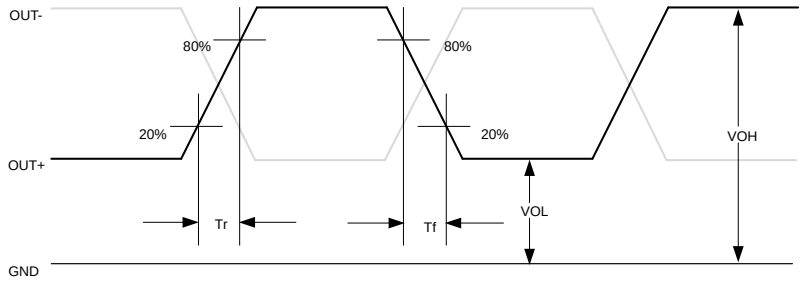


Figure 2. LVPECL/HCSL Voltage Levels per Differential Pin (OUT+/OUT-)

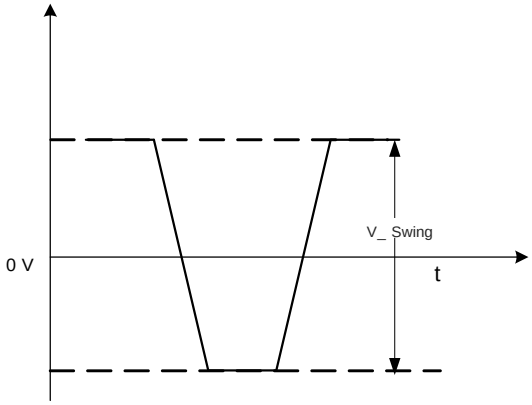


Figure 3. LVPECL/HCSL Voltage Levels across Differential Pair

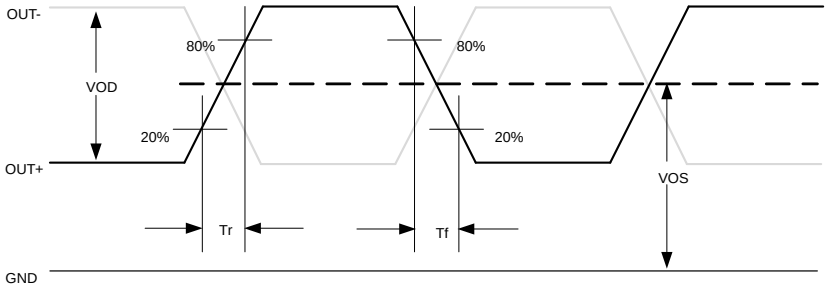


Figure 4. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

Termination Diagrams

LVPECL:

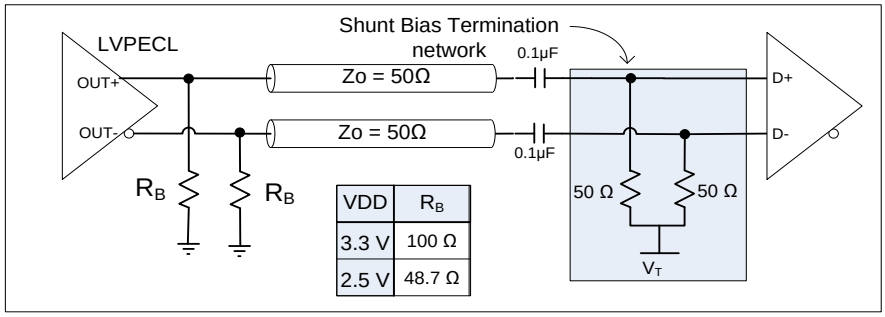


Figure 5. LVPECL with AC-coupled termination

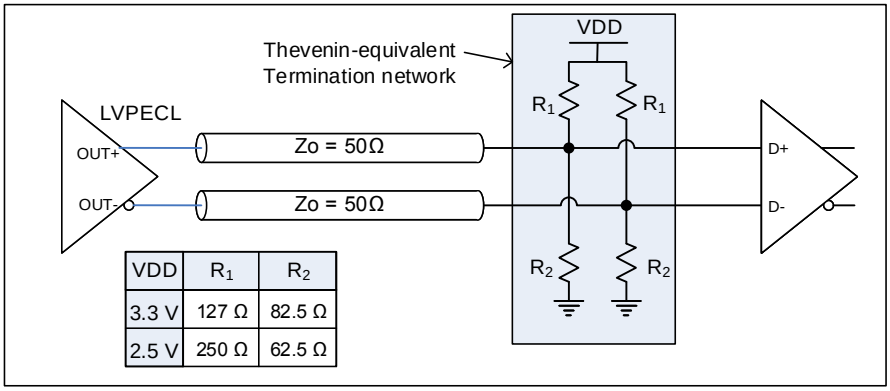


Figure 6. LVPECL DC-coupled load termination with Thevenin equivalent network

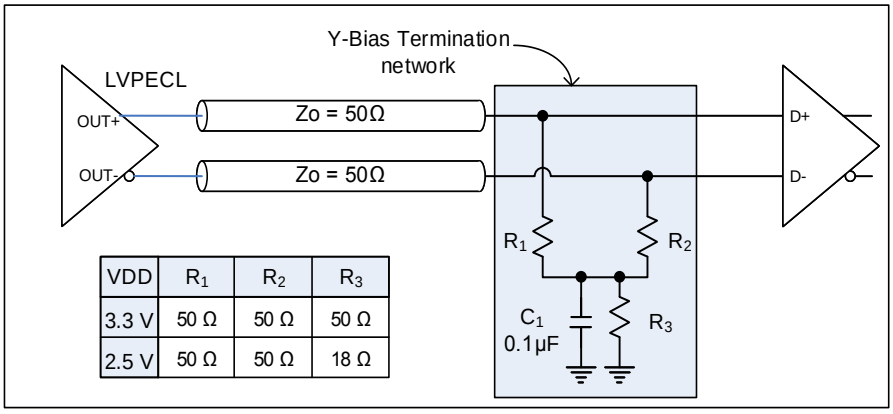


Figure 7. LVPECL with Y-Bias termination

Termination Diagrams (Continued)

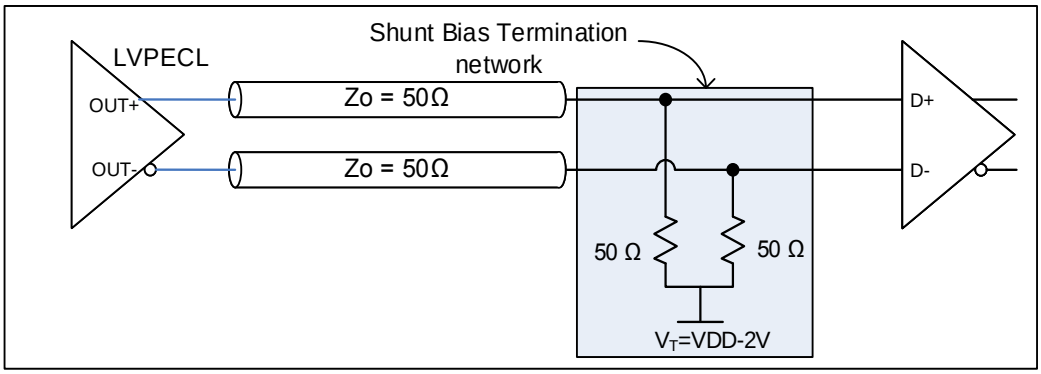


Figure 8. LVPECL with DC-coupled parallel shunt load termination

Termination Diagrams (Continued)

LVDS:

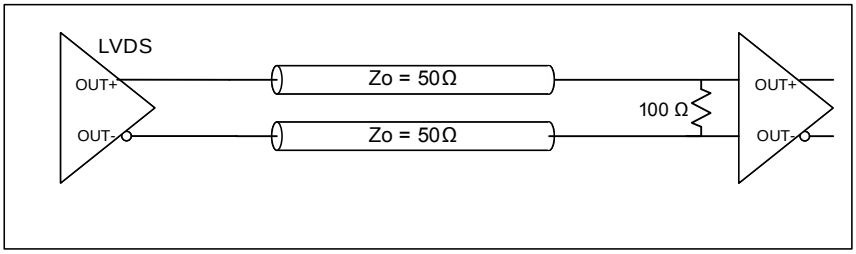


Figure 9. LVDS single DC termination at the load

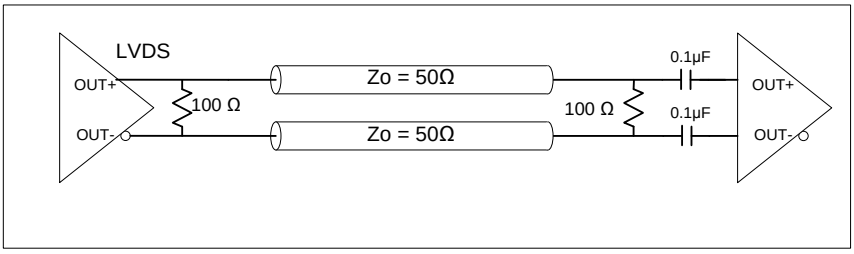


Figure 10. LVDS double AC termination with capacitor close to the load

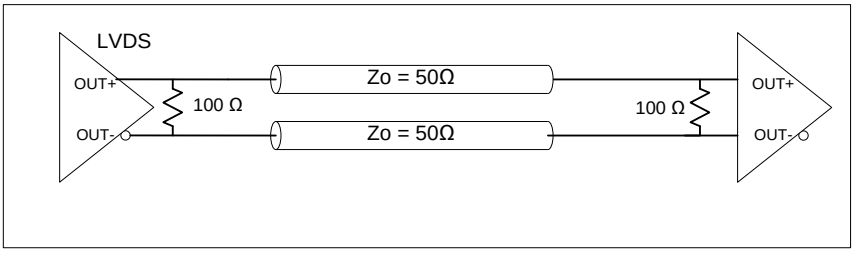


Figure 11. LVDS double DC termination

Termination Diagrams (Continued)

HCSL:

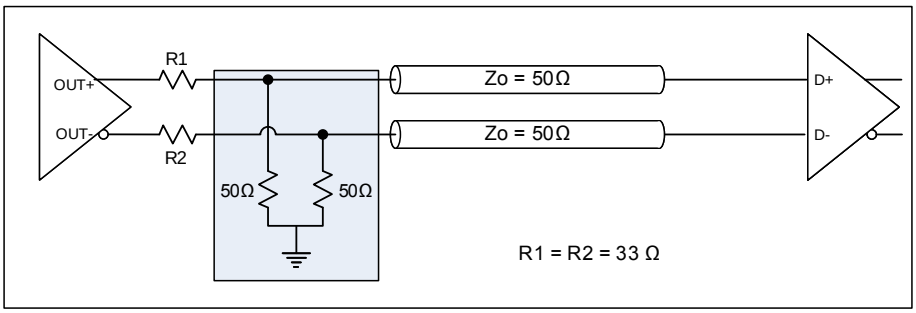
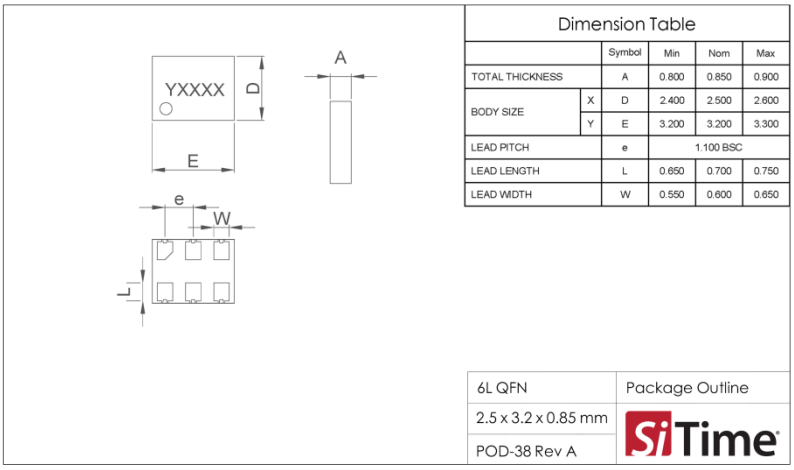


Figure 12. HCSL interface termination

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[8]	Recommended Land Pattern (Unit: mm)[9]
3.2 x 2.5 x 0.85 mm	**3.2 x 2.5 x 0.85 mm**
7.0 x 5.0 x 0.85 mm[10]	**7.0 x 5.0 x 0.85 mm**[10]

3.2 x 2.5 x 0.85 mm

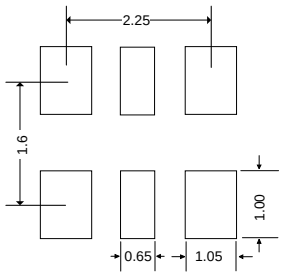


Dimension Table

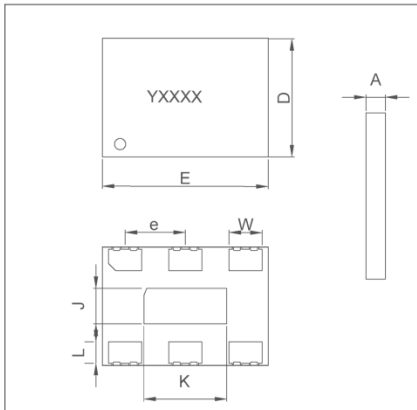
		Symbol	Min	Nom	Max
TOTAL THICKNESS		A	0.800	0.850	0.900
BODY SIZE	X	D	2.400	2.500	2.600
	Y	E	3.200	3.200	3.300
LEAD PITCH		e	1.100 BSC		
LEAD LENGTH		L	0.650	0.700	0.750
LEAD WIDTH		W	0.550	0.600	0.650

6L QFN	Package Outline
2.5 x 3.2 x 0.85 mm	
POD-38 Rev A	

3.2 x 2.5 x 0.85 mm



7.0 x 5.0 x 0.85 mm[10]

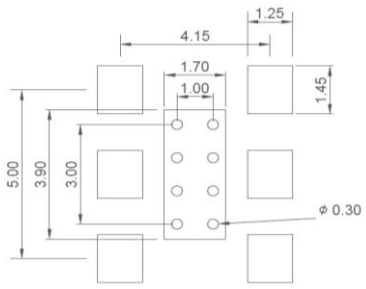


Dimension Table

		Symbol	Min	Nom	Max
TOTAL THICKNESS		A	0.800	0.850	0.900
BODY SIZE	X	D	4.900	5.000	5.100
	Y	E	6.900	7.000	7.100
EP SIZE	X	J	1.400	1.500	1.600
	Y	K	3.400	3.500	3.600
LEAD PITCH		e	2.540 BSC		
LEAD LENGTH		L	0.850	0.900	0.950
LEAD WIDTH		W	1.350	1.400	1.450

6L QFN	Package Outline
5.0 x 7.0 x 0.85 mm	
POD-37 Rev A	

7.0 x 5.0 x 0.85 mm[10]

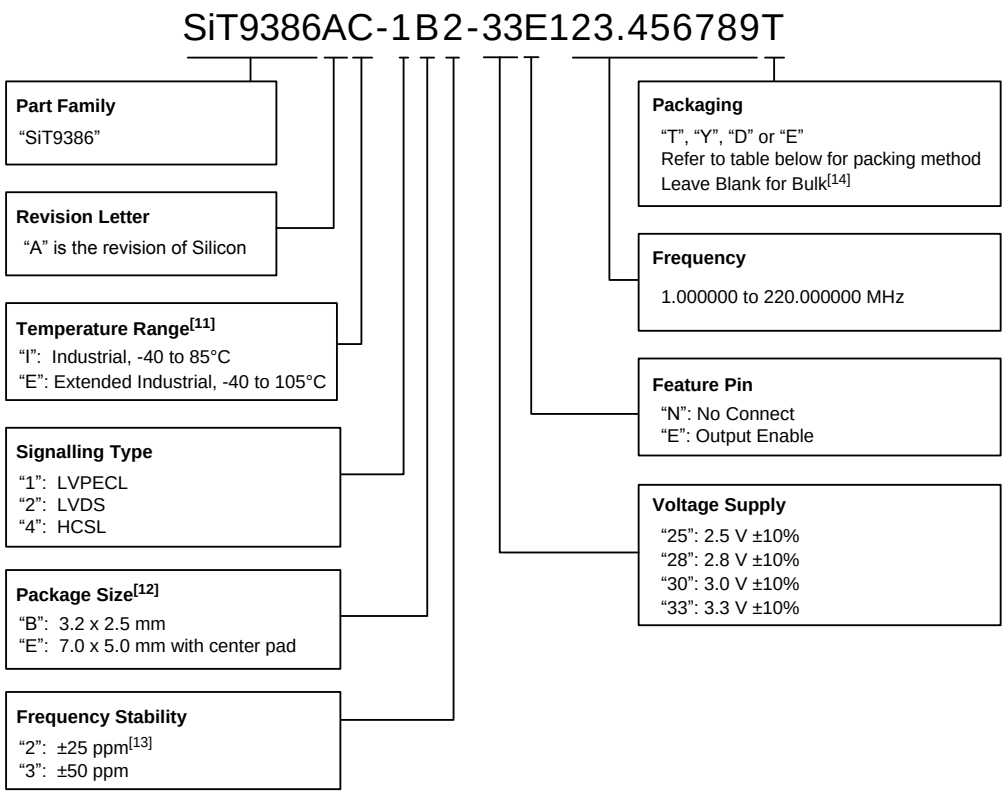


Note:
Circles in center pad are thermal vias, recommended to improve thermal performance

Notes:

8. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
9. A capacitor of value 0.1 µF or higher between Vdd and GND is required. An additional 10 µF capacitor between Vdd and GND is required for the best phase jitter performance
10. The center pad has no electrical function. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

Ordering Information



Notes:

11. Contact SiTime for higher temperature range options.
12. Contact SiTime for 5.0 x 3.2 mm package.
13. Contact SiTime for ±25 ppm option.
14. Bulk is available for sampling only.

Table 10. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
7.0 x 5.0	—	—	—	—	T	Y
3.2 x 2.5	D	E	T	Y	—	—

Table 11. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
Part number Generator	Tool used to create the part number based on desired features.	—
Time Machine II	MEMS oscillator programmer	http://www.sitime.com/support/time-machine-oscillator-programmer
Field Programmable Oscillators	Devices that can be programmable in the field by Time Machine II	http://www.sitime.com/products/field-programmable-oscillators
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	http://www.sitime.com/component/docman/doc_download/243-manufacturing-notes-for-sitime-oscillators
Qualification Reports	RoHS report, reliability reports, composition reports	http://www.sitime.com/support/quality-and-reliability
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	http://www.sitime.com/support/performance-measurement-report
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes

Table 12. Revision History

Revision	Release Date	Change Summary
0.1	03/11/2017	Initial draft
0.87	11/06/2017	Updated package drawings Corrected tape/reel ordering information Updated Electrical Characteristics based on characterization Included max numbers for IPJ Added additional information table Corrected formatting issues Increased temperature range from 95ºC to 105ºC Removed ±10 ppm options for automotive and industrial temperature ranges Changed ±20 ppm to “contact SiTime” Updated termination diagrams Lower mechanical shock from 20,000 to 10,000 *g*
0.90	11/24/2017	Ordering information updates and page layout changes

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