

### FEATURES

- Output frequency range: 2400 MHz to 2725 MHz
- Divide-by-2 output
- 3.0 V to 3.6 V power supply
- 1.8 V logic compatibility
- Integer-N synthesizer
- Programmable dual-modulus prescaler 16/17, 32/33
- Programmable output power level
- 3-wire serial interface
- Analog and digital lock detect
- Hardware and software power-down mode

### APPLICATIONS

- Wireless handsets (DECT, GSM, PCS, DCS, WCDMA)
- Test equipment
- Wireless LANs
- CATV equipment

### GENERAL DESCRIPTION

The ADF4360-0 is a fully integrated integer-N synthesizer and voltage-controlled oscillator (VCO). The ADF4360-0 is designed for a center frequency of 2600 MHz. In addition, a divide-by-2 option is available, whereby the user gets an RF output of between 1200 MHz and 1360 MHz.

Control of all the on-chip registers is through a simple 3-wire interface. The device operates with a power supply ranging from 3.0 V to 3.6 V and can be powered down when not in use.

### FUNCTIONAL BLOCK DIAGRAM

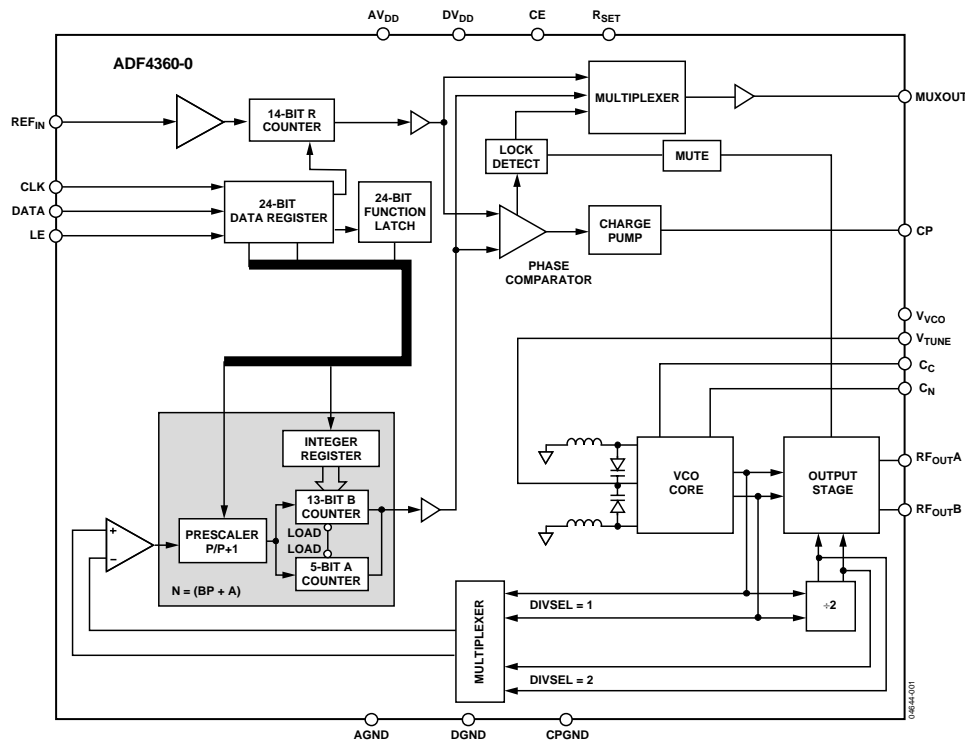


Figure 1.

Rev. D

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# ADF4360-0\* PRODUCT PAGE QUICK LINKS

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- ADF4360-0 Evaluation Board

## DOCUMENTATION

### Application Notes

- AN-30: Ask the Applications Engineer - PLL Synthesizers
- AN-873: Lock Detect on the ADF4xxx Family of PLL Synthesizers

### Data Sheet

- ADF4360-0: Integrated Synthesizer and VCO Data Sheet

### User Guides

- UG-095: Evaluation Board User Guide for ADF4360-0
- UG-476: PLL Software Installation Guide

## SOFTWARE AND SYSTEMS REQUIREMENTS

- ADF4360 - Microcontroller No-OS Driver

## TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF

## REFERENCE MATERIALS

### Product Selection Guide

- RF Source Booklet

### Technical Articles

- Phase Locked Loops for High-Frequency Receivers and Transmitters – Part 1
- Phase Locked Loops for High-Frequency Receivers and Transmitters – Part 3
- Phase-Locked Loops for High-Frequency Receivers and Transmitters - Part 2

## DESIGN RESOURCES

- ADF4360-0 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

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## SAMPLE AND BUY

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## TECHNICAL SUPPORT

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**TABLE OF CONTENTS**

Specifications.....	3	VCO .....	10
Timing Characteristics.....	5	Output Stage.....	11
Absolute Maximum Ratings.....	6	Latch Structure .....	12
Transistor Count.....	6	Power-Up.....	16
ESD Caution.....	6	Control Latch .....	18
Pin Configuration and Function Descriptions.....	7	N Counter Latch.....	19
Typical Performance Characteristics .....	8	R Counter Latch .....	19
Circuit Description.....	9	Applications Information .....	20
Reference Input Section.....	9	Fixed Frequency LO.....	20
Prescaler (P/P + 1).....	9	Interfacing .....	20
A and B Counters .....	9	PCB Design Guidelines for Chip Scale Package.....	21
R Counter .....	9	Output Matching.....	21
PFD and Charge Pump.....	9	Outline Dimensions .....	22
MUXOUT and Lock Detect.....	10	Ordering Guide .....	22
Input Shift Register.....	10		

**REVISION HISTORY**

**3/16—Rev. C to Rev. D**

Changed ADF4360 Family to ADF4360-0 and ADSP-21xx to ADSP-2181 .....	Throughout
Changes to Figure 3.....	7
Updated Outline Dimensions .....	22
Changes to Ordering Guide .....	22

**11/12—Rev. B to Rev. C**

Changes to Table 1.....	4
Changes to Table 3.....	6
Change to Output Matching Section .....	22
Updated Outline Dimensions .....	23

**2/12—Rev. A to Rev. B**

Changes to Figure 3 and Table 4.....	7
Updated Outline Dimensions .....	22
Changes to Ordering Guide .....	22

**12/04—Rev. 0 to Rev. A**

Updated Format.....	Universal
Changes to Timing Characteristics.....	5
Changes to Power-Up Section .....	16
Added Table 10 .....	16
Added Figure 16 .....	16
Changes to Ordering Guide .....	22
Updated Outline Dimensions .....	22

**7/04—Revision 0: Initial Version**

## SPECIFICATIONS<sup>1</sup>

$AV_{DD} = DV_{DD} = V_{VCO} = 3.3 \text{ V} \pm 10\%$ ;  $AGND = DGND = 0 \text{ V}$ ;  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 1.

Parameter	B Version	Unit	Test Conditions/Comments
<b>REF<sub>IN</sub> CHARACTERISTICS</b>			
REF <sub>IN</sub> Input Frequency	10/250	MHz min/max	For $f < 10 \text{ MHz}$ , use dc-coupled CMOS-compatible square wave, slew rate $> 21 \text{ V}/\mu\text{s}$ .
REF <sub>IN</sub> Input Sensitivity	$0.7/AV_{DD}$ 0 to $AV_{DD}$	V p-p min/max V max	AC-coupled. CMOS-compatible.
REF <sub>IN</sub> Input Capacitance	5.0	pF max	
REF <sub>IN</sub> Input Current	$\pm 100$	$\mu\text{A}$ max	
<b>PHASE DETECTOR</b>			
Phase Detector Frequency <sup>2</sup>	8	MHz max	
<b>CHARGE PUMP</b>			
I <sub>CP</sub> Sink/Source <sup>3</sup>			With $R_{SET} = 4.7 \text{ k}\Omega$ .
High Value	2.5	mA typ	
Low Value	0.312	mA typ	
R <sub>SET</sub> Range	2.7/10	k $\Omega$	
I <sub>CP</sub> Three-State Leakage Current	0.2	nA typ	
Sink and Source Current Matching	2	% typ	$1.25 \text{ V} \leq V_{CP} \leq 2.5 \text{ V}$ .
I <sub>CP</sub> vs. V <sub>CP</sub>	1.5	% typ	$1.25 \text{ V} \leq V_{CP} \leq 2.5 \text{ V}$ .
I <sub>CP</sub> vs. Temperature	2	% typ	$V_{CP} = 2.0 \text{ V}$ .
<b>LOGIC INPUTS</b>			
V <sub>INH</sub> , Input High Voltage	1.5	V min	
V <sub>INL</sub> , Input Low Voltage	0.6	V max	
I <sub>INH</sub> /I <sub>INL</sub> , Input Current	$\pm 1$	$\mu\text{A}$ max	
C <sub>IN</sub> , Input Capacitance	3.0	pF max	
<b>LOGIC OUTPUTS</b>			
V <sub>OH</sub> , Output High Voltage	$DV_{DD} - 0.4$	V min	CMOS output chosen.
I <sub>OH</sub> , Output High Current	500	$\mu\text{A}$ max	
V <sub>OL</sub> , Output Low Voltage	0.4	V max	I <sub>OL</sub> = 500 $\mu\text{A}$ .
<b>POWER SUPPLIES</b>			
AV <sub>DD</sub>	3.0/3.6	V min/V max	
DV <sub>DD</sub>	AV <sub>DD</sub>		
V <sub>VCO</sub>	AV <sub>DD</sub>		
A <sub>IDD</sub> <sup>4</sup>	10	mA typ	
D <sub>IDD</sub> <sup>4</sup>	2.5	mA typ	
I <sub>VCO</sub> <sup>4,5</sup>	19.0	mA typ	I <sub>CORE</sub> = 10 mA.
I <sub>RFOUT</sub> <sup>4</sup>	3.5 to 11.0	mA typ	RF output stage is programmable.
Low Power Sleep Mode <sup>4</sup>	7	$\mu\text{A}$ typ	
<b>RF OUTPUT CHARACTERISTICS<sup>5</sup></b>			
VCO Output Frequency	2400/2725	MHz min/max	I <sub>CORE</sub> = 15 mA.
VCO Sensitivity	56	MHz/V typ	
Lock Time <sup>6</sup>	250	$\mu\text{s}$ typ	To within 10 Hz of final frequency.
Frequency Pushing (Open-Loop)	1	MHz/V typ	
Frequency Pulling (Open-Loop)	15	kHz typ	Into 2.00 VSWR load.
Harmonic Content (Second)	-30	dBc typ	
Harmonic Content (Third)	-39	dBc typ	
Output Power <sup>5,7</sup>	-13/-6.5	dBm typ	Programmable in 3 dB steps. See Table 7.
Output Power Variation	$\pm 3$	dB typ	For tuned loads, see the Output Matching section.
VCO Tuning Range	1.25/2.50	V min/max	
VCO Tuning Port Leakage Current	0.2	nA typ	

Parameter	B Version	Unit	Test Conditions/Comments
<b>NOISE CHARACTERISTICS<sup>5</sup></b>			
VCO Phase-Noise Performance <sup>8</sup>	-111	dBc/Hz typ	At 100 kHz offset from carrier.
	-133	dBc/Hz typ	At 1 MHz offset from carrier.
	-140	dBc/Hz typ	At 3 MHz offset from carrier.
	-145	dBc/Hz typ	At 10 MHz offset from carrier.
Synthesizer Phase-Noise Floor <sup>9</sup>	-172	dBc/Hz typ	At 25 kHz PFD frequency.
	-163	dBc/Hz typ	At 200 kHz PFD frequency.
	-147	dBc/Hz typ	At 8 MHz PFD frequency.
Phase Noise Figure of Merit <sup>9</sup>	-216	dBc/Hz typ	
In-Band Phase Noise <sup>10, 11</sup>	-80	dBc/Hz typ	At 1 kHz offset from carrier.
RMS Integrated Phase Error <sup>12</sup>	1.4	Degrees typ	100 Hz to 100 kHz.
Spurious Signals due to PFD Frequency <sup>11, 13</sup>	-75	dBc typ	
Level of Unlocked Signal with MTLT Enabled	-45	dBm typ	

<sup>1</sup> Operating temperature range is: -40°C to +85°C.

<sup>2</sup> Guaranteed by design. Sample tested to ensure compliance.

<sup>3</sup> I<sub>CP</sub> is internally modified to maintain constant loop gain over the frequency range.

<sup>4</sup> T<sub>A</sub> = 25°C; AV<sub>DD</sub> = DV<sub>DD</sub> = V<sub>VCO</sub> = 3.3 V; P = 32.

<sup>5</sup> These characteristics are guaranteed for VCO core power = 10 mA.

<sup>6</sup> Jumping from 2.4 GHz to 2.725 GHz. PFD frequency = 200 kHz; loop bandwidth = 10 kHz.

<sup>7</sup> Using 50 Ω resistors to V<sub>VCO</sub> into a 50 Ω load. For tuned loads, see the Output Matching section.

<sup>8</sup> The noise of the VCO is measured in open-loop conditions.

<sup>9</sup> The synthesizer phase-noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value). The phase noise figure of merit subtracts 10 log (PFD frequency).

<sup>10</sup> The phase noise is measured with the [EV-ADF4360-0EB1Z](#) Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REF<sub>IN</sub> for the synthesizer; offset frequency = 1 kHz.

<sup>11</sup> f<sub>REFIN</sub> = 10 MHz; f<sub>PFD</sub> = 200 kHz; N = 13000; Loop B/W = 10 kHz.

<sup>12</sup> f<sub>REFIN</sub> = 10 MHz; f<sub>PFD</sub> = 1 MHz; N=2600; Loop B/W = 25 kHz.

<sup>13</sup> The spurious signals are measured with the [EV-ADF4360-0EB1Z](#) Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REF<sub>IN</sub> for the synthesizer; f<sub>REFOUT</sub> = 10 MHz at 0 dBm.

# TIMING CHARACTERISTICS<sup>1</sup>

$V_{DD} = DV_{DD} = V_{VCO} = 3.3\text{ V} \pm 10\%$ ;  $AGND = DGND = 0\text{ V}$ ; 1.8 V and 3 V logic levels used;  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 2.

Parameter	Limit at $T_{MIN}$ to $T_{MAX}$ (B Version)	Unit	Test Conditions/Comments
$t_1$	20	ns min	LE Setup Time
$t_2$	10	ns min	DATA to CLOCK Setup Time
$t_3$	10	ns min	DATA to CLOCK Hold Time
$t_4$	25	ns min	CLOCK High Duration
$t_5$	25	ns min	CLOCK Low Duration
$t_6$	10	ns min	CLOCK to LE Setup Time
$t_7$	20	ns min	LE Pulse Width

<sup>1</sup> See the Power-Up section for the recommended power-up procedure for this device.

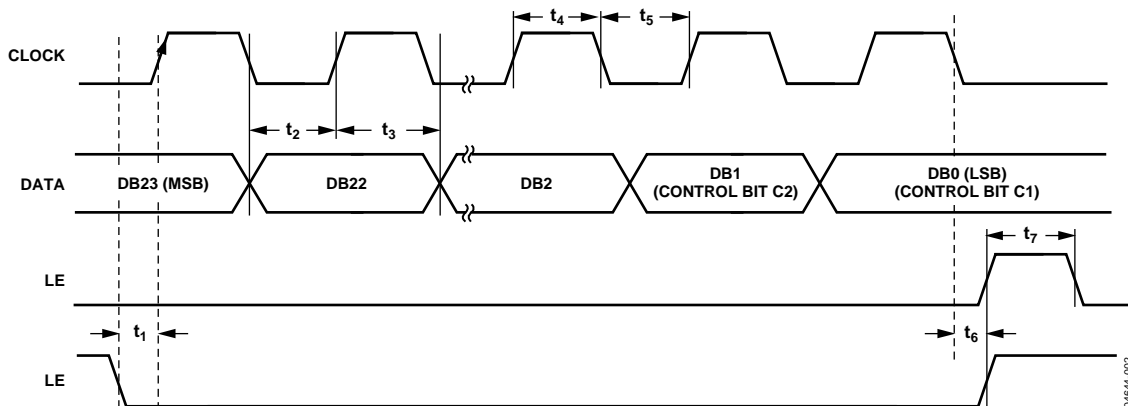


Figure 2. Timing Diagram

046844-002

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Rating
$AV_{DD}$ to GND <sup>1</sup>	-0.3 V to +3.9 V
$AV_{DD}$ to $DV_{DD}$	-0.3 V to +0.3 V
$V_{VCO}$ to GND	-0.3 V to +3.9 V
$V_{VCO}$ to $AV_{DD}$	-0.3 V to +0.3 V
Digital I/O Voltage to GND	-0.3 V to $V_{DD} + 0.3$ V
Analog I/O Voltage to GND	-0.3 V to $V_{DD} + 0.3$ V
$REF_{IN}$ to GND	-0.3 V to $V_{DD} + 0.3$ V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	150°C
CSP $\theta_{JA}$ Thermal Impedance	
Paddle Soldered	50°C/W
Paddle Not Soldered	88°C/W
Lead Temperature, Soldering Reflow	260°C

<sup>1</sup> GND = AGND = DGND = 0 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

This device is a high performance RF integrated circuit with an ESD rating of <1 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

### TRANSISTOR COUNT

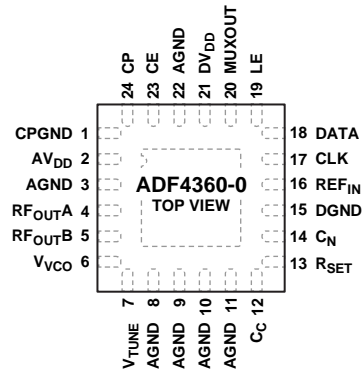
12543 (CMOS) and 700 (Bipolar).

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. THE EXPOSED PAD MUST BE CONNECTED TO AGND.

04644-003

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
2	AV <sub>DD</sub>	Analog Power Supply. This ranges from 3.0 V to 3.6 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV <sub>DD</sub> must have the same value as DV <sub>DD</sub> .
3, 8 to 11, 22	AGND	Analog Ground. This is the ground return path of the prescaler and VCO.
4	RF <sub>OUTA</sub>	VCO Output. The output level is programmable from –6.5 dBm to –13 dBm. See the Output Matching section for a description of the various output stages.
5	RF <sub>OUTB</sub>	VCO Complementary Output. The output level is programmable from –6.5 dBm to –13 dBm. See the Output Matching section for a description of the various output stages.
6	V <sub>VCO</sub>	Power Supply for the VCO. This ranges from 3.0 V to 3.6 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. V <sub>VCO</sub> must have the same value as AV <sub>DD</sub> .
7	V <sub>TUNE</sub>	Control Input to the VCO. This voltage determines the output frequency and is derived from filtering the CP output voltage.
12	C <sub>C</sub>	Internal Compensation Node. This pin must be decoupled to ground with a 10 nF capacitor.
13	R <sub>SET</sub>	Connecting a resistor between this pin and CP <sub>GND</sub> sets the maximum charge pump output current for the synthesizer. The nominal voltage potential at the R <sub>SET</sub> pin is 0.6 V. The relationship between I <sub>CP</sub> and R <sub>SET</sub> is $I_{CPmax} = \frac{11.75}{R_{SET}}$ where R <sub>SET</sub> = 4.7 kΩ, I <sub>CPmax</sub> = 2.5 mA.
14	C <sub>N</sub>	Internal Compensation Node. This pin must be decoupled to V <sub>VCO</sub> with a 10 μF capacitor.
15	DGND	Digital Ground.
16	REF <sub>IN</sub>	Reference Input. This is a CMOS input with a nominal threshold of V <sub>DD</sub> /2 and a dc equivalent input resistance of 100 kΩ. See Figure 10. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
17	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
18	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
19	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, and the relevant latch is selected using the control bits.
20	MUXOUT	This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
21	DV <sub>DD</sub>	Digital Power Supply. This ranges from 3.0 V to 3.6 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV <sub>DD</sub> must have the same value as AV <sub>DD</sub> .
23	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump into three-state mode. Taking the pin high powers up the device depending on the status of the power-down bits.
24	CP	Charge Pump Output. When enabled, this provides ± I <sub>CP</sub> to the external loop filter, which in turn, drives the internal VCO.
0	EP	Exposed Pad. The exposed pad must be connected to AGND.



TYPICAL PERFORMANCE CHARACTERISTICS

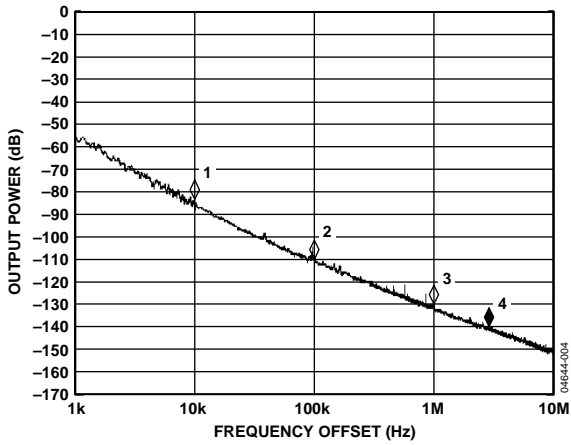


Figure 4. Open-Loop VCO Phase Noise

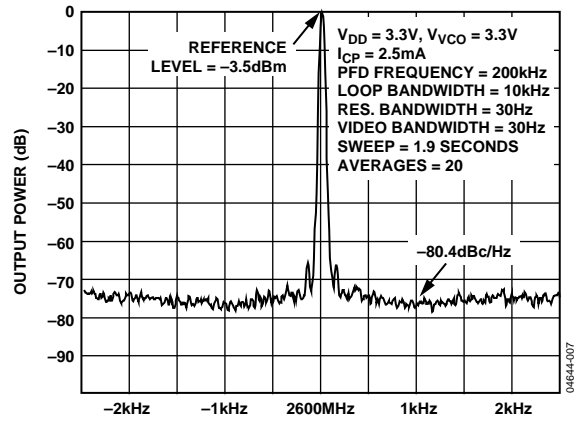


Figure 7. Close-In Phase Noise at 2600 MHz (200 kHz Channel Spacing)

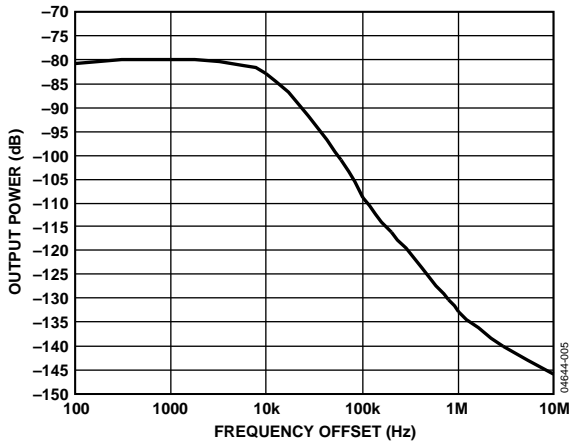


Figure 5. VCO Phase Noise, 2600 MHz, 200 kHz PFD, 10 kHz Loop Bandwidth

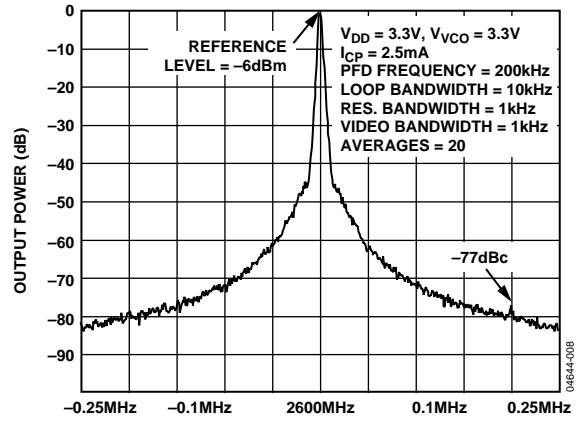


Figure 8. Reference Spurs at 2600 MHz (200 kHz Channel Spacing, 10 kHz Loop Bandwidth)

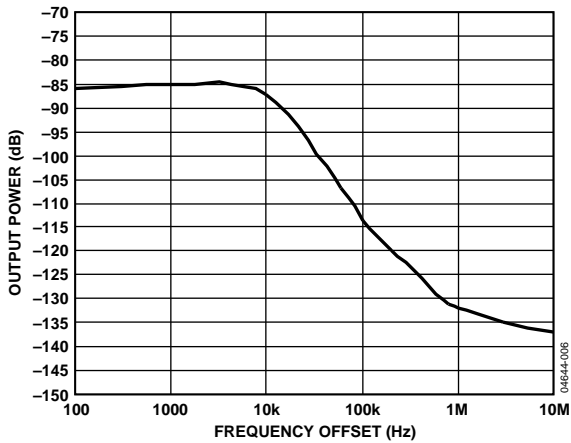


Figure 6. VCO Phase Noise, 1300 MHz, Divide-by-2 Enabled, 200 kHz PFD, 10 kHz Loop Bandwidth

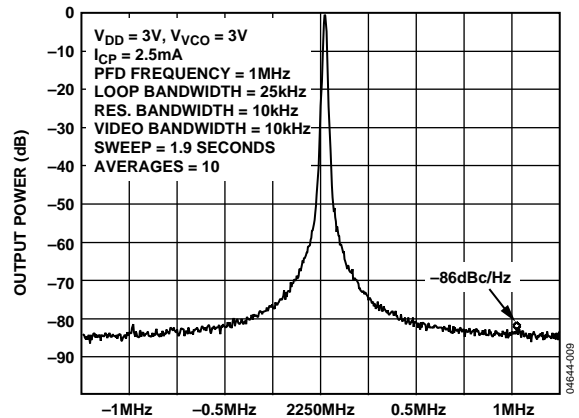


Figure 9. Reference Spurs at 2600 MHz (1 MHz Channel Spacing, 25 kHz Loop Bandwidth)

# CIRCUIT DESCRIPTION

## REFERENCE INPUT SECTION

The reference input stage is shown in Figure 10. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed, and SW1 and SW2 are opened. This ensures that there is no loading of the REF<sub>IN</sub> pin on power-down.

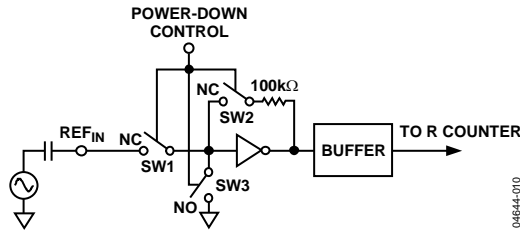


Figure 10. Reference Input Stage

## PRESCALER (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the A and B counters, enables the large division ratio, N, to be realized ( $N = BP + A$ ). The dual-modulus prescaler, operating at CML levels, takes the clock from the VCO and divides it down to a manageable frequency for the CMOS A and B counters. The prescaler is programmable. It can be set in software to 8/9, 16/17, or 32/33 and is based on a synchronous 4/5 core. There is a minimum divide ratio possible for fully contiguous output frequencies; this minimum is determined by P, the prescaler value, and is given by  $(P^2 - P)$ .

## A AND B COUNTERS

The A and B CMOS counters combine with the dual-modulus prescaler to allow a wide range division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 300 MHz or less. Thus, with a VCO frequency of 2.5 GHz, a prescaler value of 16/17 is valid, but a value of 8/9 is not valid.

## Pulse Swallow Function

The A and B counters, in conjunction with the dual-modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The VCO frequency equation is

$$f_{VCO} = ((P \times B) + A) \times f_{REFIN} / R$$

where:

$f_{VCO}$  is the output frequency of the VCO.

P is the preset modulus of the dual-modulus prescaler (8/9, 16/17, and so on).

B is the preset divide ratio of the binary 13-bit counter (3 to 8191).

A is the preset divide ratio of the binary 5-bit swallow counter (0 to 31).

$f_{REFIN}$  is the external reference frequency oscillator.

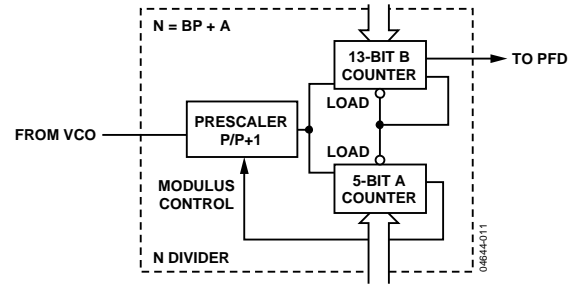


Figure 11. A and B Counters

## R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

## PFD AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter ( $N = BP + A$ ) and produces an output proportional to the phase and frequency difference between them. Figure 12 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antbacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the R counter latch, ABP2 and ABP1, control the width of the pulse (see Table 9).

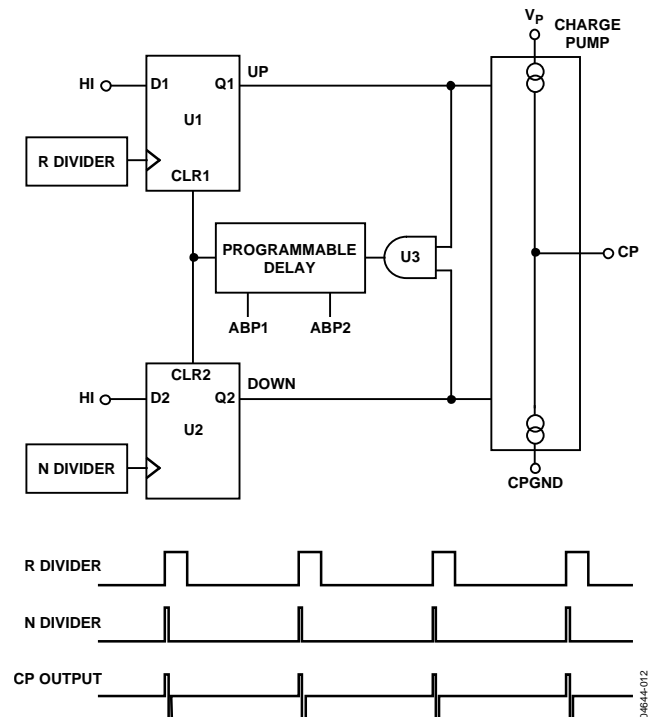


Figure 12. PFD Simplified Schematic and Timing (In Lock)

**MUXOUT AND LOCK DETECT**

The output multiplexer on the [ADF4360-0](#) allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. The full truth table is shown in Table 7. Figure 13 shows the MUXOUT section in block diagram form.

**Lock Detect**

MUXOUT can be programmed for two types of lock detect: digital and analog. Digital lock detect is active high. When LDP in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector cycles is less than 15 ns.

With LDP set to 1, five consecutive cycles of less than 15 ns phase error are required to set the lock detect. It stays set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle.

The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When a lock has been detected, this output is high with narrow low-going pulses.

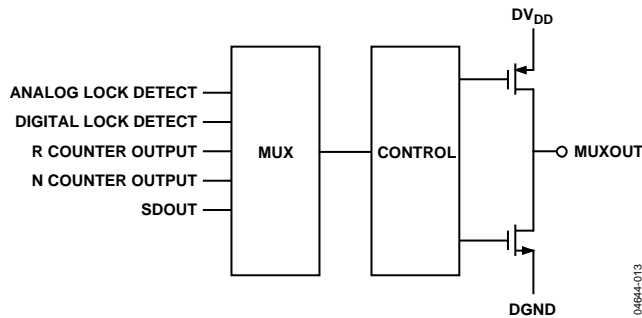


Figure 13. MUXOUT Circuit

**INPUT SHIFT REGISTER**

The digital section of the [ADF4360-0](#) includes a 24-bit input shift register, a 14-bit R counter, and an 18-bit N counter, comprised of a 5-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in Figure 2.

The truth table for these bits is shown in Table 5. Table 6 shows a summary of how the latches are programmed. Note that the test mode latch is used for factory testing and should not be programmed by the user.

Table 5. C2 and C1 Truth Table

Control Bits		Data Latch
C2	C1	
0	0	Control Latch
0	1	R Counter
1	0	N Counter (A and B)
1	1	Test Mode Latch

**VCO**

The VCO core in the [ADF4360-0](#) uses eight overlapping bands, as shown in Figure 14, to allow a wide frequency range to be covered without a large VCO sensitivity ( $K_v$ ) and resultant poor phase noise and spurious performance.

The correct band is chosen automatically by the band select logic at power-up or whenever the N counter latch is updated. It is important that the correct write sequence be followed at power-up. This sequence is

1. R counter latch
2. Control latch
3. N counter latch

During band select, which takes five PFD cycles, the VCO  $V_{TUNE}$  is disconnected from the output of the loop filter and connected to an internal reference voltage.

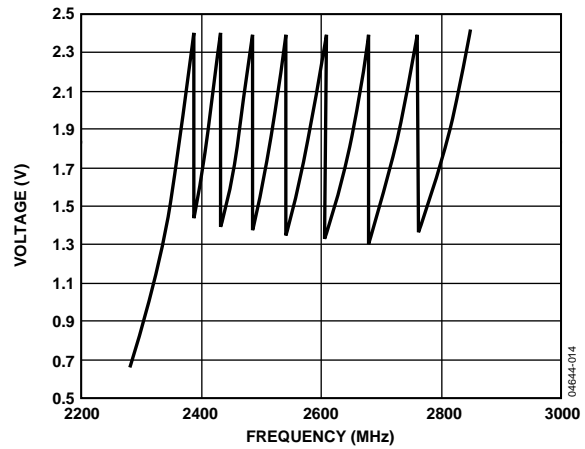


Figure 14. Frequency vs.  $V_{TUNE}$ , ADF4360-0

The R counter output is used as the clock for the band select logic and should not exceed 1 MHz. A programmable divider is provided at the R counter input to allow division by 1, 2, 4, or 8 and is controlled by Bits BSC1 and BSC2 in the R counter latch. Where the required PFD frequency exceeds 1 MHz, the divide ratio should be set to allow enough time for correct band selection.

After band select, normal PLL action resumes. The nominal value of  $K_v$  is 56 MHz/V or 28 MHz/V, if divide-by-2 operation has been selected (by programming DIV2 [DB22] high in the N counter latch). The [ADF4360-0](#) contains linearization circuitry to minimize any variation of the product of  $I_{CP}$  and  $K_v$ .

The operating current in the VCO core is programmable in four steps: 5 mA, 10 mA, 15 mA, and 20 mA. This is controlled by Bits PC1 and PC2 in the control latch.

## OUTPUT STAGE

The RF<sub>OUTA</sub> and RF<sub>OUTB</sub> pins of the ADF4360-0 are connected to the collectors of an NPN differential pair driven by buffered outputs of the VCO, as shown in Figure 15. To allow the user to optimize the power dissipation vs. the output power requirements, the tail current of the differential pair is programmable via Bits PL1 and PL2 in the control latch. Four current levels may be set: +3.5 mA, +5 mA, +7.5 mA, and +11 mA. These levels give output power levels of -13 dBm, -11 dBm, -8.5 dBm, and -6.5 dBm, respectively, using a 50 Ω resistor to V<sub>DD</sub> and ac coupling into a 50 Ω load. Alternatively, both outputs can be combined in a 1 + 1:1 transformer or a 180° microstrip coupler (see the Output Matching section).

If the outputs are used individually, the optimum output stage consists of a shunt inductor to V<sub>DD</sub>.

Another feature of the ADF4360-0 is that the supply current to the RF output stage is shut down until the device achieves lock as measured by the digital lock detect circuitry. This is enabled by the mute-till-lock detect (MTLD) bit in the control latch.

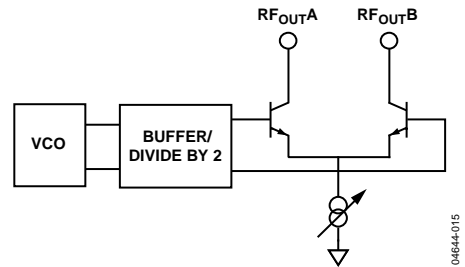


Figure 15. Output Stage ADF4360-0

0464-015

LATCH STRUCTURE

Table 6 shows the three on-chip latches for the ADF4360-0. The two LSBs determine which latch is programmed.

Table 6. Latch Structure

CONTROL LATCH

PRESCALER VALUE		POWER-DOWN 2	POWER-DOWN 1	CURRENT SETTING 2			CURRENT SETTING 1			OUTPUT POWER LEVEL		MUTE-TILL-LD	CP GAIN	CP THREE-STATE	PHASE DETECTOR POLARITY	MUXOUT CONTROL			COUNTER RESET	CORE POWER LEVEL		CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	PD1	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	PL2	PL1	MTLD	CPG	CP	PDP	M3	M2	M1	CR	PC2	PC1	C2 (0)	C1 (0)

N COUNTER LATCH

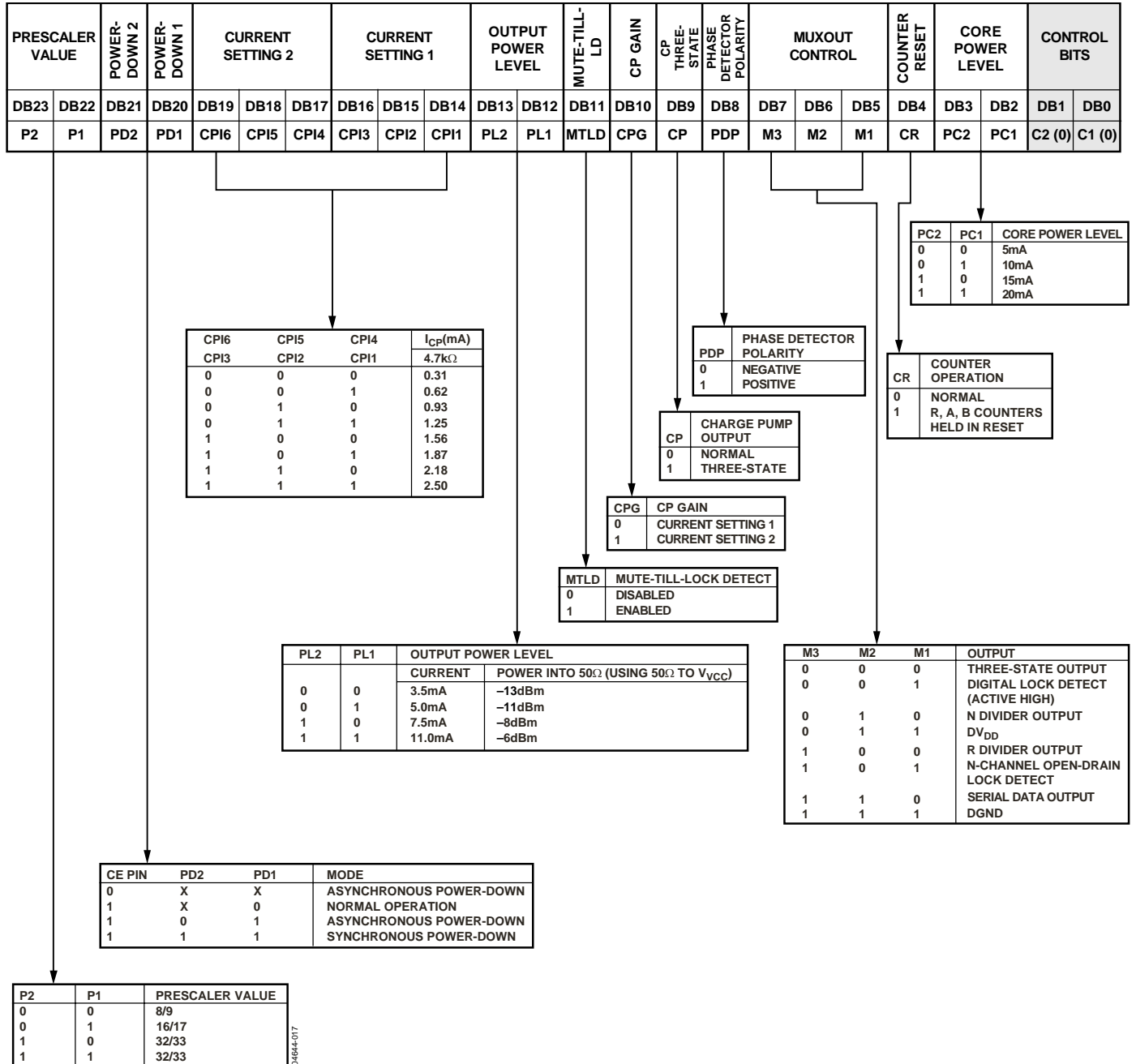
DIVIDE-BY-2 SELECT	DIVIDE-BY-2	CP GAIN	13-BIT B COUNTER													RESERVED	5-BIT A COUNTER					CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DIVSEL	DIV2	CPG	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	RSV	A5	A4	A3	A2	A1	C2 (1)	C1 (0)

R COUNTER LATCH

RESERVED	RESERVED	BAND SELECT CLOCK		TEST MODE BIT	LOCK DETECT PRECISION	ANTI-BACKLASH PULSE WIDTH	14-BIT REFERENCE COUNTER														CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RSV	RSV	BSC2	BSC1	TMB	LDP	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (1)

0464-016

Table 7. Control Latch



04844-017

Table 8. N Counter Latch

DIVIDE-BY-2 SELECT	DIVIDE-BY-2	CP GAIN	13-BIT B COUNTER													RESERVED	5-BIT A COUNTER					CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DIVSEL	DIV2	CPG	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	RSV	A5	A4	A3	A2	A1	C2 (1)	C1 (0)

THIS BIT IS NOT USED BY THE DEVICE AND IS A DON'T CARE BIT.

A5	A4	.....	A2	A1	A COUNTER DIVIDE RATIO
0	0	.....	0	0	0
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	28
1	1	.....	0	1	29
1	1	.....	1	0	30
1	1	.....	1	1	31

B13	B12	B11	.....	B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	.....	0	0	0	NOT ALLOWED
0	0	0	.....	0	0	1	NOT ALLOWED
0	0	0	.....	0	1	0	NOT ALLOWED
0	0	0	.....	1	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	8188
1	1	1	.....	1	0	1	8189
1	1	1	.....	1	1	0	8190
1	1	1	.....	1	1	1	8191

F4 (FUNCTION LATCH) FASTLOCK ENABLE	CP GAIN	OPERATION
0	0	CHARGE PUMP CURRENT SETTING 1 IS PERMANENTLY USED
0	1	CHARGE PUMP CURRENT SETTING 2 IS PERMANENTLY USED

$N = BP + A$ ; P IS PRESCALER VALUE SET IN THE CONTROL LATCH. B MUST BE GREATER THAN OR EQUAL TO A. FOR CONTINUOUSLY ADJACENT VALUES OF  $(N \times F_{REF})$ , AT THE OUTPUT,  $N_{MIN}$  IS  $(P^2 - P)$ .

DIV2	DIVIDE-BY-2
0	FUNDAMENTAL OUTPUT
1	DIVIDE-BY-2

DIVSEL	DIVIDE-BY-2 SELECT (PRESCALER INPUT)
0	FUNDAMENTAL OUTPUT SELECTED
1	DIVIDE-BY-2 SELECTED

04644-018

Table 9. R Counter Latch

RESERVED	RESERVED	BAND SELECT CLOCK		TEST MODE BIT	LOCK DETECT PRECISION	ANTI-BACKLASH PULSE WIDTH		14-BIT REFERENCE COUNTER														CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RSV	RSV	BSC2	BSC1	TMB	LDP	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (1)

THESE BITS ARE NOT USED BY THE DEVICE AND ARE DON'T CARE BITS.

TEST MODE BIT SHOULD BE SET TO 0 FOR NORMAL OPERATION.

R14	R13	R12	R3	R2	R1	DIVIDE RATIO	
0	0	0	.....	0	0	0	1
0	0	0	.....	0	1	1	2
0	0	0	.....	0	1	0	3
0	0	0	.....	1	0	1	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16380
1	1	1	.....	1	0	1	16381
1	1	1	.....	1	1	0	16382
1	1	1	.....	1	1	1	16383

ABP2	ABP1	ANTIBACKLASH PULSE WIDTH
0	0	3.0ns
0	1	1.3ns
1	0	6.0ns
1	1	3.0ns

LDP	LOCK DETECT PRECISION
0	THREE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.
1	FIVE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.

BSC2	BSC1	BAND SELECT CLOCK DIVIDER
0	0	1
0	1	2
1	0	4
1	1	8

04644-013



**POWER-UP**

**Power-Up Sequence**

The correct programming sequence for the ADF4360-0 after power-up is:

1. R counter latch
2. Control latch
3. N counter latch

**Initial Power-Up**

Initial power-up refers to programming the device after the application of voltage to the AV<sub>DD</sub>, DV<sub>DD</sub>, V<sub>VCO</sub>, and CE pins. On initial power-up, an interval is required between programming the control latch and programming the N counter latch.

This interval is necessary to allow the transient behavior of the ADF4360-0 during initial power-up to have settled. During initial power-up, a write to the control latch powers up the device and the bias currents of the VCO begin to settle. If these currents have not settled to within 10% of their steady-state value and if the N counter latch is then programmed, the VCO may not be able to oscillate at the desired frequency, which does not allow the band select logic to choose the correct frequency band and the ADF4360-0 may not achieve lock. If the recommended interval is inserted and the N counter latch is programmed, the band select logic can choose the correct frequency band and the device locks to the correct frequency.

This duration of this interval is affected by the value of the capacitor on the C<sub>N</sub> pin (Pin 14). This capacitor is used to reduce the close-in noise of the ADF4360-0 VCO. The recommended value of this capacitor is 10 μF. Using this value requires an interval of ≥ 5 ms between the latching in of the control latch bits and latching in of the N counter latch bits. If a shorter delay is required, this capacitor can be reduced. A slight phase noise penalty is incurred by this change, which is explained further in Table 10.

Table 10. C<sub>N</sub> Capacitance vs. Interval and Phase Noise

C <sub>N</sub> value	Recommended Interval between Control Latch and N Counter Latch	Open Loop Phase Noise at 10 kHz Offset
10 μF	≥ 5 ms	-84 dBc
440 nF	≥ 600 μs	-82 dBc

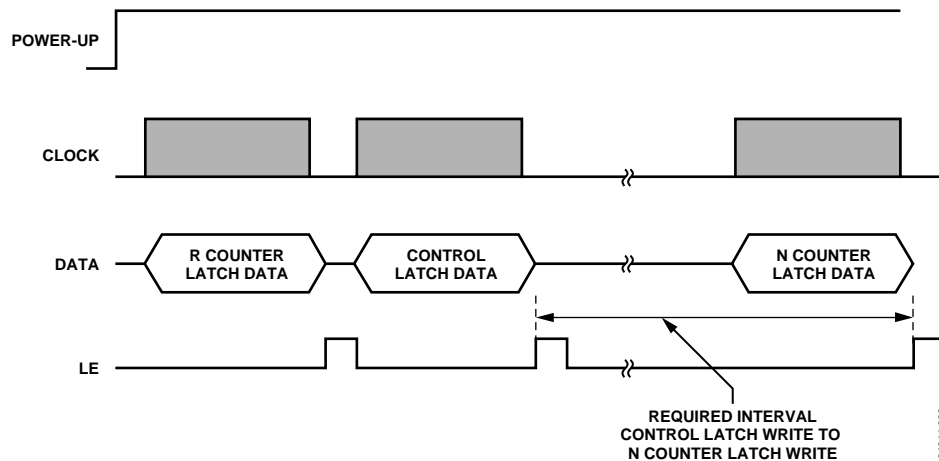


Figure 16. ADF4360-0 Power-Up Timing

**Hardware Power-Up/Power-Down**

If the ADF4360-0 is powered down via the hardware (using the CE pin) and powered up again without any change to the N counter register during power-down, it locks at the correct frequency because the device is already in the correct frequency band. The lock time depends on the value of capacitance on the  $C_N$  pin, which is <5 ms for 10  $\mu$ F capacitance. The smaller capacitance of 440 nF on this pin enables lock times of <600  $\mu$ s.

The N counter value cannot be changed while it is in power-down because the device may not lock to the correct frequency on power-up. If it is updated, the correct programming sequence for it after power-up is to the R counter latch, followed by the control latch, and finally the N counter latch, with the required interval between the control latch and N counter latch, as described in the Initial Power-Up section.

**Software Power-Up/Power-Down**

If the ADF4360-0 is powered down via the software (using the control latch) and powered up again without any change to the N counter latch during power-down, it locks at the correct frequency because it is already in the correct frequency band. The lock time depends on the value of capacitance on the  $C_N$  pin, which is <5 ms for 10  $\mu$ F capacitance. The smaller capacitance of 440 nF on this pin enables lock times of <600  $\mu$ s.

The N counter value cannot be changed while it is in power-down because the device may not lock to the correct frequency on power-up. If it is updated, the correct programming sequence for it after power-up is to the R counter latch, followed by the control latch, and finally the N counter latch, with the required interval between the control latch and N counter latch, as described in the Initial Power-Up section.

## CONTROL LATCH

With (C2, C1) = (0, 0), the control latch is programmed. Table 7 shows the input data format for programming the control latch.

### Prescaler Value

In the ADF4360-0, P2 and P1 in the control latch set the prescaler values.

### Power-Down

DB21 (PD2) and DB20 (PD1) provide programmable power-down modes.

In the programmed asynchronous power-down, the device powers down immediately after latching a 1 into Bit PD1, with the condition that PD2 has been loaded with a 0. In the programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing a 1 into Bit PD1 (on the condition that a 1 has also been loaded to PD2), the device goes into power-down on the second rising edge of the R counter output, after LE goes high. When the CE pin is low, the device is immediately disabled regardless of the state of PD1 or PD2.

When a power-down is activated (either synchronous or asynchronous mode), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry is reset.
- The RF outputs are debiased to a high impedance state.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

## Charge Pump Currents

CPI3, CPI2, and CPI1 in the ADF4360-0 determine Current Setting 1.

CPI6, CPI5, and CPI4 determine Current Setting 2. See the truth table in Table 7.

## Output Power Level

Bits PL1 and PL2 set the output power level of the VCO. See the truth table in Table 7.

## Mute-Till-Lock Detect

DB11 of the control latch in the ADF4360-0 is the mute-till-lock detect bit. This function, when enabled, ensures that the RF outputs are not switched on until the PLL is locked.

## CP Gain

DB10 of the control latch in the ADF4360-0 is the charge pump gain bit. When it is programmed to a 1, Current Setting 2 is used. When it is programmed to a 0, Current Setting 1 is used.

## Charge Pump Three-State

This bit puts the charge pump into three-state mode when programmed to a 1. It should be set to 0 for normal operation.

## Phase Detector Polarity

The PDP bit in the ADF4360-0 sets the phase detector polarity. The positive setting enabled by programming a 1 is used when using the on-chip VCO with a passive loop filter or with an active non-inverting filter. It can also be set to 0. This is required, if an active inverting loop filter is used.

## MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1. See the truth table in Table 7.

## Counter Reset

DB4 is the counter reset bit for the ADF4360-0. When this is 1, the R counter and the A, B counters are reset. For normal operation, this bit should be 0.

## Core Power Level

PC1 and PC2 set the power level in the VCO core. The recommended setting is 10 mA. See the truth table in Table 7.

**N COUNTER LATCH**

With (C2, C1) = (1, 0), the N counter latch is programmed. Table 8 shows the input data format for programming the N counter latch.

**A Counter Latch**

A5 to A1 program the 5-bit A counter. The divide range is 0 (00000) to 31 (11111).

**Reserved Bits**

DB7 is a spare bit that is reserved. It should be programmed to 0.

**B Counter Latch**

B13 to B1 program the B counter. The divide range is 3 (00.....0011) to 8191 (11.....111).

**Overall Divide Range**

The overall divide range is defined by  $((P \times B) + A)$ , where P is the prescaler value.

**CP Gain**

DB21 of the N counter latch in the [ADF4360-0](#) is the charge pump gain bit. When this is programmed to 1, Current Setting 2 is used. When programmed to 0, Current Setting 1 is used. This bit can also be programmed through DB10 of the control latch. The bit always reflects the latest value written to it, whether this is through the control latch or the N counter latch.

**Divide-by-2**

DB22 is the divide-by-2 bit. When set to 1, the output divide-by-2 function is chosen. When it is set to 0, normal operation occurs.

**Divide-by-2 Select**

DB23 is the divide-by-2 select bit. When programmed to 1, the divide-by-2 output is selected as the prescaler input. When set to 0, the fundamental is used as the prescaler input. For example, using the output divide-by-2 feature and a PFD frequency of 200 kHz, the user needs a value of  $N = 13,000$  to generate 1,500 MHz. With the divide-by-2 select bit high, the user may keep  $N = 6,500$ .

**R COUNTER LATCH**

With (C2, C1) = (0, 1), the R counter latch is programmed. Table 9 shows the input data format for programming the R counter latch.

**R Counter**

R1 to R14 set the counter divide ratio. The divide range is 1 (00.....001) to 16383 (111.....111).

**Antibacklash Pulse Width**

DB16 and DB17 set the antibacklash pulse width.

**Lock Detect Precision**

DB18 is the lock detect precision bit. This bit sets the number of reference cycles with less than 15 ns phase error for entering the locked state. With LDP at 1, five cycles are taken; with LDP at 0, three cycles are taken.

**Test Mode Bit**

DB19 is the test mode bit (TMB) and should be set to 0. With  $TMB = 0$ , the contents of the test mode latch are ignored and normal operation occurs as determined by the contents of the control latch, R counter latch, and N counter latch. Note that test modes are for factory testing only and should not be programmed by the user.

**Band Select Clock**

These bits set a divider for the band select logic clock input. The output of the R counter is by default the value used to clock the band select logic, but, if this value is too high (>1 MHz), a divider can be switched on to divide the R counter output to a smaller value (see Table 9).

**Reserved Bits**

DB23 to DB22 are spare bits that are reserved. They should be programmed to 0.

## APPLICATIONS INFORMATION

### FIXED FREQUENCY LO

Figure 17 shows the **ADF4360-0** used as a fixed frequency LO at 2.6 GHz. The low-pass filter was designed using **ADIsimPLL** for a channel spacing of 8 MHz and an open-loop bandwidth of 40 kHz. The maximum PFD frequency of the **ADF4360-0** is 8 MHz. Because using a larger PFD frequency allows users to use a smaller N, the in-band phase noise is reduced to as low as possible, -100 dBc/Hz. The 40 kHz bandwidth is chosen to be just greater than the point at which the open-loop phase noise of the VCO is -100 dBc/Hz, thus giving the best possible integrated noise. The typical rms phase noise (100 Hz to 100 kHz) of the LO in this configuration is 0.35°. The reference frequency is from a 16 MHz TCXO from Fox; thus, an R value of 2 is programmed. Taking into account the high PFD frequency and its effect on the band select logic, the band select clock divider is enabled. In this case, a value of 8 is chosen. A very simple pull-up resistor and dc blocking capacitor complete the RF output stage.

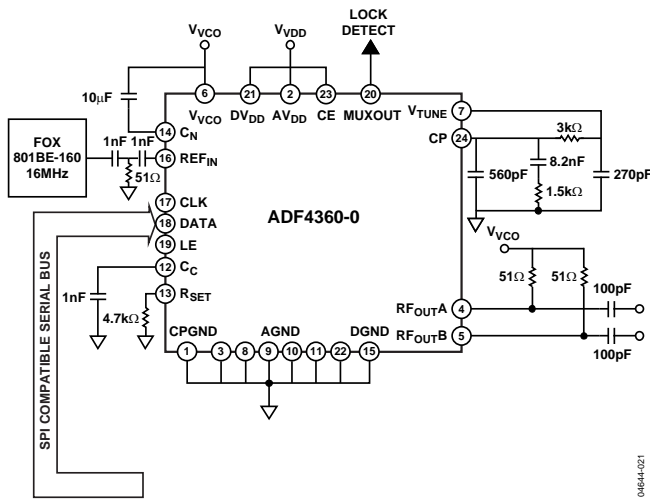


Figure 17. Fixed Frequency LO

### INTERFACING

The **ADF4360-0** has a simple SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE goes high, the 24 bits that have been clocked into the appropriate register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible is 833 kHz or one update every 1.2 µs. This is more than adequate for systems that have typical lock times in hundreds of microseconds.

### ADuC812 Interface

Figure 18 shows the interface between the **ADF4360-0** and the **ADuC812** MicroConverter®. Because the **ADuC812** is based on an 8051 core, this interface can be used with any 8051 based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the the **ADF4360-0** needs a 24-bit word, which is accomplished by writing three 8-bit bytes from the MicroConverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

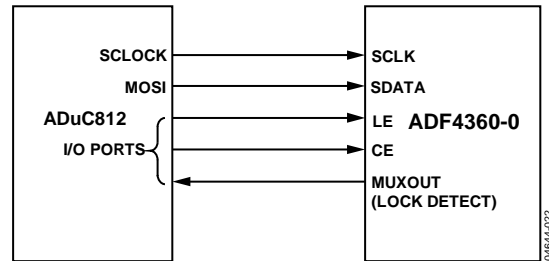


Figure 18. ADuC812 to ADF4360-0 Interface

I/O port lines on the **ADuC812** are also used to control power-down (CE input) and detect lock (MUXOUT configured as lock detect and polled by the port input). When operating in the described mode, the maximum SCLOCK rate of the **ADuC812** is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

### ADSP-2181 Interface

Figure 19 shows the interface between the **ADF4360-0** and the **ADSP-2181** digital signal processor. The **ADF4360-0** needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the **ADSP-2181** is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated.

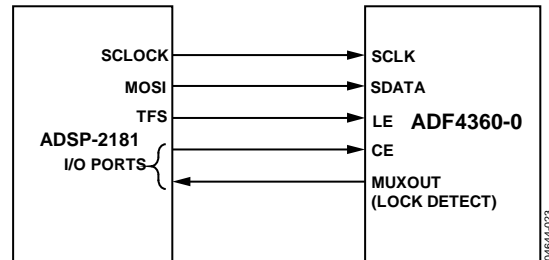


Figure 19. ADSP-2181 to ADF4360-0 Interface

Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the 8-bit bytes, enable the autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

## PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The leads on the chip scale package (CP-24) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package lead length and 0.05 mm wider than the package lead width. The lead should be centered on the pad to ensure that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern to ensure that shorting is avoided.

Thermal vias may be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at a 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 ounce of copper to plug the via.

The user should connect the printed circuit thermal pad to AGND. This is internally connected to AGND.

## OUTPUT MATCHING

There are a number of ways to match the output of the ADF4360-0 for optimum operation; the most basic is to use a 50  $\Omega$  resistor to  $V_{VCO}$ . A dc bypass capacitor of 100 pF is connected in series, as shown in Figure 20. Because the resistor is not frequency dependent, this provides a good broadband match. The output power in this circuit typically gives -6.5 dBm output power into a 50  $\Omega$  load.

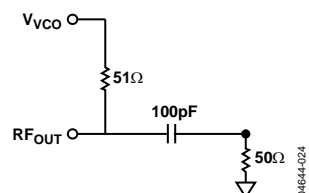


Figure 20. Simple ADF4360-0 Output Stage

A better solution is to use a shunt inductor (acting as an RF choke) to  $V_{VCO}$ . This gives a better match than a resistor and, therefore, more output power. Additionally, a series inductor is added after the dc bypass capacitor to provide a resonant LC circuit. This tunes the oscillator output and provides approximately 10 dB additional rejection of the second harmonic. The shunt inductor needs to be a relatively low value (<10 nH).

Experiments have shown that the circuit shown in Figure 21 provides an excellent match to 50  $\Omega$  over the operating range of the ADF4360-0. This gives approximately -4 dBm output power across the frequency range of the ADF4360-0. Both single-ended architectures can be examined using the EV-ADF4360-0EB1Z evaluation board.

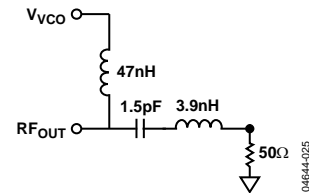


Figure 21. Differential ADF4360-0 Output Stage

If the user does not need the differential outputs available on the ADF4360-0, the user may either terminate the unused output or combine both outputs using a balun. The circuit in Figure 22 shows how best to combine the outputs.

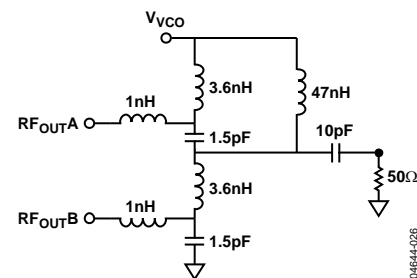
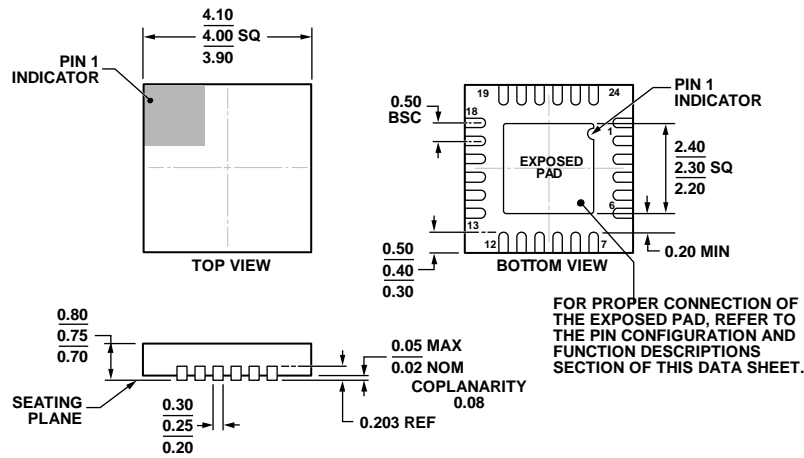


Figure 22. Balun for Combining ADF4360-0 RF Outputs

The circuit in Figure 22 is a lumped-lattice-type LC balun. It is designed for a center frequency of 2.6 GHz and outputs -1 dBm at this frequency. The series 1 nH inductor is used to tune out any parasitic capacitance due to the board layout from each input, and the remainder of the circuit is used to shift the output of one RF input by +90° and the second by -90°, thus combining the two. The action of the 3.6 nH inductor and the 1.5 pF capacitor accomplishes this. The 12 nH is used to provide an RF choke to feed the supply voltage, and the 10 pF capacitor provides the necessary dc block. To ensure good RF performance, the circuits in Figure 20 and Figure 22 are implemented with Coilcraft 0402/0603 inductors and AVX 0402 thin-film capacitors. Alternatively, instead of the LC balun shown in Figure 22, both outputs can be combined using a 180° rat-race coupler.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8.

Figure 23. 24-Lead Lead Frame Chip Scale Package [LFCS]  
4 mm × 4 mm Body and 0.75 mm Package Height  
(CP-24-14)

Dimensions shown in millimeters

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Model <sup>1</sup>	Temperature Range	Frequency Range	Package Description	Package Option
ADF4360-0BCPZ	-40°C to +85°C	2400 MHz to 2725 MHz	24-Lead Lead Frame Chip Scale Package [LFCS]	CP-24-14
ADF4360-0BCPZRL	-40°C to +85°C	2400 MHz to 2725 MHz	24-Lead Lead Frame Chip Scale Package [LFCS]	CP-24-14
ADF4360-0BCPZRL7	-40°C to +85°C	2400 MHz to 2725 MHz	24-Lead Lead Frame Chip Scale Package [LFCS]	CP-24-14
EV-ADF4360-0EB1Z			Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**



**NOTES**

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).