Applications

- High sensitivity / low power GPS and A-GPS applications
- Portable navigation devices, mobile phones and GPS peripheral devices
- Telematics equipment

Features

- Single-conversion L1-band GPS radio with integrated IF filter
- Integrated LNA; 1.6 dB typ. noise figure
- Low RF system noise figure; 2.3 dB typ.
- Low 10 mA operating current with 2.7-3.3 V supply; 8 mA with internal LNA disabled
- Standby current <10 µA
- Fully Integrated PLL, compatible with 13, 16.368, 19.5 and 26 MHz reference frequencies
- 2-bit SIGN & MAG Digital IF output
- Integrated VCO and resonator
- I/O supply range extends down to 1.7 V
- 4 x 4 mm 24 pin QFN
- Pb-free, RoHS compliant and Halogen-free

Ordering Information

Part No.	Package	Remark
SE4110L-R	24 Pin QFN	Shipped in Tape & Reel

Product Description

The SE4110L is a highly integrated GPS receiver offering high performance and low-power operation in a wide range of low-cost applications. It is particularly well-suited to mobile phone and high sensitivity L1-band GPS and A-GPS systems.

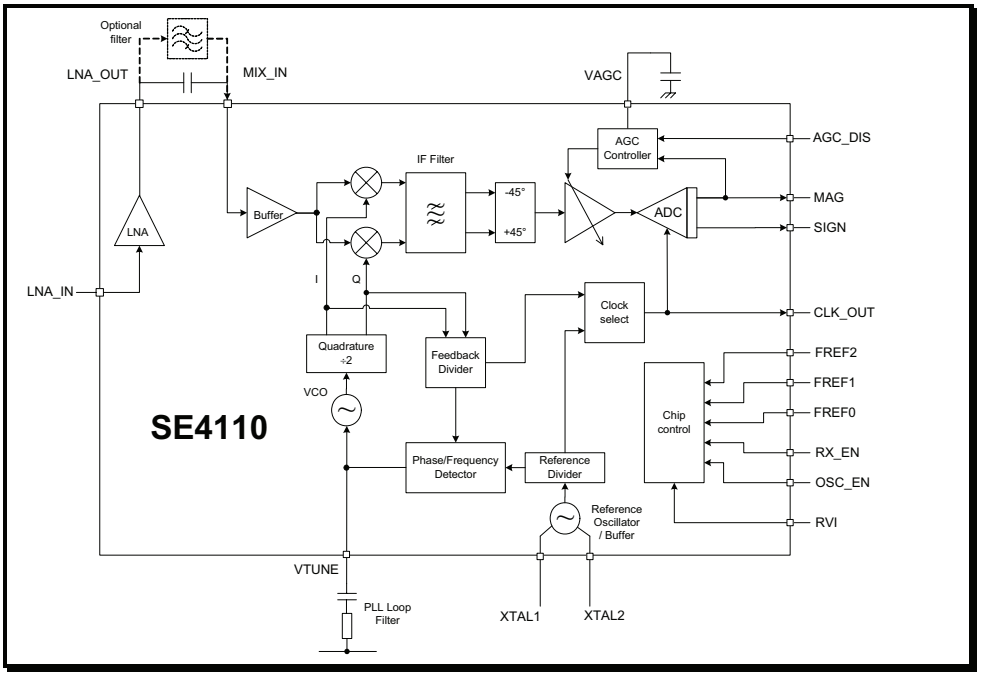
The SE4110L includes an on-chip LNA and a low IF receiver with a linear AGC and 2-bit analogue-to-digital converter (ADC). The receiver incorporates a fully integrated image reject mixer so no SAW filter is required in many applications. There is also an on-chip IF filter.

The SE4110L supports a wide range of reference frequencies, addressing both traditional GPS systems and emerging mobile phone applications. The synthesizer is highly integrated requiring only two passive components to implement an off-chip loop filter.

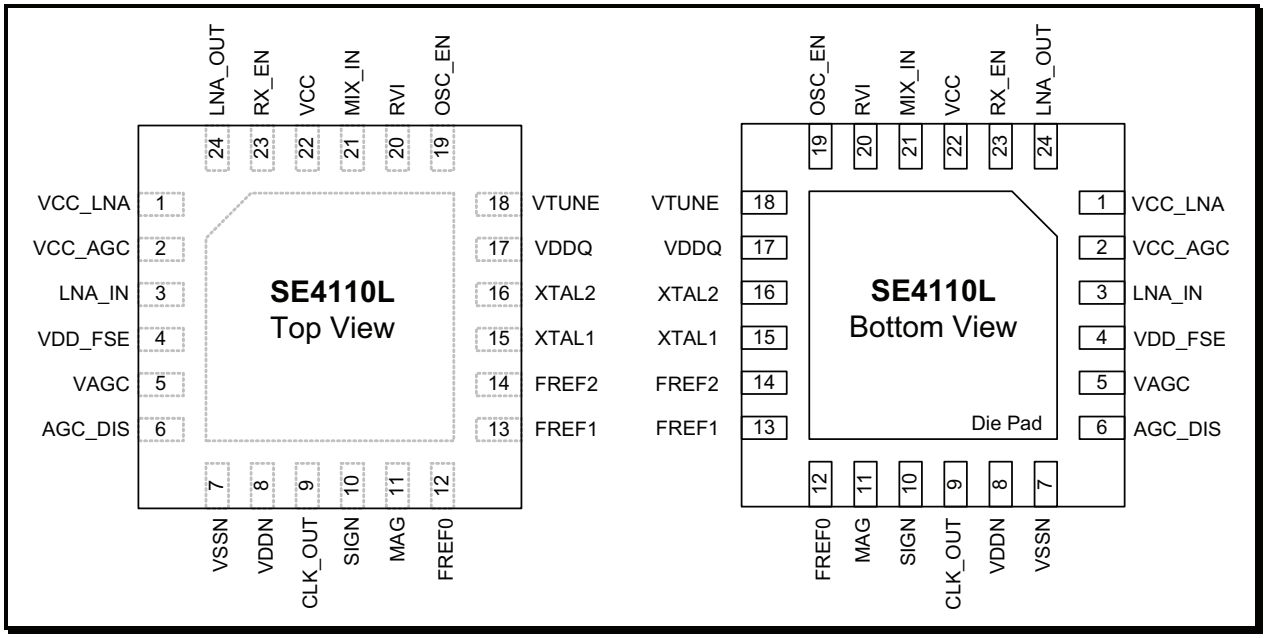
The SE4110L is optimized for the lowest possible power consumption consistent with the very low external component count.

The SE4110L incorporates current-controlled low-spurious output buffers which may optionally be run from a separate external supply to interface to low voltage systems. The buffers supply sufficient current to drive most baseband devices directly.

Functional Block Diagram



Pin Out Diagram



Pin Out Description

Pin No.	Name	Description	Connection
1	VCC_LNA	Analogue Power supply for LNA	Connect to VCC via dedicated decoupling network to enable LNA Connect to GND to disable LNA
2	VCC_AGC	Analogue Power supply for AGC	Connect to VCC
3	LNA_IN	LNA RF input	DC blocking capacitor required Connect to matching network in a compact RF layout
4	VDD_FSE	Power supply for configuration logic	Connect to VCC
5	VAGC	AGC filter capacitor	Single capacitor to GND (Pin also allows external control of AGC when AGC_DIS = '1')
6	AGC_DIS	AGC Inhibit input	AGC Gain hold (Connect to VDD) or Enable AGC (Connect to VSSN / GND)
7	VSSN	Ground return for digital interface	Connect to GND, or digital ground for baseband IC
8	VDDN	Digital Power supply for digital interface	Connect to VDD, or digital supply for baseband IC
9	CLK_OUT	Sample clock output	ADC Sample Clock output to baseband IC, at VDDN logic levels
10	SIGN	SIGN output data	ADC SIGN output to baseband IC, at VDDN logic levels
11	MAG	MAG output data	ADC MAG output to baseband IC, at VDDN logic levels
12	FREF0	Frequency Reference select pin (bit 0)	Select desired Reference / IF / CLK_OUT frequency plan as per "FREF Hardware Configuration" Table (Connect to RX_EN or VSSN / GND as required)
13	FREF1	Frequency Reference select pin (bit 1)	
14	FREF2	Frequency Reference select pin (bit 2)	
15	XTAL1	Crystal / TCXO connection	If using TCXO reference source: Connect to AC coupled TCXO reference signal If using Crystal reference source: Connect one lead of Crystal to Crystal input 1 (XTAL1)
16	XTAL2	Crystal Connection	If using TCXO reference source: Leave unconnected If using Crystal reference source: Connect other lead of Crystal to Crystal input 2 (XTAL2)
17	VDDQ	Power supply for quiet digital circuits	Connect to VCC
18	VTUNE	VCO tuning voltage input / PLL Phase-detector output	Connect to PLL Loop Filter network

Pin No.	Name	Description	Connection
19	OSC_EN	Crystal oscillator enable	If using TCXO reference source (NO crystal oscillator needed): Connect to VSSN / GND If using Crystal reference source, with crystal oscillator: Connect to VDD
20	RVI	Program baseband output drive current	Leave unconnected or Connect via a resistor to analogue VCC for up to 2x output drive current
21	MIX_IN	Mixer input	DC coupled RF input to RF Mixer
22	VCC	Analogue Power supply for RF front end	Connect to VCC
23	RX_EN	Receiver enable	Connect to VDD to enable Radio Connect to VSSN / GND to disable Radio
24	LNA_OUT	LNA RF output	RF output from LNA. DC blocked, with 10 kΩ (nom) DC impedance to ground.
Die Pad	GND	Ground connection	Main IC GND Connection

Functional Description

LNA

The internal LNA allows a high-performance, low-power GPS receiver to be completed without using any additional active components.

The GPS L1 input signal which is applied to LNA_IN (pin 3), is a spread-spectrum signal centered on 1575.42 MHz with a 1.023 Mbps BPSK modulation. The signal level at the antenna is typically -130 dBm in open-sky conditions, dropping to below -150 dBm in masked signal areas (e.g. indoors). The LNA noise figure is the largest contributor to the sensitivity so it is an important parameter; the lower, the better.

The LNA input requires a minimum of external matching components to achieve good RF gain with minimal noise figure: only a single series inductor and single shunt capacitor are required. The input requires a DC blocking capacitor if circuitry prior to the LNA has a DC bias. Although attention should be paid to track lengths and interference throughout the design, the LNA input matching circuit is the only RF circuit critically sensitive to layout.

The LNA output includes internal 50 Ω matching for connection to the mixer input, either directly or via an optional external filter.

In applications where the internal LNA is not required, the LNA can be disabled by connecting VCC_LNA (pin 1) to GND. This will save approximately 1.9 mA of active current.

Mixer RF Input

The mixer RF input, MIX_IN (pin 21), is a single-ended 50 Ω input designed to interface either to LNA_OUT (pin 24) or to the output of an external filter. An external active antenna can also be connected to the mixer input.

The image reject mixer ensures that the receiver's full sensitivity is achieved without an external filter. For applications where additional selectivity is required, an external filter can be added between the LNA_OUT and MIX_IN pins.

IF Filter

The SE4110L includes a fully integrated Intermediate Frequency (IF) filter which provides excellent interference rejection with no additional external components. The filter has a 3rd order Butterworth bandpass response.

The bandpass response has a nominal bandwidth of 2.2 MHz; the nominal center frequency is preset to 4.092 MHz. These parameters ensure very low implementation loss in all frequency plan configurations.

AGC and ADC

The SE4110L features a linear IF chain with 2-bit SIGN / MAG ADC. SIGN is on pin 10, and MAG on pin 11.

An Automatic Gain Control (AGC) system is included. This provides over 40 dB of gain control range so that the output signal level is held at an optimum level at the input of the ADC.

The MAG data controls the AGC loop, such that the MAG bit is active (HIGH) for approximately 33 % of the time.

The SIGN and MAG signals are latched by the rising edge of the sample clock, CLK_OUT (pin 9). The SIGN and MAG signals are best sampled by the GPS baseband IC on the rising edge of CLK_OUT, for optimum sample and hold in the ADC.

The AGC time constant is determined by a single external capacitor, connected between VAGC (pin 5), and VSSN / GND. The settling-time of the AGC is within 10ms with a 10nF capacitor.

The AGC system also features a control-inhibit facility, via AGC_DIS (pin 6). By connecting AGC_DIS to VDDN, the internal AGC controller is inhibited, and the gain held at the level set prior to the inhibition. While the AGC controller is inhibited, it is possible to control the AGC gain from an external source by applying a low-impedance voltage to VAGC (pin 5).

PLL and Loop Filter

The entire phase-locked loop (PLL) generating the local oscillator for the mixer is contained on-chip, with the exception of the PLL loop filter.

A PLL loop filter can be implemented by attaching a series capacitor (220 pF) and a resistor (33 kΩ) between VTUNE (pin 18) and GND / VSSN. The PLL follows a classic 3rd-order response; this is achieved in conjunction with an on-chip 10 pF capacitor connected between VTUNE and GND / VSSN. Typical PLL Loop Bandwidth is set to be 200 kHz.

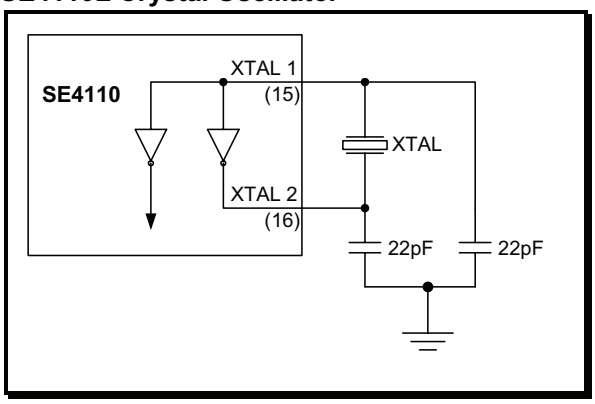
The reference frequency for the PLL may be supplied either externally or using the on-chip crystal oscillator.

Crystal Oscillator

The SE4110L features a very low power crystal oscillator which may be used to provide the frequency reference. The oscillator is designed to work with parallel resonant crystals or be driven from an external TCXO.

The crystal drive level is carefully controlled so that the device is well-suited for use with miniature surface mount crystals. The crystal oscillator is a Pierce configuration, as shown in the diagram below. The application circuit is designed to work with parallel resonant crystals with a parallel load capacitance of approx. 10 pF.

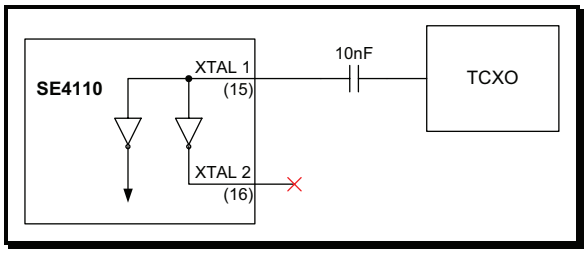
SE4110L Crystal Oscillator



The PCB layout should avoid excessive track length between XTAL1 (pin 15) and XTAL2 (pin 16) and the crystal. The capacitors at each terminal of the crystal should be mounted adjacent to the crystal and have a low impedance connection to the ground plane in order to maintain the Oscillator Loop Gain and Phase-Noise performance under all conditions.

The SE4110L can also be used with an external TCXO as shown below. The TCXO should provide a clipped sinewave signal. The XTAL2 pin should be left unconnected in this configuration.

SE4110L TCXO Connection



Clock and Data Output Coupling

The high input sensitivity achieved by the SE4110's internal LNA requires careful control of harmonically related sources of interference.

For this reason the CLK_OUT (pin 9), SIGN (pin 10) and MAG (pin 11) outputs provide carefully controlled current and slew-rate. The data and clock outputs of the SE4110L are specified to drive up to 10pF load (max standard CMOS input capacitance). The output drive of the SE4110L can be adjusted with a resistor connected between VDDQ (pin 17) and RVI (pin 20), as shown in the Logic Level Characteristics section below.

The output current drive is determined by a bias current ratio internal to the SE4110L and the external resistor.

Frequency Plan Selection

The SE4110L supports operation with a range of reference frequencies, aimed at both 'traditional' GPS and the emerging cellular GPS applications.

The supported frequency plans are tabulated below.

A (+) sign on the IF (output) frequency denotes that the digital signal is not spectrally inverted with respect to the RF input at 1575.42 MHz, as a result of the RF mixer using a low-side Local Oscillator.

A (-) sign indicates that there is a spectral inversion to be taken into account, as a result of the RF mixer using a high-side Local Oscillator.

Supported Frequency Plans

Reference frequency	Intermediate Frequency (SIGN/MAG pins)	Sample clock (CLK_OUT pin)
13 MHz	-4.080 MHz	19.5 MHz
16.368 MHz	+4.092 MHz	16.368 MHz
19.5 MHz	-4.080 MHz	19.5 MHz
26 MHz	-4.080 MHz	19.5 MHz

The frequency plan may be configured by connecting the FREF<2:0> inputs (pins 12, 13, and 14) to RX_EN (pin 23) for Logic '1', or VSSN for Logic '0'.

The following truth table gives the settings for hardware configuration.

FREF Hardware Configuration

Reference frequency	Selection value (FREF<2:0>)
16.368 MHz	000
13 MHz	100
19.5 MHz	101
26 MHz	110

Power Management

The SE4110L has 3 levels of power control: standby, oscillator only and active. These are controlled by two enable pins, RX_EN (pin 23) and OSC_EN (pin 19). A table showing the Power Control states follows:

SE4110L Power Control States

RX_EN	OSC_EN	Power state
0	0	Standby
0	1	Oscillator only
1	0	Fully active (external reference)
1	1	Fully active (internal oscillator)

In standby mode, all circuits are off and the device consumes only leakage current.

The oscillator-only mode is provided for applications where it is required to keep the sample clock (CLK_OUT (pin 9)) available when active GPS reception is not needed. This feature allows a clock to be maintained with reduced current consumption, but is not available in the 13 MHz mode.

There are two settings in the SE4110L Power Control States table for fully active operation depending on whether an external signal or the internal crystal oscillator is used to provide the reference frequency. When using an external reference, approximately 0.4 mA of supply current is saved.

The RX_EN input, (pin 23), has a 1.5MΩ pull-down resistor to GND, on-chip. This ensures that the RFIC will put itself in standby (or oscillator only mode if OSC_EN is controlled separately) when the RX_EN controller on the baseband is tri-stated to an impedance much greater than 1.5MΩ.

The internal LNA can be disabled by connecting the Vcc supply connection to the LNA, VCC_LNA (pin 1) to GND. This may be desirable in some applications, and prevents the LNA from consuming any current, saving approximately 1.9 mA.

Logic Interfacing

The SE4110L Logic Inputs can either be driven from an external baseband IC, or permanently set by connecting to either VDDN (pin 8) for Logic '1', or VSSN (pin 7) for Logic '0'. The digital interface on the SE4110L, supplied from VDDN, has been designed to operate at the same voltage as the GPS baseband IC across a wider voltage range than the RF sections of the device. It will accommodate the lower voltage baseband ICs down to 1.7 V. The SE4110L Logic Input signals are shown in the following table:

SE4110L Logic Inputs

Pin	Name	Description	Logic
6	AGC_DIS	AGC Inhibit Input	'1' Hold AGC Gain '0' Enable AGC
12	FREF0	Frequency Reference Select (bit 0)	See table: *"FREF Hardware Configuration"*
13	FREF1	Frequency Reference Select (bit 1)	
14	FREF2	Frequency Reference Select (bit 2)	
19	OSC_EN	Crystal oscillator enable	'1' Crystal source with osc enabled '0' TCXO source with osc disabled
23	RX_EN	Radio enable	'1' Enable radio '0' Standby mode

Power-up Sequencing

To use the SE4110L device with either the FREF0 (pin 12), FREF1 (pin 13) or FREF2 (pin 14) connections set to a logic '1' to enable one of the Hardware Configurations described above, it is recommended that the pins concerned are connected directly to the signal driving RX_EN (pin 23). The RX_EN signal should be set to VDD levels (logic '1') a short time (>100us) *after* main VCC/VDD power is applied to the SE4110L device.

Absolute Maximum Ratings

These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of the device. Avoid operating the device outside the recommended operating conditions defined below. This IC can be damaged by electro-static discharges. Handling and assembly of this device should be at ESD protected workstations.

Symbol	Parameter	Note	Min.	Max.	Unit
V_{CC}/V_{DD}	Supply Voltage	1	-0.3	+3.6	V
V_X	Voltage On Any Pin With Respect To V_{SSN}	1	-0.3	V_{DD}+0.3	V
LNA_IN_{MAX}	LNA input power	1	-	+3	dBm
ESD	Electrostatic Discharge Immunity (HBM)	1, 2	-	2	kV
T_{STG}	Storage Temperature Range	1	-40	+150	°C
T_{SLDR}	Solder Reflow Temperature	1	-	+260	°C

Note: (1) No damage assuming only one parameter is set at limit at a time with all other parameters set at or below the recommended operating conditions.
(2) ESD checked to the Human Body Model (HBM). A charged 100 pF capacitor discharged through a switch and 1.5kΩ series resistor into the component.

Recommended Operating Conditions

Symbol	Parameter	Note	Min.	Max.	Unit
T_A	Ambient Operating Temperature	-	-40	+85	°C
V_{CC}	Main Supply Voltage	1	2.7	3.6	V
V_{DDN}	Digital I/O Supply Voltage	-	1.7	3.6	V

Note: (1) All supply pins except V_{DDN}.

DC Electrical Characteristics

Conditions: $V_{CC} = V_{DD} = 3.3$ V, $T_A = 25$ °C

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
I_{CC}	Total Supply Current, All Circuits Active (16.368 MHz reference)	1	-	10	-	mA
	Total Supply Current, All Circuits Active (13, 19.5, 26 MHz reference)	1	-	10.5	-	mA
$I_{CC(OSC)}$	Total supply Current, Receiver Shut Down, Clock Circuits Only Active (16.368 & 19.5 MHz reference)	2	-	1	-	mA
$I_{CC(OFF)}$	Supply Current, All Circuits Shut Down	-	-	3	10	µA
$I_{CC(LNA)}$	LNA supply Current	-	-	1.9	-	mA

Note: (1) Using on-chip crystal oscillator with SIGN (pin 10), MAG (pin 11) and CLK_OUT (pin 9) outputs unloaded.
(2) Oscillator-only mode unavailable in 13 and 26 MHz reference mode

AC Electrical Characteristics, LNA

Conditions: V_{CC} = V_{DD} = 3.3 V, T_A = 25 °C, f_{RF} = 1575.42 MHz unless otherwise stated

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
S_{21}	Forward Gain	-	-	16	-	dB
NF	Noise Figure	1	-	1.6	-	dB
S_{11}	Input 50 Ω return loss	1	-	5	-	dB
S_{22}	Output 50 Ω return loss, f_{RF} = 1570 MHz to 1580 MHz	-	-	14	-	dB
P_{1dB}	1dB Input Gain Compression	-	-	-30	-	dBm
-	1dB GPS Signal Input Gain Compression (1575.42 MHz) in presence of CW Blocking Signal	-	-	-	-	-
$P_{1dBLNBLK}$	1227.6 MHz (GPS L2) 824 - 849 MHz (GSM850) 880 - 915 MHz (GSM900) 1710 - 1785 MHz (DCS) 1850 - 1910 MHz (PCS) 1920 – 1980 MHz (W-CDMA) 2.4 -2.5 GHz (WLAN/Bluetooth)	2, 3	-	-26.0 -24.0 -23.5 -27.5 -24.0 -23.0 -8.5	-	dBm
t_R	Recovery Time From 0 dBm Input Overload Signal	4	-	1.5	-	µs

Note: (1) With specified input matching network
(2) 1575.42MHz signal for blocking measurement is CW at a fixed level of -50dBm
(3) Levels do not include effects of any external RF filtering
(4) LNA has recovered when forward gain (S_{21}) has resettled to achieve its minimum specification limit.

AC Electrical Characteristics, Receiver

Conditions: V_{CC} = V_{DD} = 3.3 V, T_A = 25 °C, f_{RF} = 1575.42 MHz unless otherwise stated

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
NF	Noise Figure, f_{RF} = 1570 MHz To 1580 MHz, Input to 'MIX_IN'	-	-	10	-	dB
S_{11}	Input 50 Ω return loss, f_{RF} = 1570 MHz to 1580 MHz	-	-	16	-	dB
f_{IF}	IF Center Frequency, FREF<2:0> = 100 (13 MHz reference)	1	-	-4.080	-	MHz
	IF Center Frequency, FREF<2:0> = 000 (16.368 MHz reference)	1	-	+4.092	-	MHz
	IF Center Frequency, FREF<2:0> = 101 (19.5 MHz reference)	1	-	-4.080	-	MHz
	IF Center Frequency, FREF<2:0> = 110 (26 MHz reference)	1	-	-4.080	-	MHz
M_{IX_IR}	Mixer Image Rejection	2	20	30	-	dB
BW	-3dB Bandwidth	3	-	2.2	-	MHz
A_{RIP}	Amplitude ripple , $f_C \pm 512$ kHz	-	-	0.5	-	dBpp
ΔT_g	Group Delay Variation, $f_C \pm 512$ kHz	-	-	60	-	ns
Av_2	Selectivity At $f_C \pm 2$ MHz	-	-	8	-	dB
Av_4	Selectivity At $f_C \pm 4$ MHz	-	-	23	-	dB
P_{MAX}	Maximum signal load at MIX_IN (pin 21) (for normal AGC operation)	4	-	-	-137	dBm/Hz
-	1dB GPS Signal Gain Compression (1575.42 MHz) in presence of CW Blocking Signal	-	-	-	-	-
$P_{1dBRXBLK}$	1227.6 MHz (GPS L2) 824 - 849 MHz (GSM850) 880 - 915 MHz (GSM900) 1710 - 1785 MHz (DCS) 1850 - 1910 MHz (PCS) 1920 – 1980 MHz (W-CDMA) 2.4 -2.5 GHz (WLAN/Bluetooth)	5, 6	-	-32.0 -35.0 -35.5 -30.5 -29.5 -28.5 -26.0	-	dBm
t_R	Recovery Time From -20 dBm Input Overload Signal	7	-	3	-	µs

Note:
(1) Positive IF frequency denotes no spectral inversion, negative frequency has inverted spectrum
(2) Ratio of level through mixer between wanted input signal at 1575.42MHz and image signal at 1567.236MHz.
(3) Centered at IF CF = 4.092 MHz.
(4) The application should be designed to meet this maximum level across 1575.42 ±5 MHz. An absence of strong interferers is assumed.
(5) 1575.42MHz signal for blocking measurement is CW at a fixed level of -101dBm.
(6) Levels do not include effects of any external RF filtering.
(7) AGC loop disabled. Receiver is deemed to have recovered when the rms signal level in the ADC has resettled to its initial value ±1.5 dB.

AC Electrical Characteristics, VCO and Local Oscillator

Conditions: $V_{CC} = V_{DD} = 3.3$ V, $T_A = 25$ °C

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
f_{LO}	LO Centre Frequency (16.368 MHz reference)	1	-	1571.328	-	MHz
	LO Centre Frequency (13, 19.5 & 26 MHz reference)	1	-	1579.5	-	MHz
L_{1k}	LO SSB Phase Noise At 1 kHz Offset	2	-	-86	-	dBc/Hz
L_{10k}	LO SSB Phase Noise At 10 kHz Offset	2	-	-88	-	dBc/Hz
L_{100k}	LO SSB Phase Noise At 100 kHz Offset	2	-	-83	-	dBc/Hz
f_{CLK}	Sample clock output frequency (16.368 MHz reference)	-	-	16.368	-	MHz
	Sample clock output frequency (13, 19.5 & 26 MHz reference)	-	-	19.5	-	MHz

Note: (1) VCO frequency operates at 2x LO frequency.
(2) Typical PLL Loop Bandwidth = 200 kHz

AC Electrical Characteristics, Crystal Oscillator

Conditions: $V_{CC} = V_{DD} = 3.3$ V, $T_A = 25$ °C

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
f_{XTAL}	Oscillator Frequency	-	13	-	26	MHz
	Recommended crystal parameters					
R_X	ESR	1, 2			80	Ω
C_{LOAD}	Load capacitance			10		pF
P_X	Drive power specification		50			µW
t_{START}	Oscillator Startup Time To 95 % Of Final Amplitude And Within 10 ppm Of Final Frequency	-	-	2	-	ms
V_{IN}	External oscillator drive level	-	0.2	1	-	V p-p
C_{IN}	External oscillator Input Load Capacitance	3	-	0.5	-	pF

Note: (1) Recommended crystal parameters assume a parallel, fundamental mode crystal is used.
(2) Valid for a 13 MHz crystal.
(3) Connected TCXO to XTAL1 (pin 15) input

Logic Level Characteristics

Conditions: V_{CC} = V_{DD} = 3.3 V, T_A = 25 °C

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
V_{IH}	Logic High Input Voltage	1	0.7V_{DDN}	-	V_{DDN}	V
V_{IL}	Logic Low Input Voltage	1	0	-	0.3V_{DDN}	V
I_{IH}	Input Current Logic High Voltage	1	-	200	-	nA
$I_{IH\_RX\_EN}$	Input Current Logic High Voltage for RX_EN Input (pin 23)	2	-	2.2	-	µA
I_{IL}	Input Current Logic Low Voltage	1	-	-200	-	nA
C_{ILOAD}	Input Load Capacitance	1	-	-	2	pF
V_{OH}	Logic High Output Voltage	3	V_{DDN} - 0.1V	-	V_{DDN}	V
V_{OL}	Logic Low Output Voltage	3	0	-	0.1	V
I_{OH}	Output Current Logic High Voltage	3, 4	-	1.45	-	mA
I_{OL}	Output Current Logic Low Voltage	3, 4	-	-1.45	-	mA
C_{OLOAD}	Output Load Capacitance	3	-	-	10	pF

Note: (1) Applies to all Logic pins used as inputs: AGC_DIS (pin 6), FREF0 (pin 12), FREF1 (pin 13), FREF2 (pin 14), OSC_EN (pin 19) and RX_EN (pin 23).
(2) Applies to RX_EN (pin 23) only. Figure dominated by 1.5 MΩ (nom) on-chip pull-down resistor.
(3) Applies to all Logic pins used as outputs: CLK_OUT (pin 9), SIGN (pin 10), and MAG (pin 11).
(4) Output Current set at Nominal level; no Current Setting Resistor on RVI (pin 20). Positive value indicates current source; negative value indicates current sink.

Logic Output Current Drive Adjustment Settings

The Logic Outputs on the SE4110L can be adjusted to compensate for parasitics in application board layout. This can be achieved by adding a resistor between RVI (pin 20) and VDDQ (pin 17) as shown below.
The additional interface capacitance of PCB tracking and connectors between the SE4110L output and baseband IC input is included in these figures.
These figures are Typical only, and are not guaranteed across temperature and silicon process.

Conditions: V_{CC} = V_{DD} = 3.3 V, T_A = 25 °C

Current Setting Resistor Value (RVI (pin 20) to VDDQ (pin 17)) (Ω)	Maximum Allowable Capacitive Loading (pF)	Current Drive Level
Not Fitted	5	Nominal
100K	6	X 1.2
39K	7	X 1.4
0R	10	X 2.0

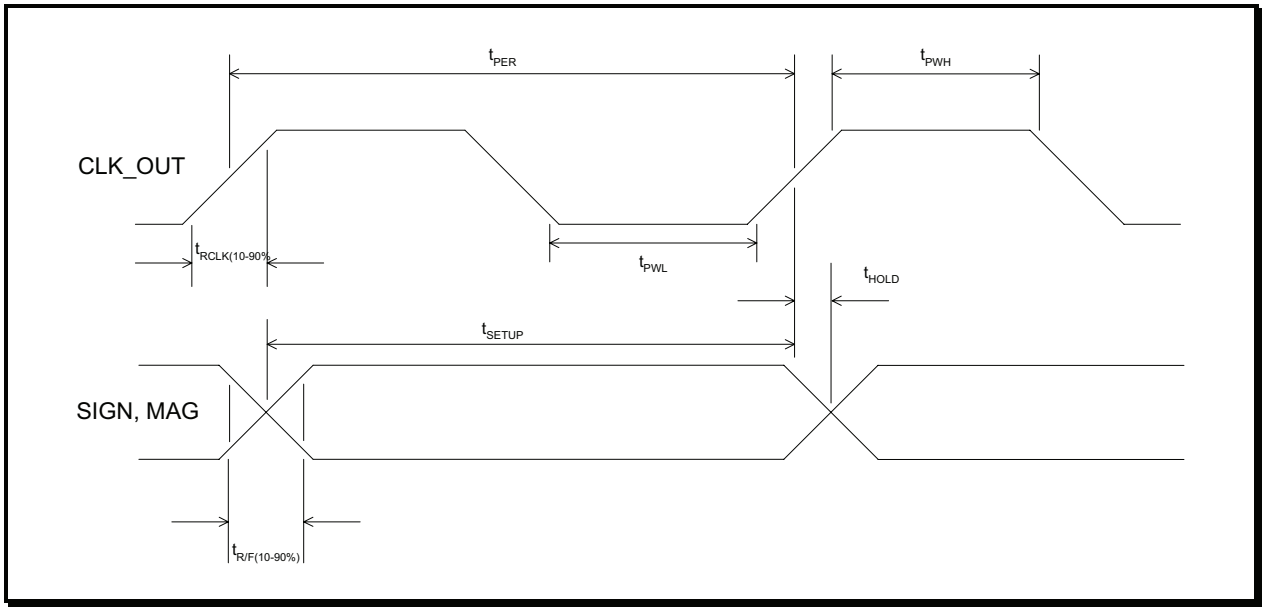
Logic Timing Characteristics

Conditions: $C_L \leq 10$ pF, $V_{CC} = V_{DD} = 3.3$ V, $T_A = 25$ °C at Maximum Buffer Current

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
t_{PER}	Clock Period	-	51.2	-	61.1	ns
t_{PWL}	Clock Low Width	1	10	-	-	ns
t_{PWH}	Clock High Width	1	10	-	-	ns
t_{SETUP}	Setup Time	1	10	-	-	ns
t_{HOLD}	Hold Time	-	1.7	-	-	ns
t_{RCLK}	Rise Time CLK_OUT, 10 - 90%	1	-	-	17	ns
$t_{R/F}$	Rise and Fall Time SIGN/MAG, 10 - 90%	1	-	-	17	ns

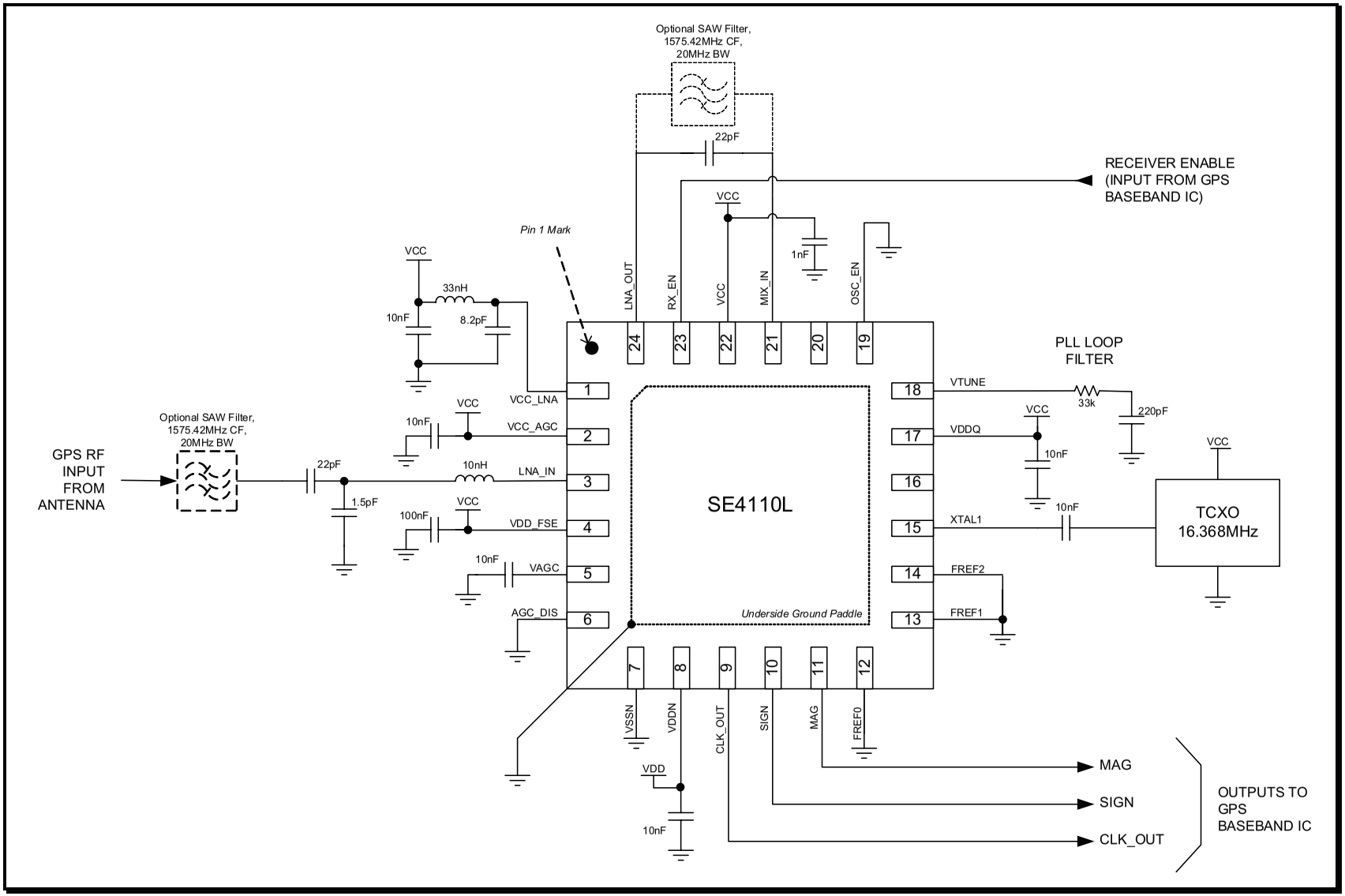
Note: (1) Values dependent on output drive level, determined by resistor on RVI (pin 20).

Logic Output Data Timing Diagram

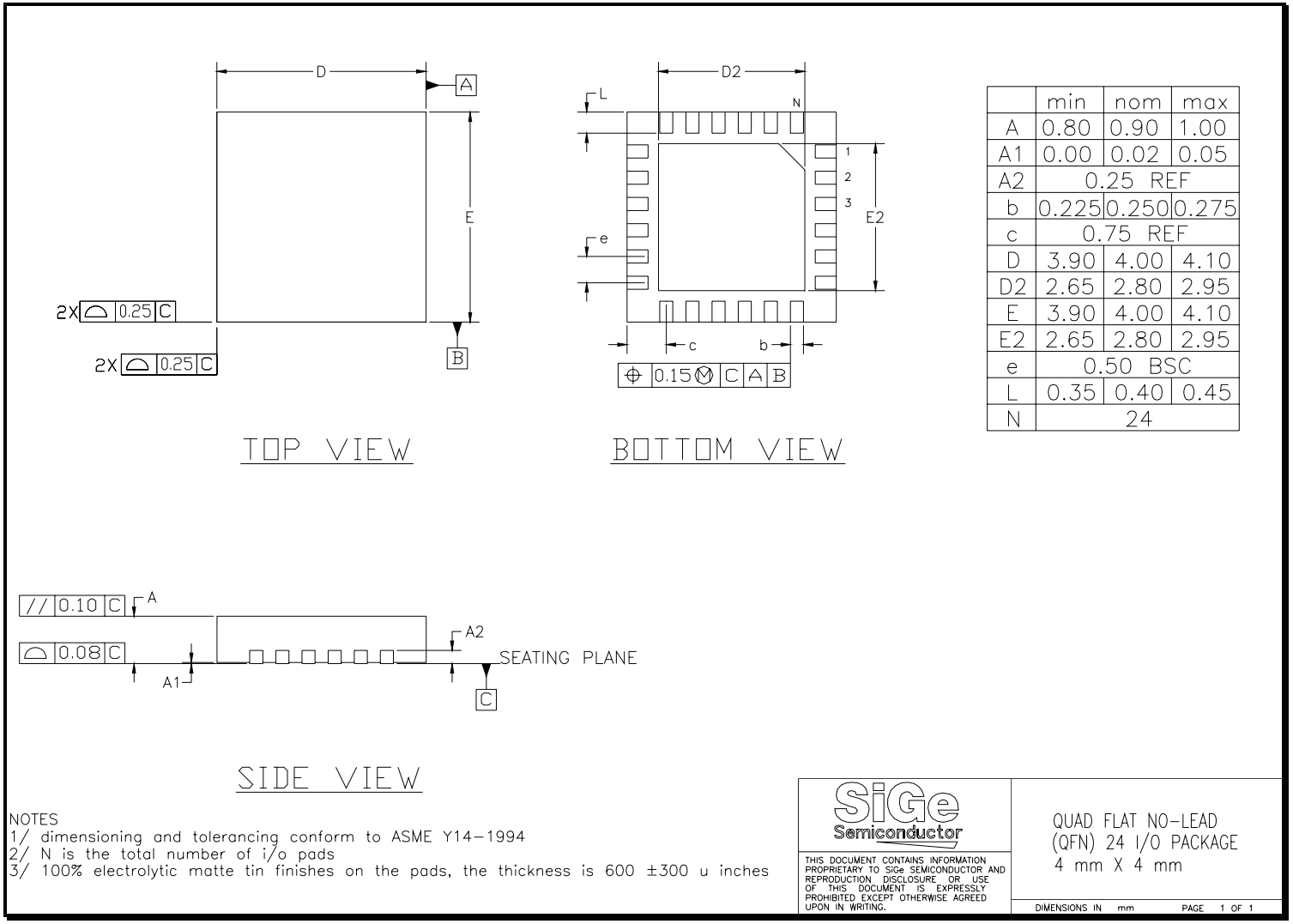


Conditions: (1) Cload SIGN/MAG ≤ 10pF
(2) Cload CLK_OUT ≤ Cload SIGN/MAG
(3) Output drive set to Maximum: RVI (pin 20) directly connected to VDDQ (pin 17)

Typical Application Circuit Diagram



Package Information



	min	nom	max
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.25 REF	
b	0.225	0.250	0.275
c		0.75 REF	
D	3.90	4.00	4.10
D2	2.65	2.80	2.95
E	3.90	4.00	4.10
E2	2.65	2.80	2.95
e		0.50 BSC	
L	0.35	0.40	0.45
N		24	

Note: This package is Pb-free, RoHS compliant and Halogen-free. The product is rated MSL1.

Recommended PCB Footprint – PCB Metal & Solder Mask

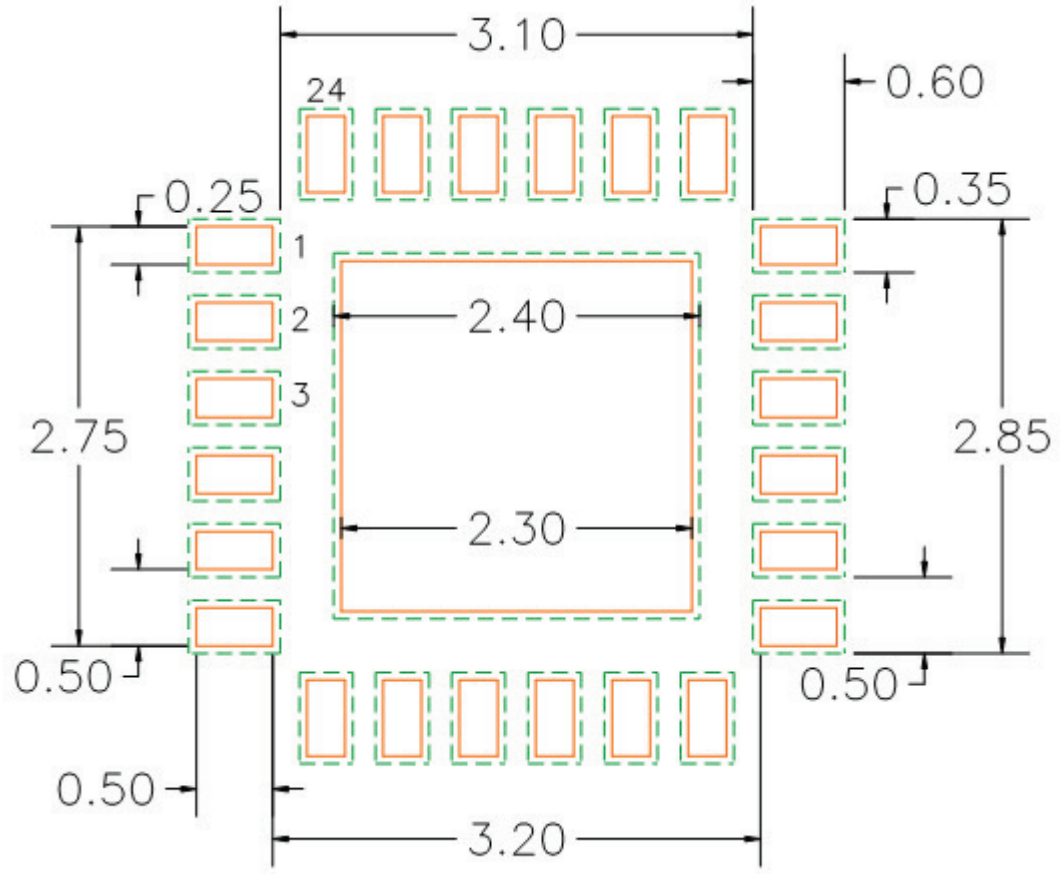
The PCB footprint below is only for reference.

This footprint is a Non-Solder Mask Defined layout [NSMD]. The dotted-green lines define the solder mask apertures. The solid-red lines define the metal pad sizes.

The user should modify the design layout in order to meet their specific solder fillet requirements & solder joint reliability requirements.

All dimensions in the figure below are in mm.

SE4110L QFN 24-pin [4x4mm] PCB Footprint



Scale 20:1 **Units in mm**

Recommended PCB Footprint – Stencil Apertures Pattern

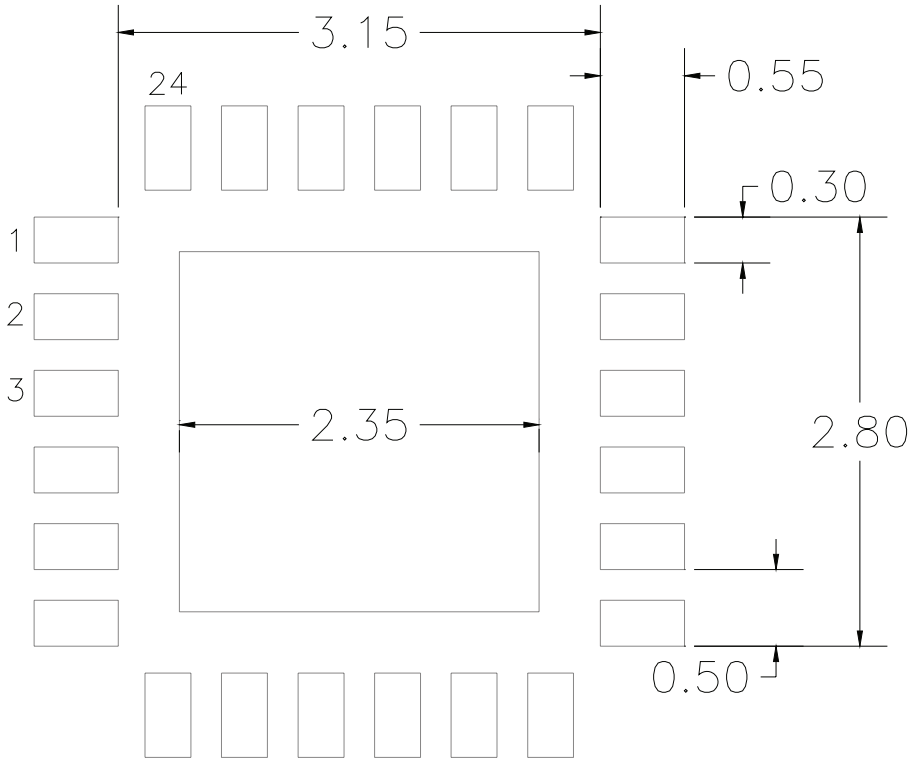
The stencil apertures design below is only for reference.

It is based on a 6 mil [0.15 mm] stencil thickness with apertures oversized by 1 mil [0.025 mm] on the pad metal.

The user should modify the design layout in order to meet their particular solder fillet & solder joint reliability requirements.

All dimensions in the figure below are in mm.

SE4110L QFN 24-pin [4x4mm] PCB Footprint – Stencil Pattern

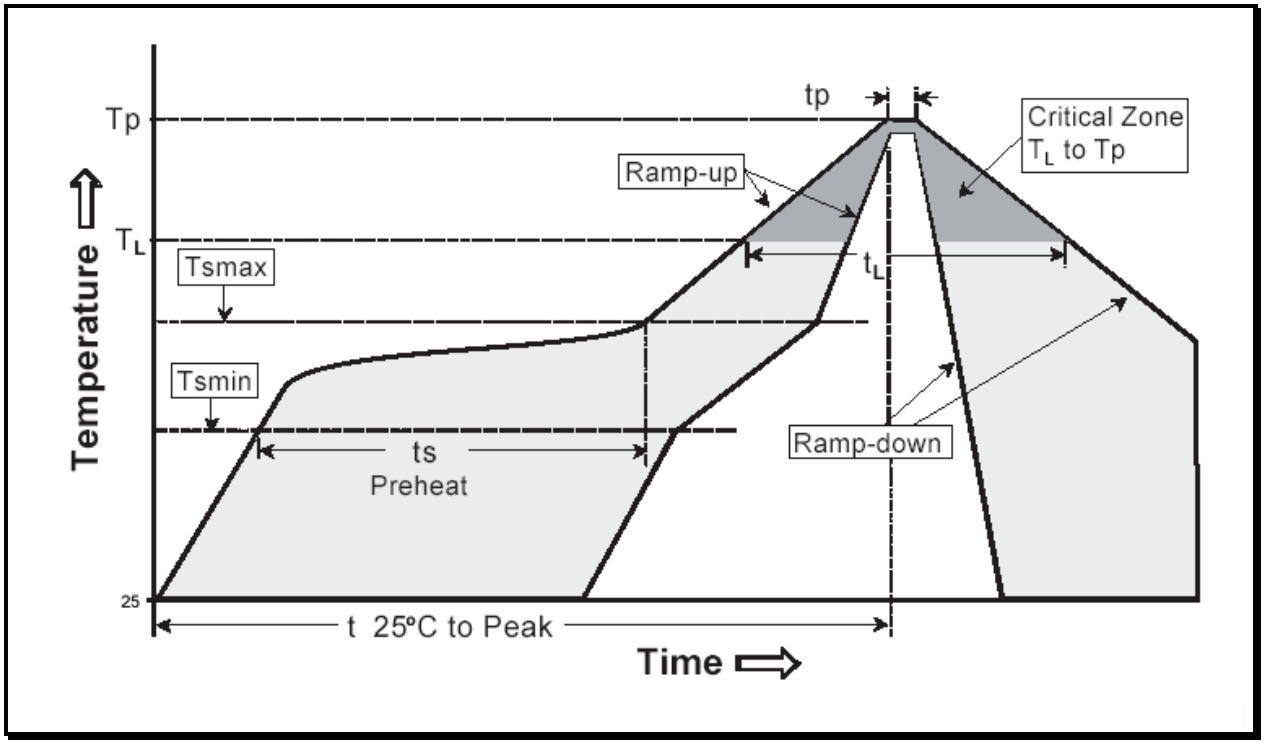


Scale 20:1 **Units in mm**

Recommended Reflow Temperature Profile

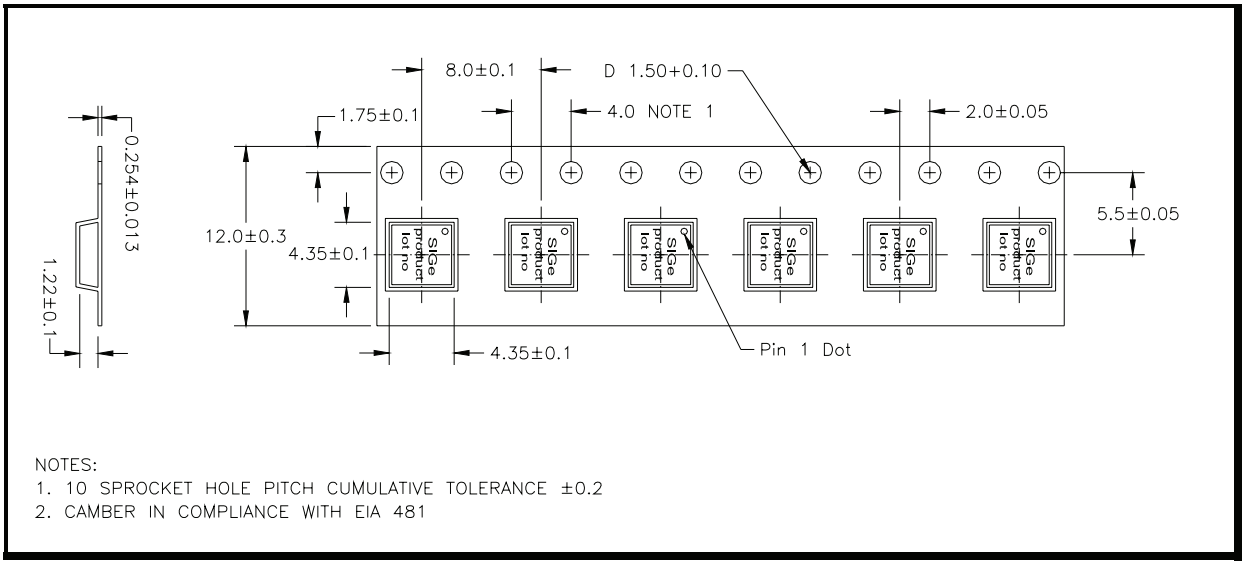
Profile Feature	SnPb Eutectic Assembly	Lead (Pb) Free Assembly
Average Ramp-up Rate (T_L to T_P)	3 °C / s (max)	3 °C / s (max)
Preheat		
Temperature Min. (T_{smin})	100 °C	150 °C
Temperature Max. (T_{smax})	150 °C	200 °C
Time (Min. to Max) (t_s)	60 - 120 s	60 - 80 s
Ramp Up		
Tsmax to t_L	-	3 °C / s (max)
Time 25°C to Peak Temperature	6 mins. (max)	8 mins. (max)
Reflow		
Temperature (t_L)	183 °C	217°C
Time maintained above t_L	60 - 150 s	60 - 150 s
Peak Temperature (t_p)	240 ±5 °C	260 +0/-5 °C
Time Within 5°C of Actual Peak Temperature (t_p)	10 - 30 s	20 - 40 s
Ramp-Down		
Ramp-Down Rate	6 °C / s (max)	6 °C / s (max)

Reflow Profile (Reference JEDEC J-STD-020)



Tape and Reel Information

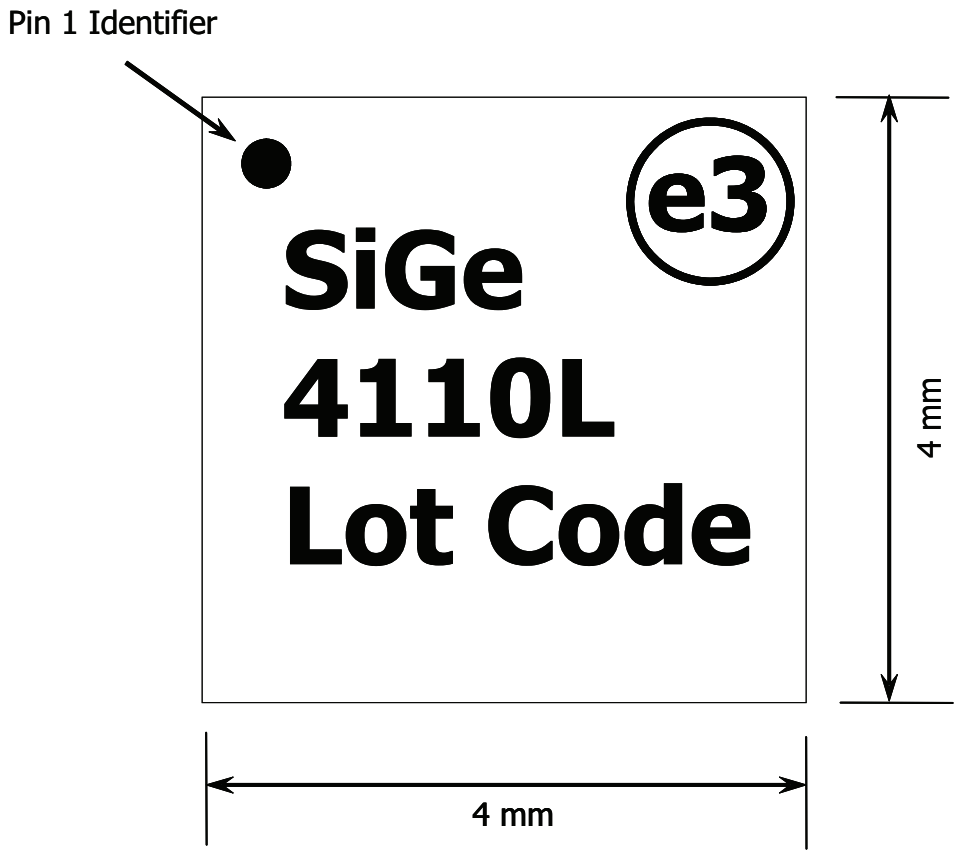
Parameter	Value
Devices Per Reel	3000
Reel Diameter	13 inches
Tape Width	12 millimeters



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481

Branding Information

SE4110L TOP MARK [4x4mm]



e3 = JEDEC Pb-free finish designation

This page intentionally left blank.

http://www.sige.com

Email: sales@sige.com

Customer Service Locations:

North America:
1050 Morrison Drive, Suite 100
Ottawa ON K2H 8K7 Canada

Phone: +1 613 820 9244
Fax: +1 613 820 4933

Hong Kong
Phone: +852 3428 7222
Fax: +852 3579 5450

San Diego
Phone: +1 858 668 3541 (ext. 226)
Fax: +1 858 668 3546

United Kingdom
Phone: +44 1279 464217
Fax: +44 1279 464201

Product Preview
The datasheet contains information from the product concept specification. SiGe Semiconductor, Inc. reserves the right to change information at any time without notification.

Preliminary Information
The datasheet contains information from the design target specification. SiGe Semiconductor, Inc. reserves the right to change information at any time without notification.

Production testing may not include testing of all parameters.