

MPS6521 (NPN) MPS6523 (PNP)

MPS6521 is a Preferred Device

Amplifier Transistors

Features

- Voltage and Current are Negative for PNP Transistors
- Pb-Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	NPN	PNP	Unit
Collector–Emitter Voltage MPS6521 MPS6523	V_{CEO}	25 –	– 25	Vdc
Collector–Base Voltage MPS6521 MPS6523	V_{CBO}	40 –	– 25	Vdc
Emitter–Base Voltage	V_{EBO}	4.0		Vdc
Collector Current – Continuous	I_C	100		mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	625 5.0		mW mW/°C
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	1.5 12		W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to–Ambient (Printed Circuit Board Mounting)	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction-to–Case	$R_{\theta JC}$	83.3	°C/W

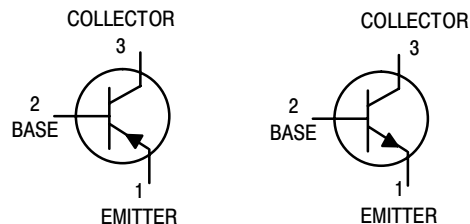
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

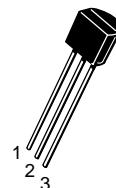


ON Semiconductor®

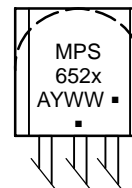
<http://onsemi.com>



MARKING DIAGRAM



TO-92
CASE 29-11
STYLE 1



MPS652x = Device Code
x = 1 or 3
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
MPS6521	TO-92	5000 Units/Box
MPS6521G	TO-92 (Pb-Free)	5000 Units/Box
MPS6521RLRA	TO-92	2000/Tape & Reel
MPS6521RLRAG	TO-92 (Pb-Free)	2000/Tape & Reel
MPS6523	TO-92	5000 Units/Box
MPS6523G	TO-92 (Pb-Free)	5000 Units/Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

MPS6521 (NPN) MPS6523 (PNP)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector – Emitter Breakdown Voltage (I _C = 0.5 mA _{dc} , I _B = 0)	V _{(BR)CEO}	25	–	V _{dc}
Emitter – Base Breakdown Voltage (I _E = 10 μA _{dc} , I _C = 0)	V _{(BR)EBO}	4.0	–	V _{dc}
Collector Cutoff Current (V _{CB} = 30 V _{dc} , I _E = 0) (V _{CB} = 20 V _{dc} , I _E = 0)	I _{CBO}	–	0.05	μA _{dc}
	MPS6521 MPS6523	–	0.05	
ON CHARACTERISTICS				
DC Current Gain (I _C = 100 μA _{dc} , V _{CE} = 10 V _{dc})	h _{FE}	150	–	–
	MPS6521	150	–	
(I _C = 2.0 mA _{dc} , V _{CE} = 10 V _{dc})	MPS6521	300	600	
(I _C = 100 μA _{dc} , V _{CE} = 10 V _{dc})	MPS6523	150	–	
(I _C = 2.0 mA _{dc} , V _{CE} = 10 V _{dc})	MPS6523	300	600	
Collector – Emitter Saturation Voltage (I _C = 50 mA _{dc} , I _B = 5.0 mA _{dc})	V _{CE(sat)}	–	0.5	V _{dc}
SMALL-SIGNAL CHARACTERISTICS				
Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0, f = 1.0 MHz)	C _{obo}	–	3.5	pF
Noise Figure (I _C = 10 μA _{dc} , V _{CE} = 5.0 V _{dc} , R _S = 10 k Ω, Power Bandwidth = 15.7 kHz, 3.0 dB points @ 10 Hz and 10 kHz)	NF	–	3.0	dB

NPN MPS6521 EQUIVALENT SWITCHING TIME TEST CIRCUITS

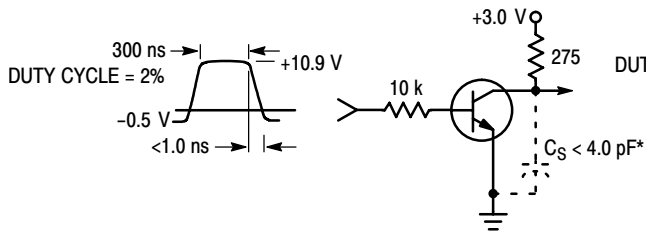


Figure 1. Turn-On Time

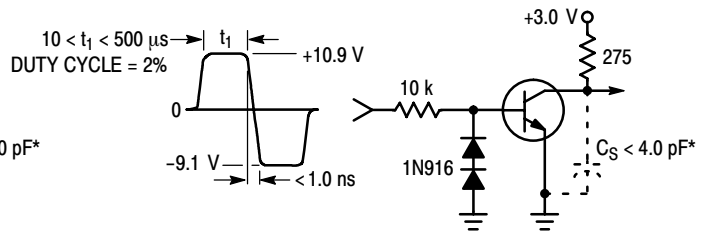


Figure 2. Turn-Off Time

*Total shunt capacitance of test jig and connectors

MPS6521 (NPN) MPS6523 (PNP)

TYPICAL NOISE CHARACTERISTICS

($V_{CE} = 5.0 \text{ Vdc}$, $T_A = 25^\circ\text{C}$)

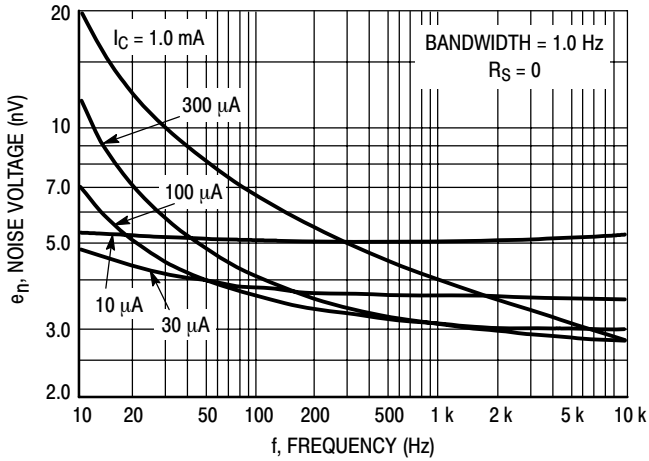


Figure 3. Noise Voltage

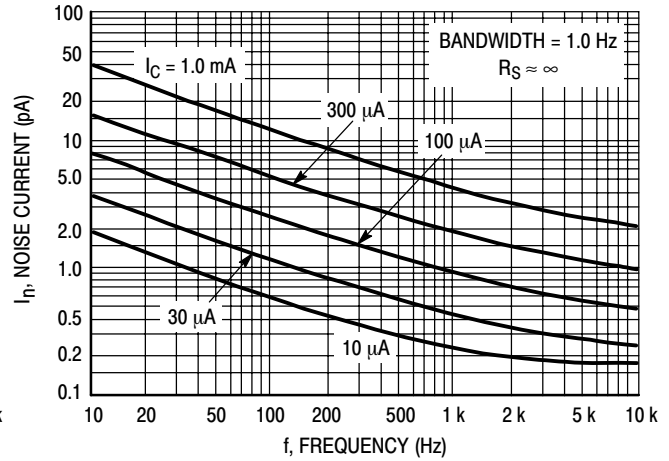


Figure 4. Noise Current

NPN MPS6521 NOISE FIGURE CONTOURS

($V_{CE} = 5.0 \text{ Vdc}$, $T_A = 25^\circ\text{C}$)

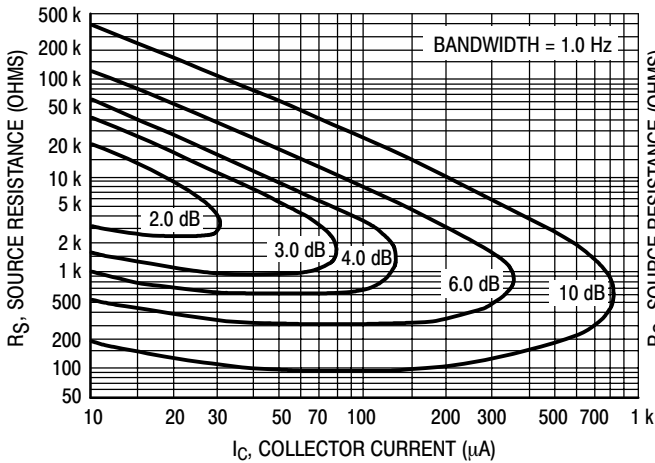


Figure 5. Narrow Band, 100 Hz

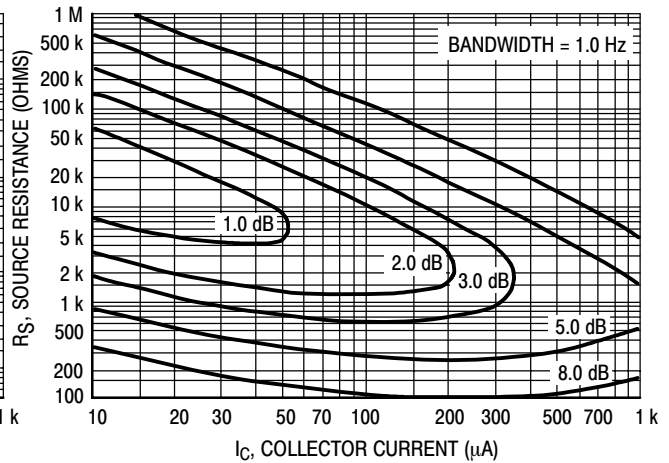


Figure 6. Narrow Band, 1.0 kHz

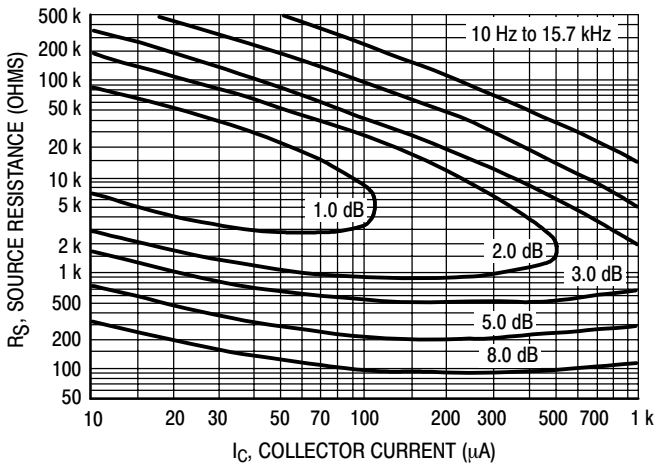


Figure 7. Wideband

Noise Figure is defined as:

$$NF = 20 \log_{10} \left(\frac{e_n^2 + 4KTR_S + I_n^2 R_S^2}{4KTR_S} \right)^{1/2}$$

e_n = Noise Voltage of the Transistor referred to the input. (Figure 3)

I_n = Noise Current of the Transistor referred to the input. (Figure 4)

K = Boltzman's Constant ($1.38 \times 10^{-23} \text{ J/}^\circ\text{K}$)

T = Temperature of the Source Resistance ($^\circ\text{K}$)

R_S = Source Resistance (Ohms)

MPS6521 (NPN) MPS6523 (PNP)

NPN
MPS6521
TYPICAL STATIC CHARACTERISTICS

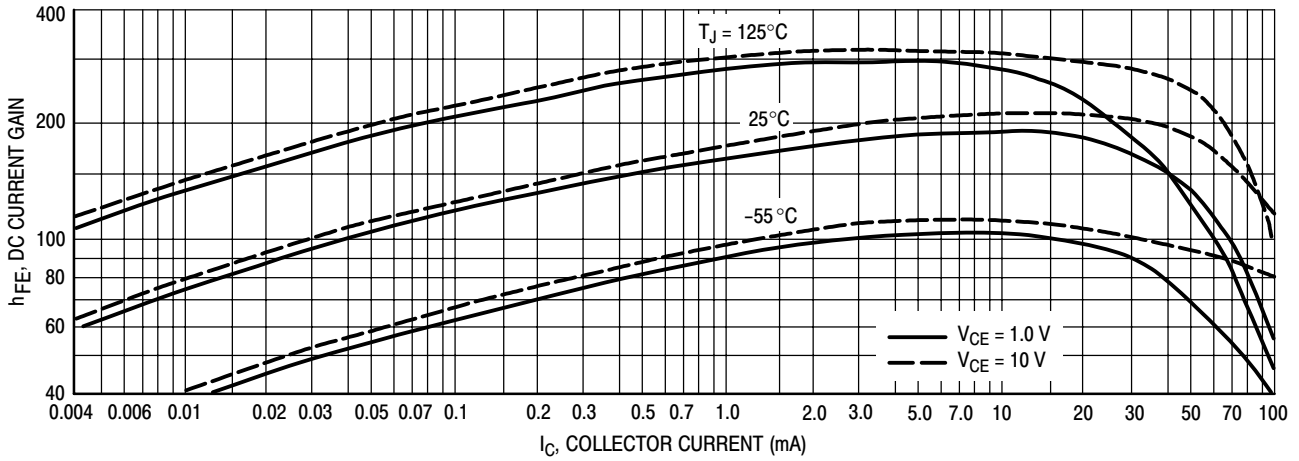


Figure 8. DC Current Gain

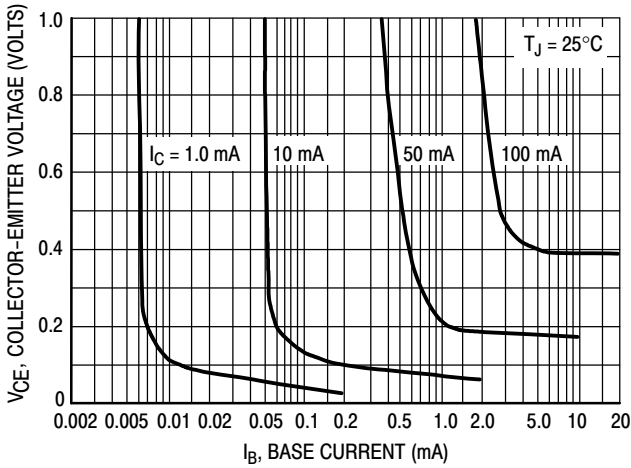


Figure 9. Collector Saturation Region

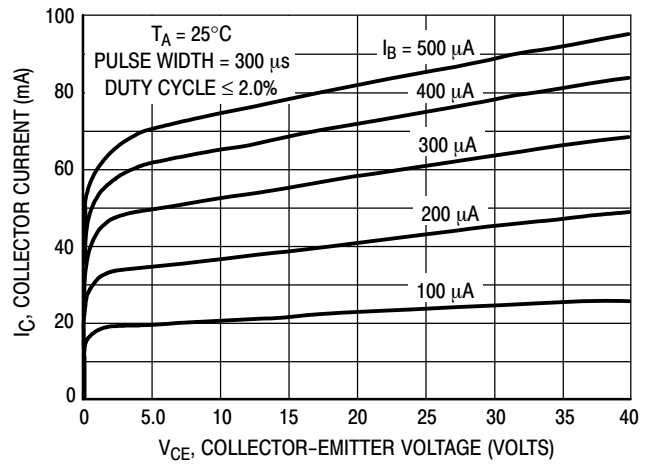


Figure 10. Collector Characteristics

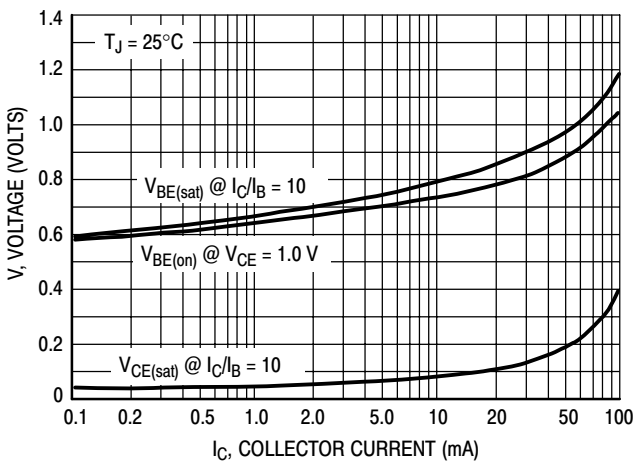


Figure 11. "On" Voltages

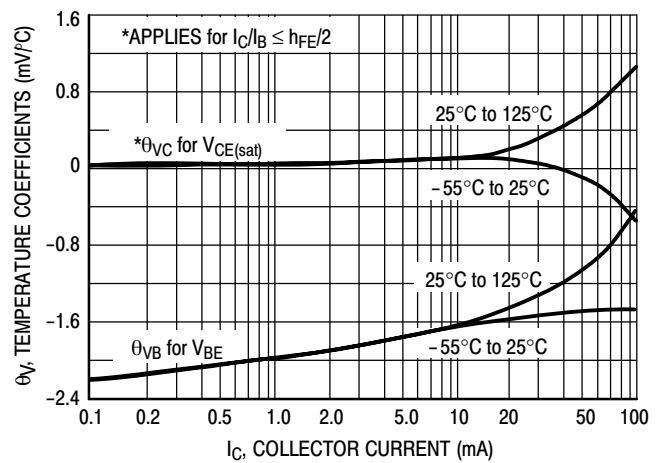


Figure 12. Temperature Coefficients

NPN

MPS6521

TYPICAL DYNAMIC CHARACTERISTICS

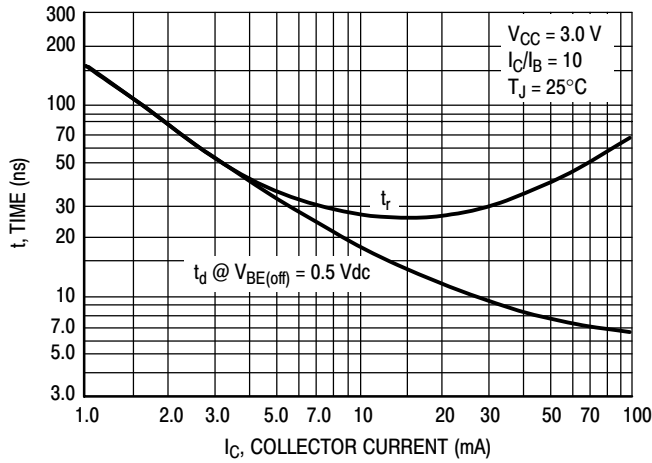


Figure 13. Turn-On Time

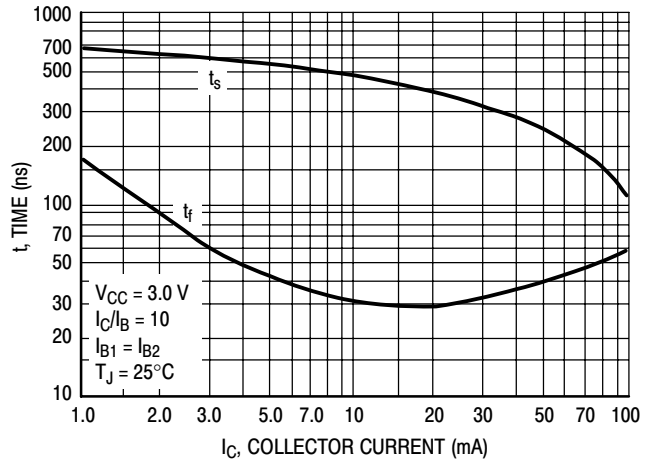


Figure 14. Turn-Off Time

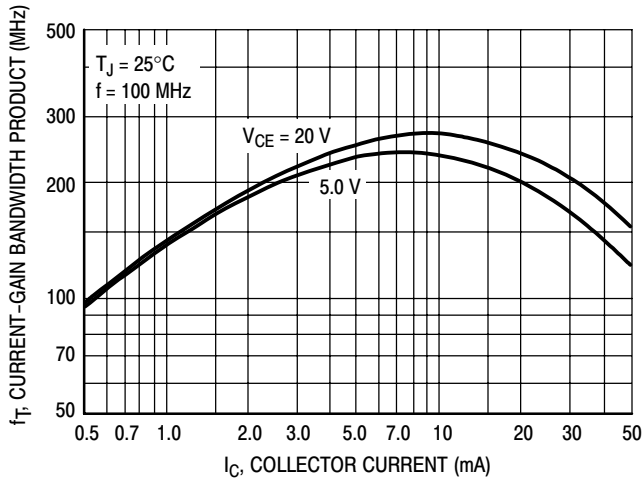


Figure 15. Current-Gain — Bandwidth Product

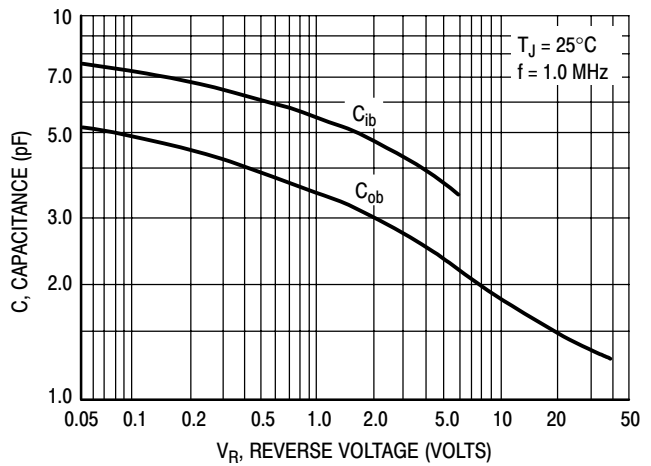


Figure 16. Capacitance

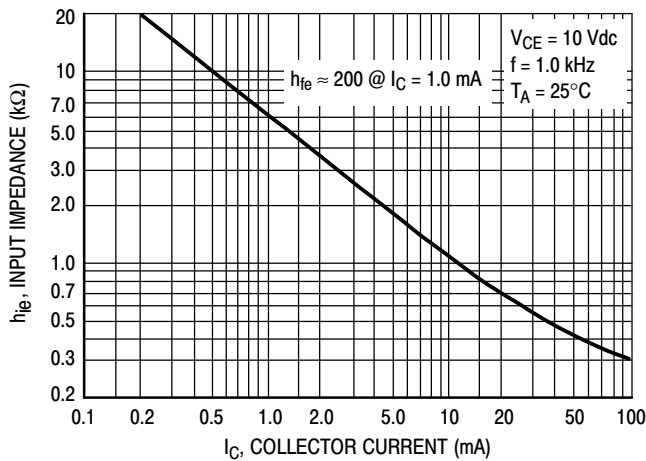


Figure 17. Input Impedance

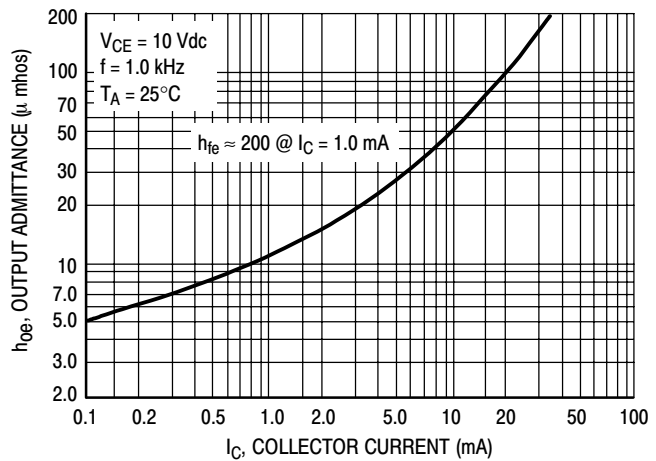


Figure 18. Output Admittance

NPN
MPS6521

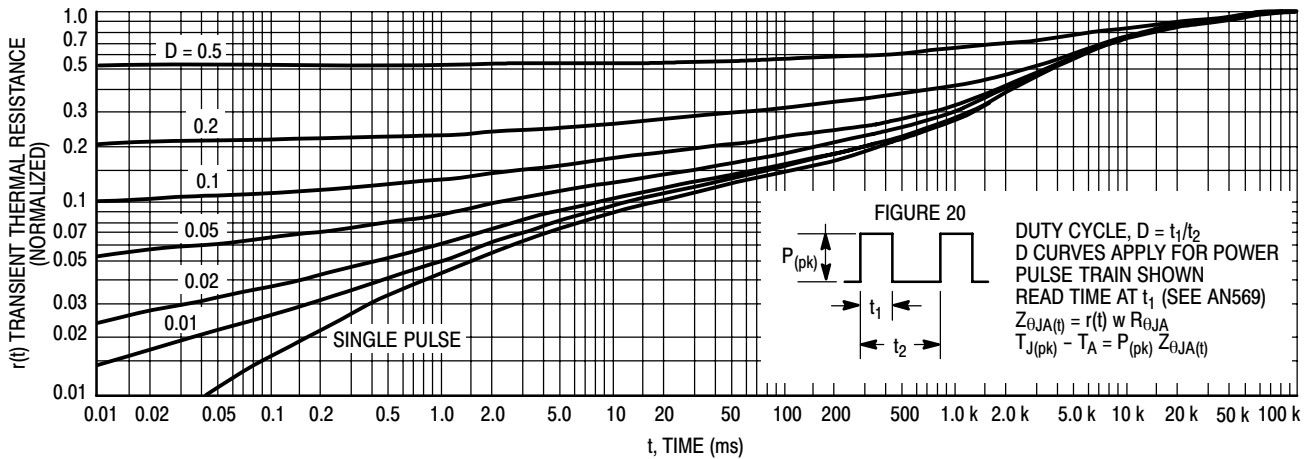


Figure 19. Thermal Response

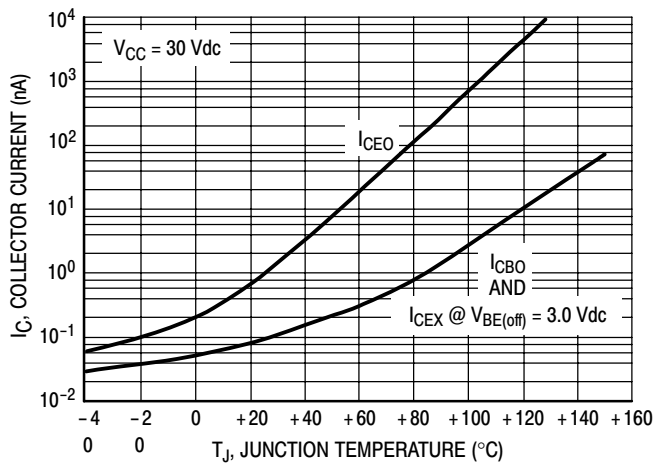


Figure 21.

DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 20. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 19 was calculated for various duty cycles.

To find $Z_{\theta JA(t)}$, multiply the value obtained from Figure 19 by the steady state value $R_{\theta JA}$.

Example:

The MPS6521 is dissipating 2.0 watts peak under the following conditions:

$$t_1 = 1.0 \text{ ms}, t_2 = 5.0 \text{ ms. (D = 0.2)}$$

Using Figure 19 at a pulse width of 1.0 ms and $D = 0.2$, the reading of $r(t)$ is 0.22.

The peak rise in junction temperature is therefore

$$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88^\circ\text{C}.$$

For more information, see ON Semiconductor Application Note AN569/D, available from the Literature Distribution Center or on our website at www.onsemi.com.

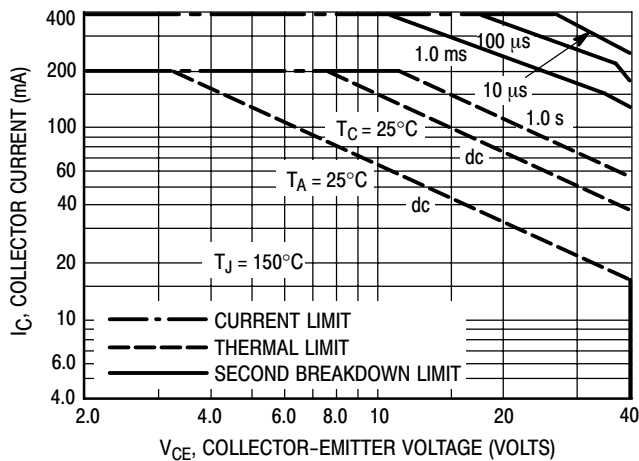


Figure 22.

The safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 22 is based upon $T_{J(pk)} = 150^\circ\text{C}$; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 19. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

PNP
MPS6523
TYPICAL NOISE CHARACTERISTICS

($V_{CE} = -5.0$ Vdc, $T_A = 25^\circ\text{C}$)

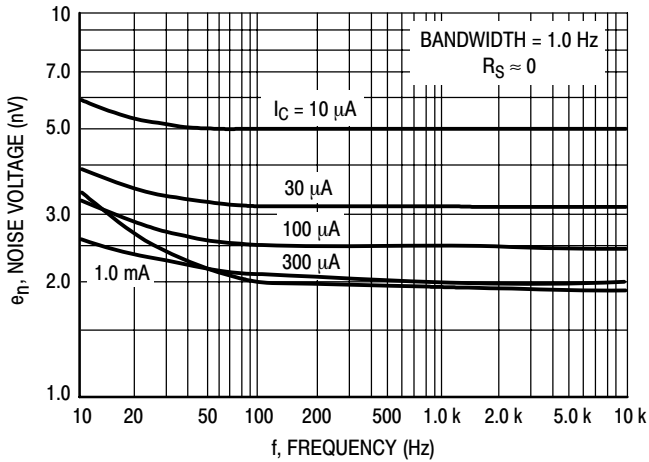


Figure 23. Noise Voltage

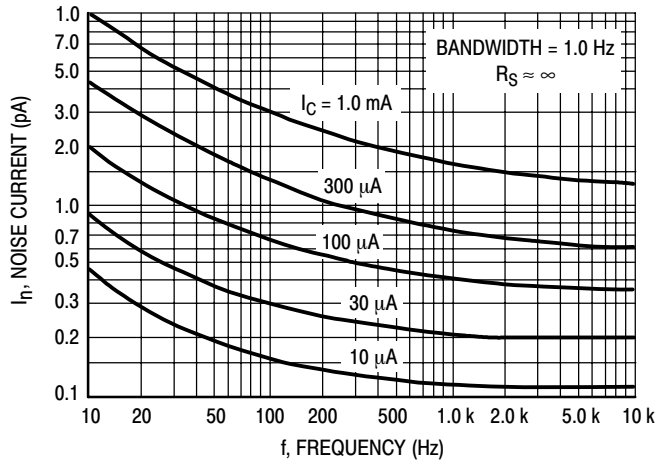


Figure 24. Noise Current

NOISE FIGURE CONTOURS

($V_{CE} = -5.0$ Vdc, $T_A = 25^\circ\text{C}$)

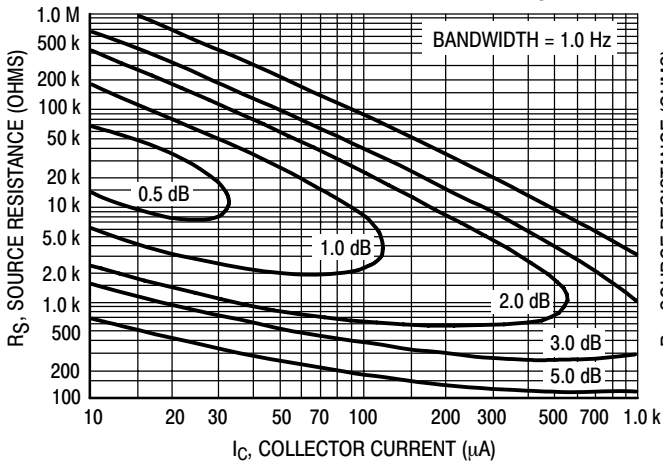


Figure 25. Narrow Band, 100 Hz

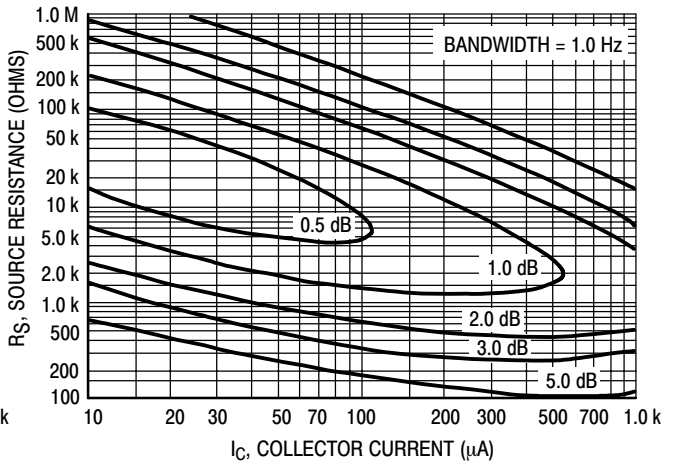


Figure 26. Narrow Band, 1.0 kHz

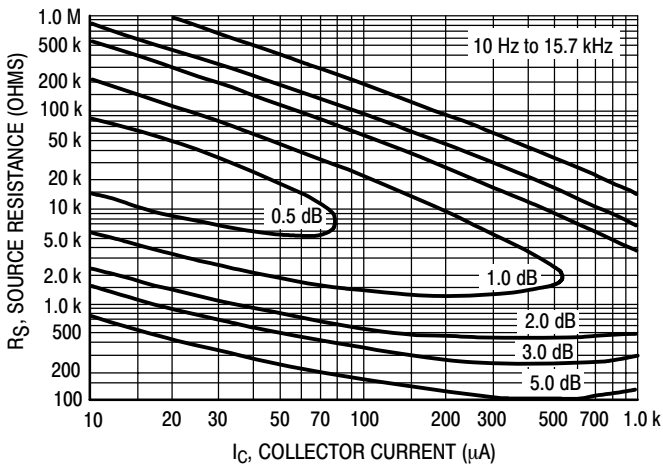


Figure 27. Wideband

Noise Figure is Defined as:

$$NF = 20 \log_{10} \left[\frac{e_n^2 + 4KTR_S + I_n^2 R_S^2}{4KTR_S} \right]^{1/2}$$

e_n = Noise Voltage of the Transistor referred to the input. (Figure 3)

I_n = Noise Current of the Transistor referred to the input. (Figure 4)

K = Boltzman's Constant (1.38×10^{-23} J/°K)

T = Temperature of the Source Resistance (°K)

R_S = Source Resistance (Ohms)

MPS6521 (NPN) MPS6523 (PNP)

PNP
MPS6523
TYPICAL STATIC CHARACTERISTICS

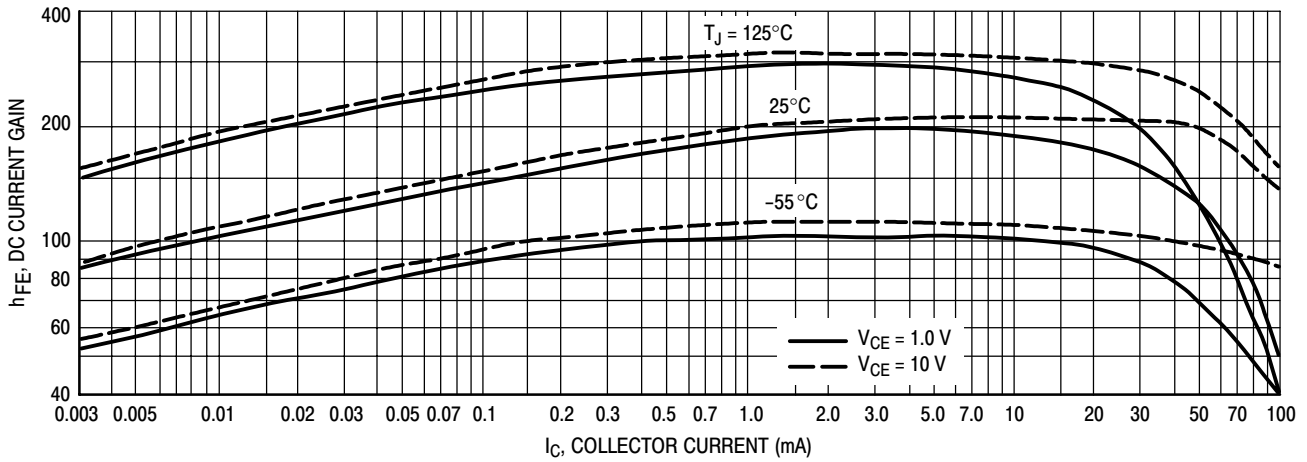


Figure 28. DC Current Gain

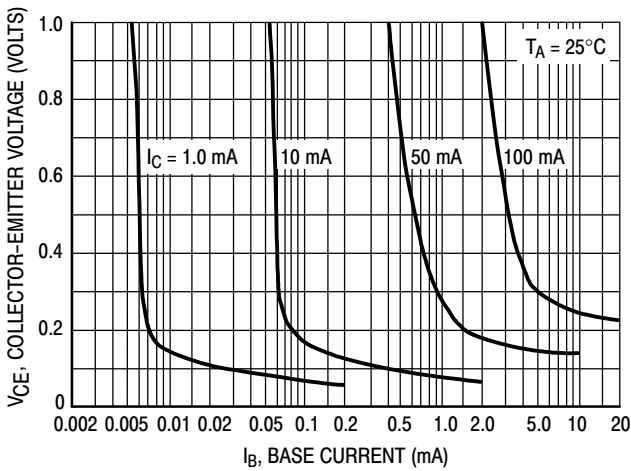


Figure 29. Collector Saturation Region

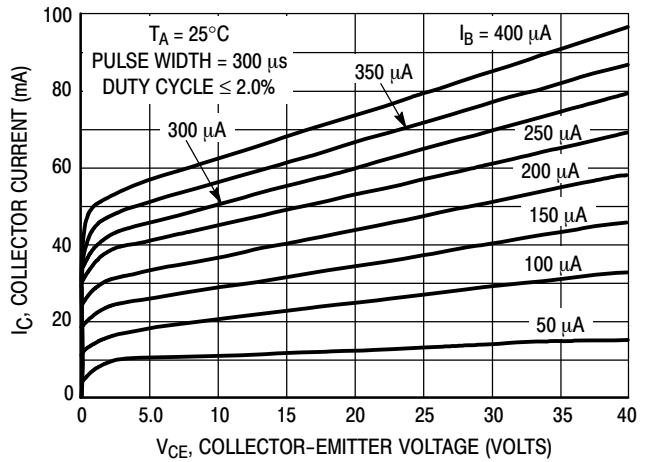


Figure 30. Collector Characteristics

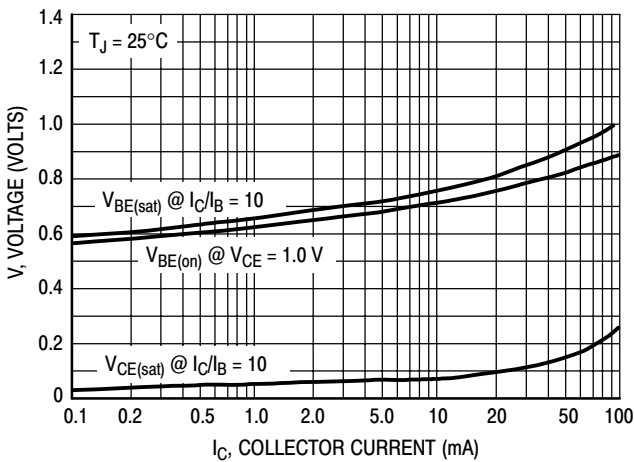


Figure 31. "On" Voltages

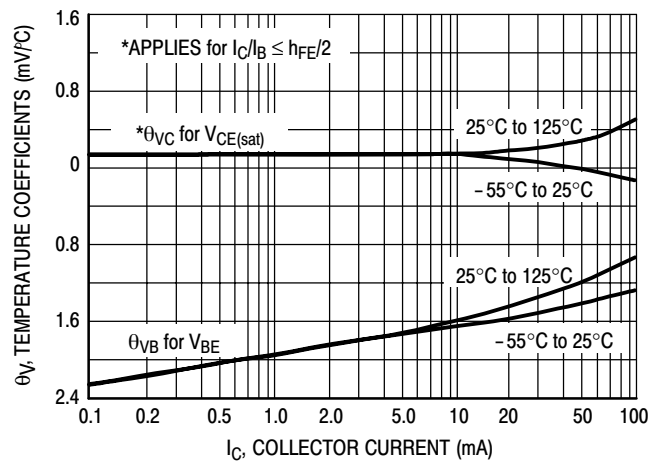


Figure 32. Temperature Coefficients

MPS6521 (NPN) MPS6523 (PNP)

PNP
MPS6523
TYPICAL DYNAMIC CHARACTERISTICS

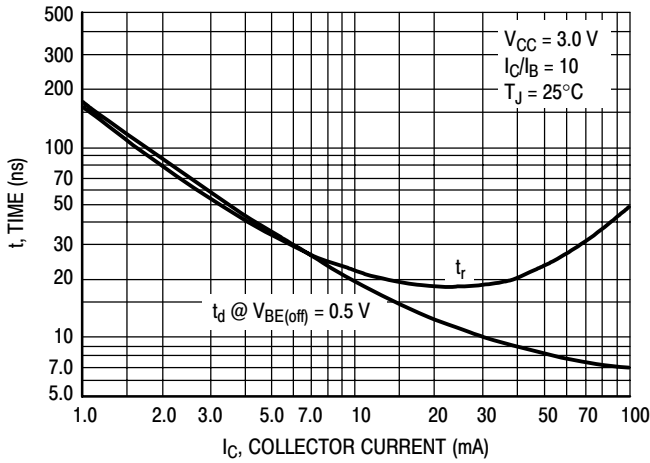


Figure 33. Turn-On Time

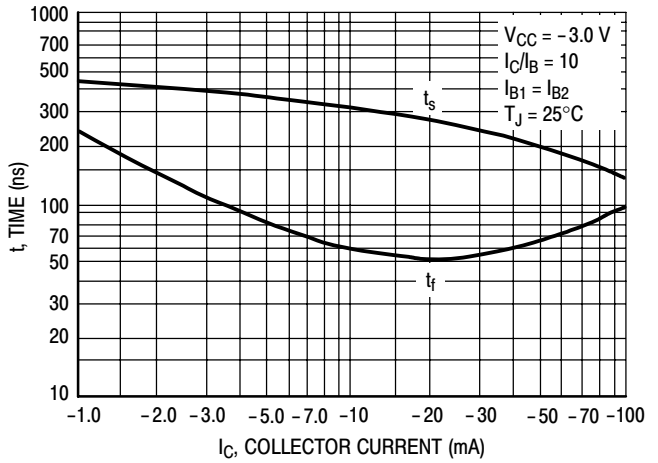


Figure 34. Turn-Off Time

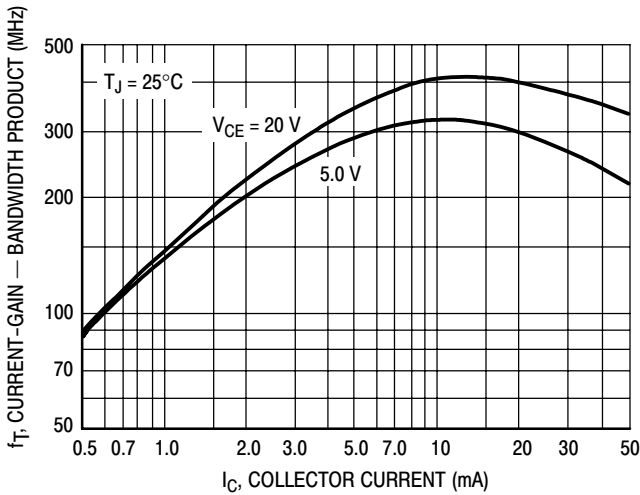


Figure 35. Current-Gain — Bandwidth Product

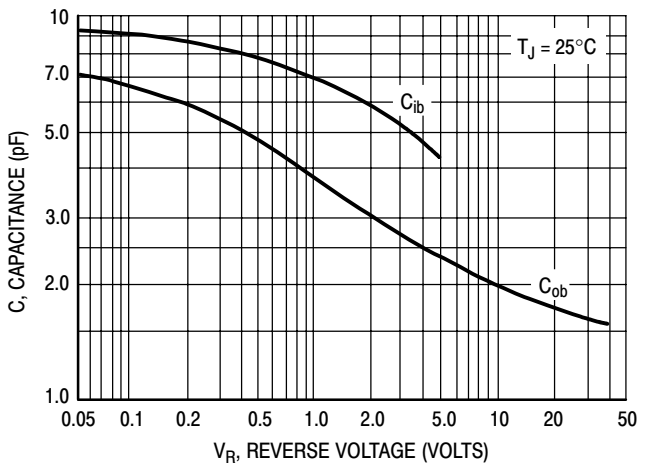


Figure 36. Capacitance

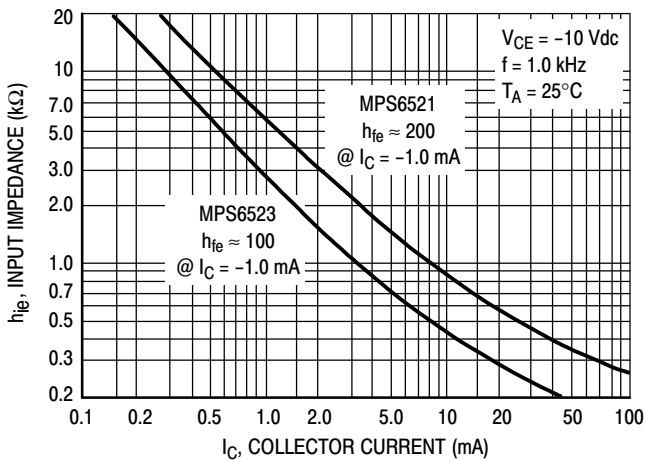


Figure 37. Input Impedance

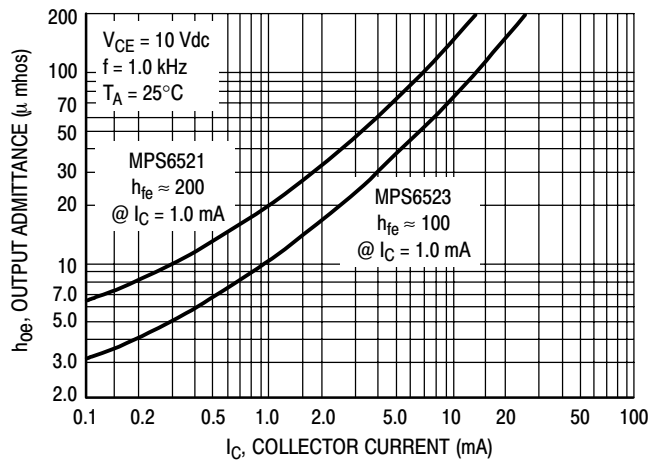


Figure 38. Output Admittance

PNP
MPS6523

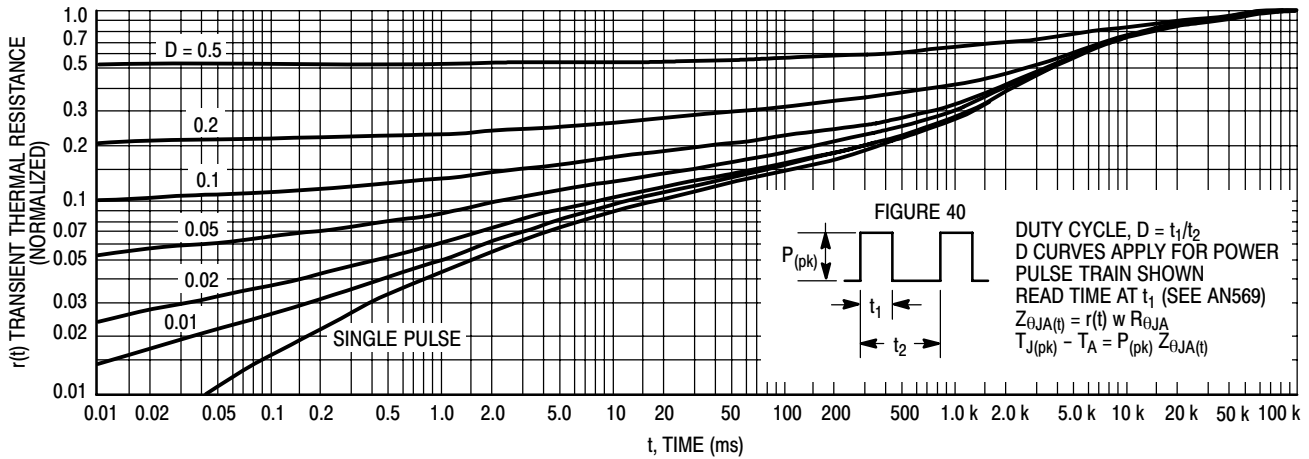


Figure 39. Thermal Response

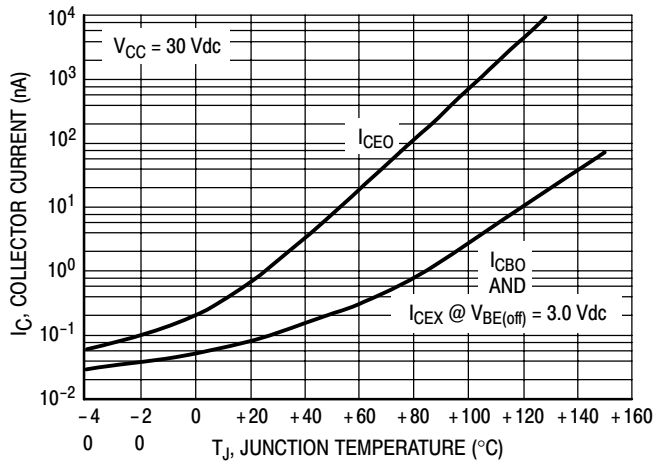


Figure 41.

DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 40. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 39 was calculated for various duty cycles.

To find $Z_{\theta JA(t)}$, multiply the value obtained from Figure 39 by the steady state value $R_{\theta JA}$.

Example:

The MPS6523 is dissipating 2.0 watts peak under the following conditions:

$$t_1 = 1.0 \text{ ms}, t_2 = 5.0 \text{ ms. (D = 0.2)}$$

Using Figure 39 at a pulse width of 1.0 ms and $D = 0.2$, the reading of $r(t)$ is 0.22.

The peak rise in junction temperature is therefore

$$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88^\circ\text{C}.$$

For more information, see ON Semiconductor Application Note AN569/D, available from the Literature Distribution Center or on our website at www.onsemi.com.

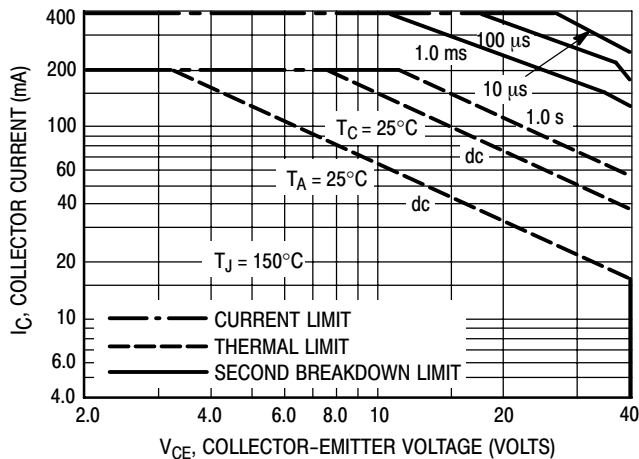


Figure 42.

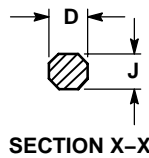
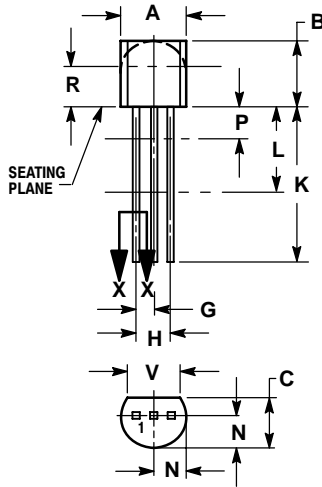
The safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 42 is based upon $T_{J(pk)} = 150^\circ\text{C}$; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 39. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MPS6521 (NPN) MPS6523 (PNP)

PACKAGE DIMENSIONS

TO-92 (TO-226)
CASE 29-11
ISSUE AL



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

STYLE 1:

1. PIN 1. EMITTER
2. BASE
3. COLLECTOR

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your
local Sales Representative.