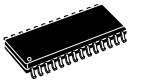
STA320

2.1 MULTICHANNELS DIGITAL AUDIO PROCESSOR WITH DDX™

1 FEATURES

- 2.1 Channels of 24-bit DDX™
- >100dB SNR and Dynamic Range
- Selectable 32kHz-192kHz Input Sample Rates
- I^2C control with Selectable Device Address
- Digital Gain/Attenuation +48dB to -90dB in 0.5dB steps
- Soft Volume Update
- Individual Channel and Master Gain/ Attenuation
- Dual Independent Limiters/Compressors
- Dynamic Range Compression or Anti-Clipping Modes
- AutoModes™:
  - 7 Preset Crossover filters
  - 32 Preset EQ Settings
  - Auto Volume Controlled Loudness
  - 3 Preset Volume Curves
  - 2 Preset Anti-Clipping Modes
  - Preset Nighttime Listening Mode
  - Preset TV AGC
- Individual Channel and Master Soft and Hard Mute
- Independent Channel Volume and DSP Bypass
- Automatic Zero-Detect Mute
- Automatic Invalid Input Detect Mute
- 2-Channel I^2S Input Data Interface
- Input and Output Channel Mapping
- 4 28-bit User Programmable Biquads (EQ) per channel
- Bass/Treble Tone Control
- DC Blocking Selectable High-Pass Filter
- Selectable De-emphasis

Figure 1. Package



SO28

Table 1. Order Code

Part Number	Package
STA320	SO28

- Post-EQ User Programmable Mix
- User Programmable 2.1 Bass Management
- Sub Channel Mix into Left and Right Channels
- Advanced AM Interference Frequency Switching and Noise Suppression Modes
- Selectable High or Low Bandwidth Noise Shaping Topologies
- Variable Max Power Correction for lower full-power THD
- 3 or 4 Output Routing Configurations
- Selectable Clock Input Ratio
- 96kHz Internal Processing Sample Rate, 24 to 28-bit precision

2 DESCRIPTION

The STA320 is a single chip solution for digital audio processing and control in 2.1-channel applications. It provides output capabilities for DDX™ (Direct Digital Amplification). In conjunction with a DDX™ power device, it provides high-quality, high-efficiency, all digital amplification.

Figure 2. PIN CONNECTION (Top view)

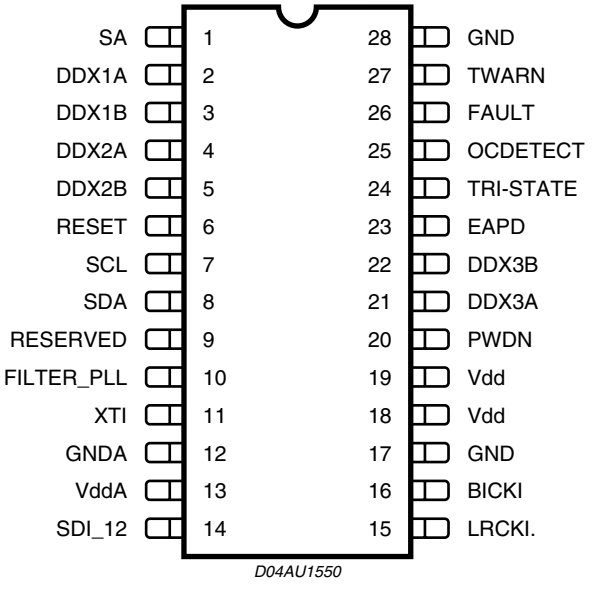


Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	3.3V I/O Power Supply	-0.5 to 4	V
V_{DDA}	3.3V Logic Power Supply	-0.5 to 4	V
V_i	Voltage on input pins	-0.5 to (VDD+0.5)	V
V_o	Voltage on output pins	-0.5 to (VDD+0.3)	V
T_{stg}	Storage Temperature	-40 to +150	°C
T_{amb}	Ambient Operating Temperature	-20 to +85	°C

Table 3. THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$	Thermal resistance Junction to Ambient	85	°C/W

Table 4. RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	I/O Power Supply	3.0 to 3.6	V
V_{DDA}	Logic Power Supply	3.0 to 3.6	V
T_j	Operating Junction Temperature	-20 to +125	°C

Table 5. PIN FUNCTION

Pin N`	Name	Type	Description	Pad Type
1	SA	I	I²C Address selector	CMOS Input Buffer with Pull-Down
2	DDX1A	O	Channel 1 DDX Output A	3.3V Capable TTL 4mA Output Buffer
3	DDX1B	O	Channel 1 DDX Output B	3.3V Capable TTL 4mA Output Buffer
4	DDX2A	O	Channel 2 DDX Output A	3.3V Capable TTL 4mA Output Buffer
5	DDX2B	O	Channel 2 DDX Output B	3.3V Capable TTL 4mA Output Buffer
6	RESET	I	Global reset (active low)	5V Tolerant TTL Schmitt Trigger Input Buffer
7	SCL	I	I²C Serial Clock	5V Tolerant TTL Schmitt Trigger Input Buffer
8	SDA	I/O	I²C Serial Data	Bidirectional Buffer: 5V Tolerant TTL Schmitt Trigger Input; 3.3V Capable 2mA Slew-rate controlled Output.
9	RESERVED	--	Test pin to be externally connected to Ground	
10	FILTER_PLL	I	Connection to PLL_filter	Analog Pad
11	XTI	I	PLL Input clock	5V Tolerant TTL Schmitt Trigger Input Buffer
12	GNDA		Analog Ground	Analog Ground
13	VddA		3.3V Analog Power Supply Voltage	3.3V Analog Power Supply Voltage
14	SDI_12	I	I²S Serial Data Channels 1 & 2	5V Tolerant TTL Input Buffer
15	LRCKI	I	I²S Left/Right Clock	5V Tolerant TTL Input Buffer
16	BICKI	I	I²S Serial Clock	5V Tolerant TTL Input Buffer
17	GND	I/O	Digital Ground	Digital Ground
18	Vdd	I/O	3.3V Digital Power Supply Voltage	3.3V Digital Power Supply Voltage
19	Vdd	I/O	3.3V Digital Power Supply Voltage	3.3V Digital Power Supply Voltage
20	PWDN	I	Device Powerdown	5V Tolerant TTL Schmitt Trigger Input Buffer
21	DDX3A	O	Channel 3 DDX Output A	3.3V Capable TTL 4mA Output Buffer
22	DDX3B	O	Channel 3 DDX Output B	3.3V Capable TTL 4mA Output Buffer
23	EAPD	O	External Amp Power Down	3.3V Capable TTL 4mA Output Buffer
24	TRI-STATE	O	Tri-state output to Power block	3.3V Capable TTL 4mA Output Buffer
25	OCDETECT	I	Over-current Indicator	5V Tolerant TTL Input Buffer
26	FAULT	I	Power Fault Indicator	5V Tolerant TTL Input Buffer
27	TWARN	I	Thermal Warning Indicator	5V Tolerant TTL Input Buffer
28	GND	I/O	Digital Ground	Digital Ground

3 ELECTRICAL CHARACTERISTCS (V_{DD3} = 3.3V ± 0.3V; V_{DDA} = 3.3V ± 0.3V; T_{AMB} = 0 TO 70 °C; UNLESS OTHERWISE SPECIFIED)

Table 6. GENERAL INTERFACE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
I_{il}	Low Level Input no pull-up	V_i = 0V			1	µA	1
I_{ih}	High Level Input no pull-down	$V_i = V_{DD3}$			2	µA	1
I_{OZ}	Tristate output leakage without pullup/down	$V_i = V_{DD3}$			2	µA	1
V_{esd}	Electrostatic Protection	Leakage < 1µA	2000			V	2

Note 1: The leakage currents are generally very small, < 1na. The values given here are maximum after an electrostatic stress on the pin.
Note 2: Human Body Model

Table 7. DC ELECTRICAL CHARACTERISTICS: 3.3V BUFFERS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{ILhyst}	Low Level Threshold	Input Falling	0.8		1.35	V
V_{IHhyst}	High Level Threshold	Input Rising	1.3		2.0	V
V_{hyst}	Schmitt Trigger Hysteresis		0.3		0.8	V
V_{ol}	Low Level Output	Iol = 100uA			0.2	V
V_{oh}	High Level Output	Ioh = -100uA Ioh = -2mA	VDD3-0.2 2.4			V V

4 I^2C BUS SPECIFICATION

The STA320 supports the I^2C protocol via the input ports SCL and SDA_IN (Master to Slave) and the output port SDA_OUT (Slave to Master).

This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver.

The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA320 is always a slave device in all of its communications. It supported up to 400KB/sec rate (fast-mode bit rate).

4.1 COMMUNICATION PROTOCOL

4.1.1 Data Transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition.

4.1.2 Start Condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

4.1.3 Stop Condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state.

A STOP condition terminates communication between STA320 and the bus master.

4.1.4 Data Input

During the data input the STA320 samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

4.2 DEVICE ADDRESSING

To start communication between the master and the STA320, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8-bits (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I^2C bus definition. In the STA320 the I^2C interface has two device addresses depending on the SA port configuration, 0x34 when SA = 0, and 0x36 when SA = 1.

The 8^{th} bit (LSB) identifies read or write operation RW, this bit is set to 1 in read mode and 0 for write mode and 0 for write mode. After a START condition the STA320 identifies on the bus the device address and if a match is found, it acknowledges the identification on SDA bus during the 9^{th} bit time. The byte following the device identification byte is the internal space address.

4.3 WRITE OPERATION

Following the START condition the master sends a device select code with the RW bit set to 0.

The STA320 acknowledges this and the writes for the byte of internal address.

After receiving the internal byte address the STA320 again responds with an acknowledgement.

4.3.1 Byte Write

In the byte write mode the master sends one data byte, this is acknowledged by the STa320. The master then terminates the transfer by generating a STOP condition.

4.3.2 Multi-byte Write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

Figure 3. Write Mode Sequence

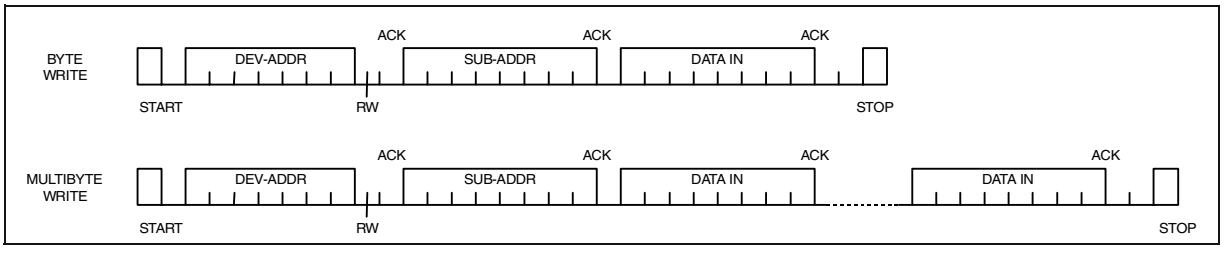
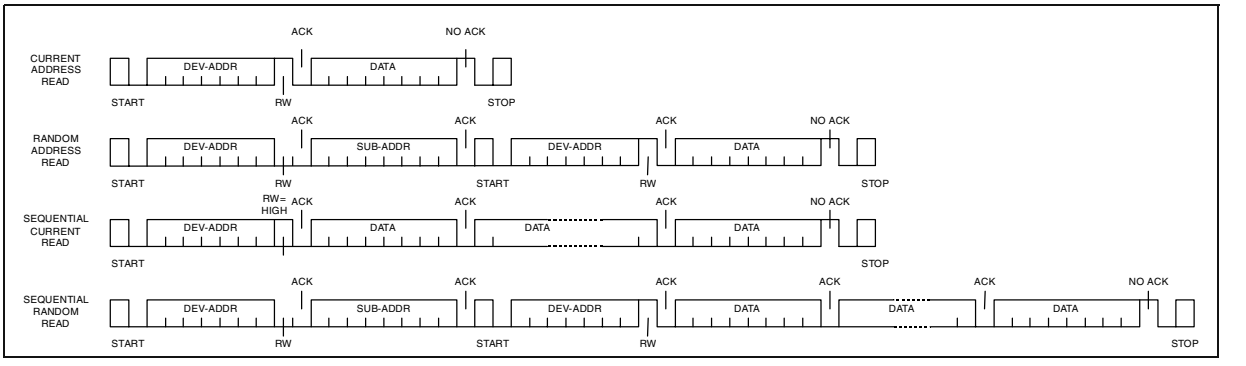


Figure 4. Read Mode Sequence



5 REGISTER SUMMARY

Table 8. Register Summary

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	**ConfA**	FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0x01	**ConfB**	C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
0x02	**ConfC**	OCRB	CSZ4	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
0x03	**ConfD**	MME	ZDE	DRC	BQL	PSL	DSPB	DEMP	HPB
0x04	**ConfE**	SVE	ZCE	DCCV	PWMS	AME	NSBW	MPC	MPCV
0x05	**ConfF**	EAPD	PWDN	ECLE	LDTE	BCLE	IDE	OCFG1	OCFG0
0x06	**Mute**	QFILT	QXEN		TFRB	C3M	C2M	C1M	MMute
0x07	**Mvol**	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
0x08	**C1Vol**	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0x09	**C2Vol**	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0x0A	**C3Vol**	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0x0B	**Auto1**	AMPS		AMGC1	AMGC0	AMV1	AMV0	AMEQ1	AMEQ0
0x0C	**Auto2**	XO3	XO2	XO1	XO0	AMAM2	AMAM1	AMAM0	AMAME
0x0D	**Auto3**				PEQ4	PEQ3	PEQ2	PEQ1	PEQ0
0x0E	**C1Cfg**	C1OM1	C1OM0	C1LS1	C1LS0	C1BO	C1VBP	C1EQBP	C1TCB
0x0F	**C2Cfg**	C2OM1	C2OM0	C2LS1	C2LS0	C2BO	C2VBP	C2EQBP	C2TCB
0x10	**C3Cfg**	C3OM1	C3OM0	C3LS1	C3LS0	C3BO	C3VBP		
0x11	**Tone**	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0x12	**L1ar**	L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0x13	**L1atrt**	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0x14	**L2ar**	L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0x15	**L2atrt**	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0x16	**Cfaddr**			CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0x17	**B1cf1**	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0x18	**B1cf2**	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0x19	**B1cf3**	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0x1A	**B2cf1**	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0x1B	**B2cf2**	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8

Table 8. Register Summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x1C	**B2cf3**	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0x1D	**A1cf1**	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16
0x1E	**A1cf2**	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0x1F	**A1cf3**	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0x20	**A2cf1**	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0x21	**A2cf2**	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0x22	**A2cf3**	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0x23	**B0cf1**	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0x24	**B0cf2**	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0x25	**B0cf3**	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0x26	**Cfud**					RA	R1	WA	W1
0x27	**MPCC1**	MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0x28	**MPCC2**	MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
0x29	**DCC1**	DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
0x2A	**DCC2**	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0
0x2B	**FDRC1**	FDRC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
0x2C	**FDRC2**	FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
0x2D	**Status**	PLLUL				OCWARN	TFAULT	FAULT	TWARN
0x2E	**BC0**	RES	RES	RES	RES	RES	RES	RES	RES
0x2F	**BS0**	RES	RES	RES	RES	RES	RES	BS9	BS8
0x30	**BS1**	RES	RES	RES	RES	RES	RES	RES	RES
0x31	**B1**	RES	RES	RES	RES	RES	RES	RES	RES
0x32	**B2**	RES	RES	RES	RES	RES	RES	RES	RES
0x33	**T**	RES	RES	RES	RES	RES	RES	RES	RES

5.1 Configuration Register A (address 00h)

D7	D6	D5	D4	D3	D2	D1	D0
FDRB	TWAB	TFRB	IR1	IR0	MCS2	MCS1	MCS0
0	1	1	0	0	0	1	1

5.1.1 Master Clock Select

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	1	MCS0	Master Clock Select : Selects the ratio between the input I^2S sample frequency and the input clock.
1	R/W	1	MCS1	
2	R/W	0	MCS2	

The STA320 will support sample rates of 32kHz, 44.1kHz, 48Khz, 88.2kHz, 96kHz, Therefore the internal clock will be:

- 32.768Mhz for 32kHz
- 45.1584Mhz for 44.1khz, 88.2kHz and 176.4kHz
- 49.152Mhz for 48kHz, 96kHz, and 192kHz

The external clock frequency provided to the XTI pin must be a multiple of the input sample frequency(fs). The relationship between the input clock and the input sample rate is determined by both the MCSx and the IR (Input Rate) register bits. The MCSx bits determine the PLL factor generating the internal clock and the IR bit determine the oversampling ratio used internally.

Table 9.

Input Sample Rate *fs* (kHz)	IR	MCS(2..0)					
		000	001	010	011	100	101
32, 44.1, 48	00	768fs	512fs	384fs	256fs	128fs	576fs
88.2, 96	01	384fs	256fs	192fs	128fs	64fs	x
176.4, 192	1X	384fs	256fs	192fs	128fs	64fs	x

5.1.2 Interpolation Ratio Select

BIT	R/W	RST	NAME	DESCRIPTION
4..3	R/W	00	IR(1..0)	Interpolation Ratio Select: Selects internal interpolation ratio based on input I^2S sample frequency

The STA320 has variable interpolation (oversampling) settings such that internal processing and DDX output rates remain consistent. The first processing block interpolates by either 2 times or 1 time (pass-through). or provides a 2 times downsample.

The IR bits determine the oversampling ratio of this interpolation.
IR bit settings as a function of Input Sample Rate

Table 10.

Input Sample Rate *Fs* (kHz)	IR(1,0)	1st Stage Interpolation Ratio
32	00	2 times oversampling
44.1	00	2 times oversampling
48	00	2 times oversampling
88.2	01	Pass-Through
96	01	Pass-Through
176.4	10	2 times oversampling
192	10	2 times oversampling

Example: IR = 00, MCS = 011 (Default value):

XTI = 256 x fs = 8.192MHz (fs=32KHz) or 11.2896MHz (fs=44.1KHz) or 12.288MHz (fs=48KHz)

5.1.3 Thermal Warning Recovery Bypass

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	1	TWRB	Thermal-Warning Recovery Bypass: 0 - Thermal warning Recovery enabled 1 - Thermal warning Recovery disabled

If the Thermal Warning Adjustment is enabled (TWAB=0), then the Thermal Warning Recovery will determine if the -3dB adjustment is removed when Thermal Warning is negative. If TWRB=0 and TWAB=0, then when a thermal warning disappears the -3dB adjustment will be removed and the gain will be added back to the system.

If TWRB=1 and TWAB=0, then when a thermal warning disappears the -3dB adjustment will remain until TWRB is changed to zero or the device is reset.

5.1.4 Thermal Warning Adjustable Bypass

BIT	R/W	RST	NAME	DESCRIPTION
6	R/W	1	TWAB	Thermal-Warning Recovery Bypass: 0 - Thermal warning Recovery enabled 1 - Thermal warning Recovery disabled

The on-chip STA320 Power Output block provides feedback to the digital controller using inputs to the Power Control block. The TWARN input is used to indicate a thermal warning condition.

When TWARN is asserted (set to 0) for a period of time greater than 400ms, the power control block will force a -3dB adjustment to the modulation limit in an attempt to eliminate the thermal warning condition. Once the thermal warning volume adjustment is applied, it remains in this state until reset.

5.1.5 hermal Warning Adjustable Bypass

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	FDRB	Fault -Detector Recovery Bypass: 0 - Fault Detector Recovery enabled 1 - Fault Detector Recovery disabled

The on-chip STA320 Power Output block provides feedback to the digital controller using inputs to the Power Control block. The FAULT input is used to indicate a fault condition (either over-current or thermal). When FAULT is asserted (set to 0), the power control block will attempt a recovery from the fault by asserting the tri-state output (setting it to 0 which directs the power output block to begin recovery), hold it at 0 for period of time in the range of .1ms to 1 second as defined by the Fault-Detect Recovery Constant register (FDRC registers 29-2Ah), then toggle it back to 1. This sequence is repeated as log as the fault indication exists. This feature is enabled by default but can be bypassed by setting the FDRB control bit to 1.

5.2 Configuration Register B(Address 01h)

D7	D6	D5	D4	D3	D2	D1	D0
C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
1	0	0	0	0	0	0	0

5.2.1 Serial Data Interface Format

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	SAI0	Serial Audio Input Interface Format: Determines the interface format of the input serial digital audio interface.
1	R/W	0	SAI1	
2	R/W	0	SAI2	
3	R/W	0	SAI3	

5.2.2 Serial Data Interface

The STA320 audio serial input was designed to interface with standard digital audio components and to accept a number of serial data formats. STA320 always acts a slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using 3 inputs: left/right clock LRCKI, serial clock BICKI, and serial data 1 & 2 SDI12.

The SAI register (Configuration Register B - 01h, Bits D3-D0) and the SAIFB register (Configuration Register B - 01h, Bit D4) are used to specify the serial data format. The default serial data format is I2S, MSB-First. Available formats are shown in the tables and figure that follow.

Table 11. Serial Data First Bit

SAIFB	Format
0	MSB-First
1	LSB-First

For example, SAI=1110 and SAIFB=1 would specify Right-Justified 16-bit data, LSB-First.

Table 4 below lists the serial audio input formats supported by STA320 as related to BICKI = 32/48/64fs, where sampling rate fs = 32/44.1/48/88.2/96kHz.

Table 12. Supported Serial Audio Input Formats

BICKI	SAI (3...0)	SAIFB	Interface Format
32fs	1100	X	I^2S 15bit Data
	1110	X	Left/Right-Justified 16bit Data
48fs	0100	X	I^2S 23bit Data
	0100	X	I^2S 20bit Data
	1000	X	I^2S 18bit Data
	0100	0	MSB First I^2S 16bit Data
	1100	1	LSB First I^2S 16bit Data
	0001	X	Left-Justified 24bit Data
	0101	X	Left-Justified 20bit Data
	1001	X	Left-Justified 18bit Data
	1101	X	Left-Justified 16bit Data
	0010	X	Right-Justified 24bit Data
	0110	X	Right-Justified 20bit Data
	1010	X	Right-Justified 18bit Data
	1110	X	Right-Justified 16bit Data
64fs	0000	X	I^2S 24bit Data
	0100	X	I^2S 20bit Data
	1000	X	I^2S 18bit Data
	0000	0	MSB First I^2S 16bit Data
	1100	1	LSB First I^2S 16bit Data
	0001	X	Left-Justified 24bit Data
	0101	X	Left-Justified 20bit Data
	1001	X	Left-Justified 18bit Data
	1101	X	Left-Justified 16bit Data
	0010	X	Right-Justified 24bit Data
	0110	X	Right-Justified 20bit Data
	1010	X	Right-Justified 18bit Data
	1110	X	Right-Justified 16bit Data

5.2.3 Delay Serial Clock Enable

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	0	DSCKE	Delay Serial Clock Enable: 0 – No serial clock delay 1 – Serial clock delay by 1 core clock cycle to tolerate anomalies in some I^2S master devices

5.2.4 Channel Input Mapping

BIT	R/W	RST	NAME	DESCRIPTION
6	R/W	0	C1IM	0 – Processing channel 1 receives Left I^2S Input 1 – Processing channel 1 receives Right I^2S Input
7	R/W	1	C2IM	0 – Processing channel 2 receives Left I^2S Input 1 – Processing channel 2 receives Right I^2S Input

Each channel received via I^2S can be mapped to any internal processing channel via the Channel Input Mapping registers. This allows for flexibility in processing. The default settings of these registers map each I^2S input channel to its corresponding processing channel.

5.3 Configuration Register C(Address 02h)

D7	D6	D5	D4	D3	D2	D1	D0
OCRB	CSZ4	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
1	1	0	0	0	0	1	0

5.3.1 DDX Power Output Mode

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	OM0	DDX Power Output Mode: Selects configuration of DDX output.
1	R/W	1	OM1	

The DDX Power Output Mode selects how the DDX output timing is configured. Different power devices use different output modes. The STA50x or STA51x recommended use is OM = 10.

Table 13. Output Modes

OM(1,0)	Output Stage – Mode
00	STA50x/STA51x – Drop Compensation
01	Discrete Output Stage – Tapered Compensation
10	STA50x/STA51x – Full Power Mode
11	Variable Drop Compensation (CSZx bits)

5.3.2 DDX Compensating Pulse Size Register

BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	0	CSZ0	Contra Size Register: When OM(1,0) = 11, this register determines the size of the DDX compensating pulse from 0 clock ticks to 31 clock periods.
3	R/W	0	CSZ1	
4	R/W	0	CSZ2	
5	R/W	0	CSZ3	
6	R/W	1	CSZ4	

Table 14. Compensating Pulse Size

CSZ(4..0)	Compensating Pulse Size
00000	0ns(0 tick) Compensating Pulse Size
00001	10ns(1 tick) Clock period Compensating Pulse Size
…	…
11111	310ns(31 tick) Clock period Compensating Pulse Size

5.3.3 Over-Current Warning Detect Adjustment Bypass

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	1	OCRB	Over-Current-Warning Adjustment Bypass: 0 - Over-Current warning Adjustment enabled 1 - Over-Current warning Adjustment disabled

The OCDETECT input is used to indicate an Over-Current Warning condition. When OCDETECT is asserted (set to 0), the power control block will force a -3dB adjustment to the modulation limit in an attempt to eliminate the over-current warning condition.

Once the over-current warning volume adjustment is applied, it remains in this state until reset is applied.

5.4 Configuration Register D(Address 03h)

D7	D6	D5	D4	D3	D2	D1	D0
MME	ZDE	DRC	BQL	PSL	DSPB	DEMP	HPB
0	1	0	0	0	0	0	0

5.4.1 High-Pass Filter Bypass

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	HPB	High-Pass Filter Bypass Bit. Setting of one bypasses internal AC coupling digital high-pass filter

The STA320 features an internal digital high-pass filter for the purpose of AC coupling. The purpose of this filter is to prevent DC signals from passing through a DDX amplifier.

DC signals can cause speaker damage. When HPB=0, this filter is enabled

5.4.2 De-Emphasis

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	0	DEMP	DE-emphasis 0 - No De-emphasis 1 - De-emphasis

Setting the DEMP bit enables de-emphasis on all channels

5.4.3 DSP Bypass

BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	0	DSPB	DSP bypass Bit: 0 - Normal Operation 1 - Bypass of Biquad and Bass/Treble Functionality

Setting the DSPB bit bypasses the EQ functionality of the STA320.

5.4.4 Post-Scale Link

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	0	PSL	Post-Scale Link: 0 - Each Channel uses individual Post-Scale value 1 - Each Channel uses Channel 1 Post-Scale value

Post-Scale functionality can be used for power-supply error correction.

For multi-channel applications running off the same power-supply, the post-scale values can be linked to the value of channel 1 for ease of use and update the values faster.

5.4.5 Biquad Coefficient Link

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	0	BQL	Biquad Link: 0 - Each Channel uses coefficient values 1 - Each Channel uses Channel 1 coefficient values

For ease of use, all channels can use the biquad coefficients loaded into the Channel 1 Coefficient RAM space by setting the BQL bit to 1. Therefore, any EQ updates only have to be performed once.

5.4.6 Dynamic Range Compression/Anti-Clipping Bit

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	0	DRC	Dynamic Range Compression/Anti-Clipping 0 – Limiters act in Anti-Clipping Mode 1 – Limiters act in Dynamic Range Compression Mode

Both limiters can be used in one of two ways, anti-clipping or dynamic range compression. When used in anti-clipping mode the limiter threshold values are constant and dependent on the limiter settings.

In dynamic range compression mode the limiter threshold values vary with the volume settings allowing a night-time listening mode that provides a reduction in the dynamic range regardless of the volume level.

5.4.7 Zero-Detect Mute Enable

BIT	R/W	RST	NAME	DESCRIPTION
6	R/W	1	ZDE	Zero-Detect Mute Enable: Setting of 1 enables the automatic zero-detect mute

Setting the ZDE bit enables the zero-detect automatic mute. The zero-detect circuit looks at the data for each processing channel at the output of the crossover (bass management) filter. If any channel receives 2048 consecutive zero value samples (regardless of fs) then that individual channel is muted if this function is enabled

5.4.8 Miami Mode™ Enable

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	MME	Miami-Mode Enable: 0 - Sub Mix into Left/Right Disabled 1 - Sub Mix into Left/Right Enabled

5.5 Configuration Register E(Address 04h)

D7	D6	D5	D4	D3	D2	D1	D0
SVE	ZCE	DCCV	PWMS	AME	NSBW	MPC	MPCV
1	1	0	0	0	0	1	0

5.5.1 Max Power Correction Variable

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	MPCV	Max Power Correction Variable: 0 - Use Standard MPC Coefficient 1 - Use MPCC bits for MPC Coefficient

5.5.2 Max Power Correction

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	1	MPC	Max Power Correction: Setting of 1 enables STA50x/STA51x correction for THD reduction near maximum power output

Setting the MPC bit turns on special processing that corrects the STA50x/STA51x power device at high power. This mode should lower the THD+N of a full STA50x/STA51x DDX system at maximum power output and slightly below. If enabled, MPC is operational in all output modes except tapered (OM(1,0) = 01).

5.5.3 Noise-Shaper Bandwidth Selection

BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	0	NSBW	Noise-Shaper Bandwidth Selection: 1 - 3rd order NS 0 - 4th order NS

5.5.4 AM Mode Enable

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	0	AME	AM Mode Enable: 0 - Normal DDX operation. 1 - AM reduction mode DDX operation

The STA320 features a DDX processing mode that minimizes the amount of noise generated in frequency range of AM radio. This mode is intended for use when DDX is operating in a device with an AM tuner active.

The SNR of the DDX processing is reduced to ~83dB in this mode, which is still greater than the SNR of AM radio.

5.5.5 PWM Speed Mode

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	0	PWMS	PWM Speed Selection: 0 - Normal Speed(384kHz) All Channels 1 - Odd Speed(341.3kHz) All Channels

5.5.6 Distortion Compensation Variable Enable

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	0	DCCV	Distortion Compensation Variable Enable: 0 - Uses Preset DC Coefficient. 1 - Uses DCC Coefficient.

5.5.7 Zero-Crossing Volume Enable

BIT	R/W	RST	NAME	DESCRIPTION
6	R/W	1	ZCE	Zero-Crossing Volume Enable: 1 - Volume adjustments will only occur at digital zero-crossings 0 - Volume adjustments will occur immediately

The ZCE bit enables zero-crossing volume adjustments. When volume is adjusted on digital zero-crossings no clicks will be audible.

5.5.8 Soft Volume Enable

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	1	SVE	Soft Volume Enable: 1 - Volume adjustments ramp according to SVR settings 0 - Volume adjustments will occur immediately

5.6 Configuration Register F(Address 05h)

D7	D6	D5	D4	D3	D2	D1	D0
EAPD	PWDN	ECLE	LDTE	BCLE	IDE	OCFG1P	OCFG0
0	1	0	1	1	1	0	0

5.6.1 Output Configuration

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	OCFG0	Selects the Output Configuration
1	R/W	0	OCFG1	

Table 15. Output Configuration Engine Selection

OCFG(1..0)	Output Configuration
00	2 Channel (Full-Bridge) Power, 1 Channel DDX: 1A/1B → 1A/1B w/ C1BO 0° 2A/2B → 2A/2B w/ C2BO 90/180° 3A/3B →3A/3B w/ C3BO 45°
01	2(Half-Bridge).1(Full-Bridge) On-Board Power: 1A → 1A Binary 0° 2A → 1B Binary 90° 3A/3B → 2A/2B Binary 45° 1A → 3A Binary 0° 2A → 3B Binary 90°
10	2 Channel (Full-Bridge) Power, 2 Channel Data-Out: 1A/1B → 1A/1B Binary 0° 2A/2B → 2A/2B Binary 90° 1A → 3A Binary 0° 2A → 3B Binary 90°
11	1 Channel Mono-Parallel: 3A → 1A/1B w/ C3BO 45° 3B → 2A/2B w/ C3BO 45° 3A/3B → 3A/3B w/ C3BO 45°
Note	To the left of the arrow is the processing channel. Note that though the defaults are shown, using channel output mapping, any of the three processing channel outputs can be used for any of the three inputs

5.6.2 Invalid Input Detect Mute Enable

BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	1	IDE	Invalid Input Detect Mute Enable: Setting of 1 enables the automatic invalid input detect mute

Setting the IDE bit enables this function, which looks at the input I^2S data and will automatically mute if the signals are perceived as invalid.

5.6.3

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	1	BCLE	Binary Output Mode Clock Loss Detection Enable

Detects loss of input MCLK in binary mode and will output 50% duty cycle.

5.6.4

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	1	LDTE	LRCLK Double Trigger Protection Enable

Actively prevents double trigger of LRCLK.

5.6.5

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	0	ECLE	Auto EAPD on Clock Loss

When active will issue a power device power down signal(EAPD) on clock loss detection

5.6.6 IC Power Down

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	1	PWDN	IC Power Down: 0 - IC Power Down Low-Power Condition 1 - IC Normal Operation

The PWDN register is used to place the IC in a low-power state. When PWDN is written as 0, the output will begin a soft-mute.

After the mute condition is reached, EAPD will be asserted to power down the power-stage, then the master clock to all internal hardware expect the I^2C block will be gated. This places the IC in a very low power consumption stateConf

5.6.7 External Amplifier Power Down

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	EAPD	External Amplifier Power Down: 0 -External Power Stage Power Down Active 1 -Normal Operation

5.7 Volume Control Registers(Addresses 06-0Ah)

5.7.1 Mute/QXpander RegisterI

D7	D6	D5	D4	D3	D2	D1	D0
QFILT	QXEN		TFRB	C3M	C2M	C1M	MMUTE
0	0		1	0	0	0	00

5.7.2 Thermal Fault(TWARN2) Recovery Bypass

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	1	TFRB	Thermal-Fault (TWARN2) Recovery Bypass: 0 - Thermal fault recovery enabled 1 - Thermal fault recovery disabled

The TWARN2(Thermal Fault) input is used to indicate a thermal fault condition by an appropriate power device. When TWARN2 is asserted (set to 0), the power control block will attempt a recovery from the fault by asserting the tri-state output (setting it to 0 which directs the power output block to begin recovery), hold it at 0 for period of time in the range of .1ms to 1 second as defined by the Fault-Detect Recovery Constant register (FDRC registers 29-2Ah), then toggle it back to 1.

This sequence is repeated as log as the fault indication exists. This feature is disabled by default but can be enabled by setting the TFRB control bit to 0.

5.7.3 Qxpander Enable

BIT	R/W	RST	NAME	DESCRIPTION
6	R/W	0	QXEN	Qxpander Enable: 0 - QXPander Disabled 1 - QXPander Enabled with proper security code

5.7.4 Qfilter Select

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	QFilt	Qfilter Select 0 - Qfilter Used 1 - Simple LPF Used

5.7.5 Master Volume Register

D7	D6	D5	D4	D3	D2	D1	D0
MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
1	1	1	1	1	1	1	1

5.7.6 Channel 1 Volume

D7	D6	D5	D4	D3	D2	D1	D0
C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0	1	1	0	0	0	0	0

5.7.7 Channel 2 Volume

D7	D6	D5	D4	D3	D2	D1	D0
C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0	1	1	0	0	0	0	0

5.7.8 Channel 3 Volume

D7	D6	D5	D4	D3	D2	D1	D0
C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0	1	1	0	0	0	0	0

The Volume structure of the STA320 consists of individual volume registers for each channel and a master volume register that provides an offset to each channels volume setting. The individual channel volumes are adjustable in 0.5dB steps from +48dB to -80 dB.

As an example if C3V = 00h or +48dB and MV = 18h or -12dB, then the total gain for channel 3 = +36dB. The Master Mute when set to 1 will mute all channels at once, whereas the individual channel mutes(CxM) will mute only that channel.

Both the Master Mute and the Channel Mutes provide a "soft mute" with the volume ramping down to mute in 4096 samples from the maximum volume setting at the internal processing rate(~96kHz). A "hard mute" can be obtained by commanding a value of all 1's(255) to any channel volume register or the master volume register. When volume offsets are provided via the master volume register any channel that whose total volume is less than -80dB will be muted.

All changes in volume take place at zero-crossings when ZCE = 1(configuration register F) on a per channel basis as this creates the smoothest possible volume transitions. When ZCE=0, volume updates will occur immediately.

Table 16. Master Volume Offset as a function of MV(7..0).

MV(7..0)	Volume Offset from Channel Value
00000000(00h)	0dB
00000001(01h)	-0.5dB
00000010(02h)	-1dB
…	…
01001100(4Ch)	-38dB
…	…
11111110(FEh)	-127dB
11111111(FFh)	Hard Master Mute

Table 17. Channel Volume as a function of CxV(7..0)

CxV(7..0)	Volume
00000000(00h)	+48dB
00000001(01h)	+47.5dB
00000010(02h)	+47dB
…	…
01100001(5Fh)	+0.5dB
01100000(60h)	0dB
01011111(61h)	-0.5dB
…	…
11010111(D7h)	+59.5dB
11011000(D8h)	-60dB
11011001(D9h)	-61dB
11011010(DAh)	-62dB
…	…
11101100(ECh)	-80 dB
11101101(EDh)	Hard Channel Mute
…	…
11111111(FFh)	Hard Channel Mute

5.8 Auto Mode Registers

5.8.1 AutoMode Register 1(Address 0x0B)

D7	D6	D5	D4	D3	D2	D1	D0
AMPS		AMGC1	AMGC2	AMV2	AMV1	AMEQ1	AMEQ0
1		0	0	0	0	0	0

Table 18. AutoMode EQ Settings

AMEQ(1,0)	Mode(Biquad 2-6)
00	User Programmable
01	Preset EQ – PEQ bits
10	Auto Volume Controlled Loudness Curve
11	NA

By setting AMEQ to any setting other than 00 enables AutoMode EQ. When set, biquads 1-4 are not user programmable. Any coefficient settings for these biquads will be ignored. Also when AutoMode EQ is used the pre-scale value for channels 1-6 becomes hard-set to -18dB, dependent upon the value of AMPS

Table 19. AutoMode Volume Settings

AMV(1,0)	Mode(MVOL)
00	MVOL 0.5dB 256 Steps (Standard)
01	MVOL Auto Curve 30 Steps
10	MVOL Auto Curve 40 Steps
11	MVOL Auto Curve 50 Steps

Table 20. Automode Gain Compression/Limiters Selection

AMGC(1...0)	Mode
00	User Programmable GC
01	AC No Clipping 2.1
10	AC Limited Clipping (10%) 2.1
11	DRC Nighttime Listening Mode 2.1

5.8.2

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	1	AMPS	AutoMode Pre-Scale 0 - User Defined Pre-scale when AMEQ /= 00 1 - -18dB used for Pre-scale when AMEQ /= 00

5.8.3 AutoMode Register 2(Address 0x0C)

D7	D6	D5	D4	D3	D2	D1	D0
XO3	XO2	XO1	XO0	AMAM2	AMAM1	AMAM0	AMAME
0	0	0	0	0	0	0	0

5.8.4 AM Interference Frequency Switching

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	AMAME	AutoMode AM Enable 0 - Switching Frequency Determined by PWMS Setting 1 - Switching Frequency Determined by AMAM Settings

Table 21. AutoMode AM Switching Frequency Selection

AMAM(2..0)	48kHz/96kHz Input Fs	44.1kHz/88.2kHz Input Fs
000	0.535MHz – 0.720MHz	0.535MHz – 0.670Mhz
001	0.721MHz – 0.900MHz	0.671MHz – 0.800MHz
010	0.901MHz – 1.100MHz	0.801MHz – 1.000MHz
011	1.101MHz – 1.300MHz	1.001MHz – 1.180MHz
100	1.301MHz – 1.480MHz	1.181MHz – 1.340Mhz
101	1.481MHz – 1.600MHz	1.341MHz – 1.500MHz
110	1.601MHz – 1.700MHz	1.501MHz – 1.700MHz

5.8.5 Bass Management Crossover

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	0	XO0	Selects the Bass-Management Crossover Frequency. A 1st-Order Hi-Pass filter (channels 1 and 2) or a 2nd-Order Lo-pass filter (channel 3) at the selected frequency is performed.
5	R/W	0	XO1	
6	R/W	0	XO2	
7	R/W	0	XO3	

Table 22. Bass Management Crossover Frequency

XO3..0)	Crossover Frequency
0000	User -Defined
0001	80 Hz
0010	100 Hz
0011	120 Hz
0100	140 Hz
0101	160 Hz
0110	180 Hz
0111	200 Hz
1000	220 Hz
1001	240 Hz
1010	260 Hz
1011	280 Hz
1100	300 Hz
1101	320 Hz
1110	340 Hz
1111	360 Hz

5.8.6 AutoModeRegister 3 (address 0x0D)

D7	D6	D5	D4	D3	D2	D1	D0
			PEQ4	PEQ3	PEQ2	PEQ1	PEQ0
			0	0	0	0	0

Table 23. Preset EQ Settings

PEQ(3..0)	Setting
00000	Flat
00001	Rock
00010	Soft Rock
00011	Jazz
00100	Classical
00101	Dance
00110	Pop
00111	Soft
01000	Hard
01001	Party
01010	Vocal
01011	Hip-Hop
01100	Dialog
01101	Bass-Boost #1
01110	Bass-Boost #2
01111	Bass-Boost #3
10000	Loudness 1 (least boost)
10001	Loudness 2
10010	Loudness 3
10011	Loudness 4
10100	Loudness 5
10101	Loudness 6
10110	Loudness 7
10111	Loudness 8
11000	Loudness 9
11001	Loudness 10
11010	Loudness 11
11011	Loudness 12
11100	Loudness 13
11101	Loudness 14
11110	Loudness 15
11111	Loudness 16 (most boost)

5.9 Channel Configuration Registers(Addresses 0E-10h

5.9.1)

D7	D6	D5	D4	D3	D2	D1	D0
C1OM1	C1OM0	C1LS1	C1LS0	C1BO	C1VPB	C1EQBP	C1TCB
0	0	0	0	0	0	0	0

5.9.2

D7	D6	D5	D4	D3	D2	D1	D0
C2OM1	C2OM0	C2LS1	C2LS0	C2BO	C2VPB	C2EQBP	C2TCB
0	0	0	0	0	0	0	0

5.9.3

D7	D6	D5	D4	D3	D2	D1	D0
C3OM1	C3OM0	C3LS1	C3LS0	C2BO	C3VPB		
1	0	0	0	0	0		

5.9.4 Tone Control Bypass

Tone control(bass/treble) can be bypassed on a per channel basis for channels 1 and 2.

CxTCB:

0 - Perform Tone Control on Channel X - normal operation

1 - Bypass Tone Control on Channel X

5.9.5 EQ Bypass

EQ control can be bypassed on a per channel basis for channels 1 and 2. If EQ control is bypassed on a given channel the prescale and all filters (high-pass, biquads, de-emphasis, bass, treble in any combination) are bypassed for that channel.

CxEQBP:

0 - Perform EQ on Channel X - normal operation

1 - Bypass EQ on Channel X

5.9.6 Volume Bypass

Each channel contains an individual channel volume bypass. If a particular channel has volume bypassed via the CxVBP = 1 register then only the channel volume setting for that particular channel affects the volume setting, the master volume setting will not affect that channel.

5.9.7 Binary Output Enable Registers

Each individual channel output can be set to output a binary PWM stream. In this mode output A of a channel will be considered the positive output and output B is negative inverse.

CxBO:

0 - DDX tri-state output - normal operation

1 - Binary OutputLimiter Select

Limiter Selection can be made on a per-channel basis according to the channel limiter select bits.

Table 24. Channel Limiter Mapping as a function of CxLS bits

CxLS(1,0)	Channel Limiter Mapping
00	Channel has limiting disabled
01	Channel is mapped to limiter #1
10	Channel is mapped to limiter #2

5.9.8 Output Mapping

Output mapping can be performed on a per channel basis according to the CxOM channel output mapping bits. Each input into the output configuration engine can receive data from any of the three processing channel outputs.

Table 25. Channel Output Mapping as a function of CxOM bits.

CxOM(1,0)	Channel x Output Source Form
00	Channel 1
01	Channel 2
10	Channel 3

5.10 Tone Control register (Address 11h)

5.10.1 Tone Control

D7	D6	D5	D4	D3	D2	D1	D0
TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0	1	1	1	0	1	1	1

5.10.2 Tone Control Boost/Cut as a function of BTC and TTC bits.

BTC(3..0)/TTC(3..0)	Boost/Cut
0000	-12dB
0001	-12dB
…	…
0111	-4dB
0110	-2dB
0111	0dB
1000	+2dB
1001	+4dB
…	…
1101	+12dB
1110	+12dB
1111	+12dB

5.11 Dynamics Control Registers (Addresses 12-15h)

5.11.1 Limiter 1 Attack/Release Rate

D7	D6	D5	D4	D3	D2	D1	D0
L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0	1	1	0	1	0	1	0

5.11.2 Limiter 1 Attack/Release Threshold

D7	D6	D5	D4	D3	D2	D1	D0
L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0	1	1	0	1	0	0	1

5.11.3 Limiter 2 Attack/Release Rate

D7	D6	D5	D4	D3	D2	D1	D0
L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0	1	1	0	1	0	1	0

5.11.4 Limiter 2 Attack/Release Threshold

D7	D6	D5	D4	D3	D2	D1	D0
L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0	1	1	0	1	0	0	1

The STA320 includes 2 independent limiter blocks. The purpose of the limiters is to automatically reduce the dynamic range of a recording to prevent the outputs from clipping in anti-clipping mode or to actively reduce the dynamic range for a better listening environment such as a night-time listening mode which is often needed for DVDs. The two modes are selected via the DRC bit in Configuration Register F, bit 0 address 0x05. Each channel can be mapped to either limiter or not mapped, meaning that channel will clip when 0dBFS is exceeded. Each limiter will look at the present value of each channel that is mapped to it, select the maximum absolute value of all these channels, perform the limiting algorithm on that value, and then if needed adjust the gain of the mapped channels in unison.

The limiter attack thresholds are determined by the LxAT registers. It is recommended in anti-clipping mode to set this to 0dBFS, which corresponds to the maximum unclipped output power of a DDX amplifier. Since gain can be added digitally within the STA320 it is possible to exceed 0dBFS or any other LxAT setting, when this occurs, the limiter, when active, will automatically start reducing the gain. The rate at which the gain is reduced when the attack threshold is exceeded is dependent upon the attack rate register setting for that limiter. The gain reduction occurs on a peak-detect algorithm. The release of limiter, when the gain is again increased, is dependent on a RMS-detect algorithm. The output of the volume/limiter block is passed through a RMS filter. The output of this filter is compared to the release threshold, determined by the Release Threshold register. When the RMS filter output falls below the release threshold, the gain is again increased at a rate dependent upon the Release Rate register. The gain can never be increased past it's set value and therefore the release will only occur if the limiter has already reduced the gain. The release threshold value can be used to set what is effectively a minimum dynamic range, this is helpful as over-limiting can reduce the dynamic range to virtually zero and cause program material to sound "lifeless".

In AC mode the attack and release thresholds are set relative to full-scale. In DRC mode the attack threshold is set relative to the maximum volume setting of the channels mapped to that limiter and the release threshold is set relative to the maximum volume setting plus the attack threshold.

Figure 5. Basic Limiter and Volume Flow Diagram.

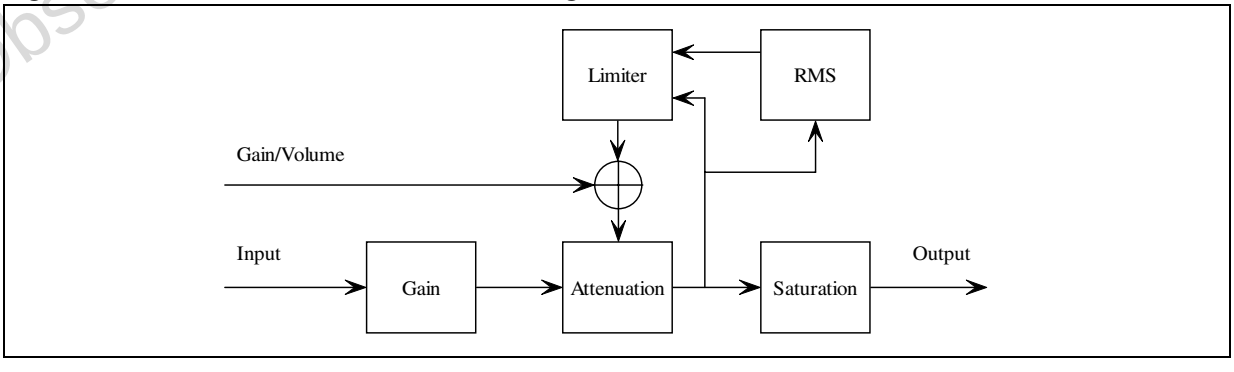


Table 26. Limiter Attack Rate as a function of LxA bits.

LxA(3..0)	Attack Rate dB/ms	
0000	3.1584	Fast
0001	2.7072	
0010	2.2560	
0011	1.8048	
0100	1.3536	
0101	0.9024	
0110	0.4512	
0111	0.2256	
1000	0.1504	
1001	0.1123	
1010	0.0902	
1011	0.0752	
1100	0.0645	
1101	0.0564	
1110	0.0501	
1111	0.0451	Slow

Table 27. Limiter Release Rate as a function of LxR bits.

LxR(3..0)	Release Rate dB/ms	
0000	0.5116	Fast
0001	0.1370	
0010	0.0744	
0011	0.0499	
0100	0.0360	
0101	0.0299	
0110	0.0264	
0111	0.0208	
1000	0.0198	
1001	0.0172	
1010	0.0147	
1011	0.0137	
1100	0.0134	
1101	0.0117	
1110	0.0110	
1111	0.0104	Slow

5.12 Anti-Clipping Mode

Table 28. Limiter Attack Threshold as a function of LxAT bits (AC-Mode).

LxAT(3..0)	AC(dB relative to FS)
0000	-12
0001	-10
0010	-8
0011	-6
0100	-4
0101	-2
0110	0
0111	+2
1000	+3
1001	+4
1010	+5
1011	+6
1100	+7
1101	+8
1110	+9
1111	+10

Table 29. Limiter Release Threshold as a as a function of LxRT bits (AC-Mode).

LxRT(3..0)	AC(dB relative to FS)
0000	-∞
0001	-29dB
0010	-20dB
0011	-16dB
0100	-14dB
0101	-12dB
0110	-10dB
0111	-8dB
1000	-7dB
1001	-6dB
1010	-5dB
1011	-4dB
1100	-3dB
1101	-2dB
1110	-1dB
1111	-0dB

5.13 Dynamic Range Compression Mode

Table 30. Limiter Attack Threshold as a function of LxAT bits (DRC-Mode).

LxAT(3..0)	DRC(dB relative to Volume)
0000	-31
0001	-29
0010	-27
0011	-25
0100	-23
0101	-21
0110	-19
0111	-17
1000	-16
1001	-15
1010	-14
1011	-13
1100	-12
1101	-10
1110	-7
1111	-4

Table 31. Limiter Release Threshold as a as a function of LxRT bits (DRC-Mode).

LxRT(3..0)	DRC(db relative to Volume + LxAT)
0000	-∞
0001	-38dB
0010	-36dB
0011	-33dB
0100	-31dB
0101	-30dB
0110	-28dB
0111	-26dB
1000	-24dB
1001	-22dB
1010	-20dB
1011	-18dB
1100	-15dB
1101	-12dB
1110	-9dB
1111	-6dB

5.14 User-Defined Coefficient Control Registers (Addresses 16-26h)

5.14.1 Coefficient Address Register 1

D7	D6	D5	D4	D3	D2	D1	D0
		CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
		0	0	0	0	0	0

5.14.2 Coefficient b1 Data Register Bits 23..16

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

5.14.3 Coefficient b1 Data Register Bits 15..8

D7	D6	D5	D4	D3	D2	D1	D0
C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0	0	0	0	0	0	0	0

5.14.4 Coefficient b1 Data Register Bits 7..0

D7	D6	D5	D4	D3	D2	D1	D0
C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0	0	0	0	0	0	0	0

5.14.5 Coefficient b2 Data Register Bits 23..16

D7	D6	D5	D4	D3	D2	D1	D0
C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0	0	0	0	0	0	0	0

5.14.6 Coefficient b2 Data Register Bits 15..8

D7	D6	D5	D4	D3	D2	D1	D0
C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0	0	0	0	0	0	0	0

5.14.7 Coefficient b2 Data Register Bits 7..0

D7	D6	D5	D4	D3	D2	D1	D0
C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0	0	0	0	0	0	0	0

5.14.8 Coefficient a1 Data Register Bits 23..16

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

5.14.9 Coefficient a1 Data Register Bits 15..8

D7	D6	D5	D4	D3	D2	D1	D0
C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0	0	0	0	0	0	0	0

5.14.10Coefficient a1 Data Register Bits 7..0

D7	D6	D5	D4	D3	D2	D1	D0
C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0	0	0	0	0	0	0	0

5.14.11Coefficient a2 Data Register Bits 23..16

D7	D6	D5	D4	D3	D2	D1	D0
C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0	0	0	0	0	0	0	0

5.14.12Coefficient a2 Data Register Bits 15..8

D7	D6	D5	D4	D3	D2	D1	D0
C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0	0	0	0	0	0	0	0

5.14.13Coefficient a2 Data Register Bits 7..0

D7	D6	D5	D4	D3	D2	D1	D0
C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0	0	0	0	0	0	0	0

5.14.14Coefficient b0 Data Register Bits 23..16

D7	D6	D5	D4	D3	D2	D1	D0
C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0	0	0	0	0	0	0	0

5.14.15Coefficient b0 Data Register Bits 15..8

D7	D6	D5	D4	D3	D2	D1	D0
C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0	0	0	0	0	0	0	0

5.14.16Coefficient b0 Data Register Bits 7..0

D7	D6	D5	D4	D3	D2	D1	D0
C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0	0	0	0	0	0	0	0

5.14.17Coefficient Write Control Register

D7	D6	D5	D4	D3	D2	D1	D0
				RA	R1	WA	W1
				0	0	0	0

Coefficients for user-defined EQ, Mixing, Scaling, and Bass Management are handled internally in the STA320 via RAM. Access to this RAM is available to the user via an I^2C register interface. A collection of I^2C registers are dedicated to this function.

One contains a coefficient base address, five sets of three store the values of the 24-bit coefficients to be written or that were read, and one contains bits used to control the write/read of the coefficient(s) to/from RAM. The following are instructions for reading and writing coefficients.

5.14.18 Reading a coefficient from RAM

- write 6-bits of address to I²C register 14h
- write 1 to R1 bit in I²C address 24h
- read top 8-bits of coefficient in I²C address 15h
- read middle 8-bits of coefficient in I²C address 16h
- read bottom 8-bits of coefficient in I²C address 17h

5.14.19 Reading a set of coefficients from RAM

- write 6-bits of address to I²C register 14h
- write 1 to RA bit in I²C address 24h
- read top 8-bits of coefficient in I²C address 15h
- read middle 8-bits of coefficient in I²C address 16h
- read bottom 8-bits of coefficient in I²C address 17h
- read top 8-bits of coefficient b2 in I²C address 18h
- read middle 8-bits of coefficient b2 in I²C address 19h
- read bottom 8-bits of coefficient b2 in I²C address 1Ah
- read top 8-bits of coefficient a1 in I²C address 1Bh
- read middle 8-bits of coefficient a1 in I²C address 1Ch
- read bottom 8-bits of coefficient a1 in I²C address 1Dh
- read top 8-bits of coefficient a2 in I²C address 1Eh
- read middle 8-bits of coefficient a2 in I²C address 1Fh
- read bottom 8-bits of coefficient a2 in I²C address 20h
- read top 8-bits of coefficient b0 in I²C address 21h
- read middle 8-bits of coefficient b0 in I²C address 22h
- read bottom 8-bits of coefficient b0 in I²C address 23h

5.14.20 Writing a single coefficient to RAM

- write 6-bits of address to I²C register 14h
- write top 8-bits of coefficient in I²C address 15h
- write middle 8-bits of coefficient in I²C address 16h
- write bottom 8-bits of coefficient in I²C address 17h
- write 1 to W1 bit in I²C address 24h

5.14.21 Writing a set of coefficients to RAM

- write 6-bits of starting address to I²C register 14h
- write top 8-bits of coefficient b1 in I²C address 15h
- write middle 8-bits of coefficient b1 in I²C address 16h
- write bottom 8-bits of coefficient b1 in I²C address 17h
- write top 8-bits of coefficient b2 in I²C address 18h
- write middle 8-bits of coefficient b2 in I²C address 19h

- write bottom 8-bits of coefficient b2 in I^2C address 1Ah
- write top 8-bits of coefficient a1 in I^2C address 1Bh
- write middle 8-bits of coefficient a1 in I^2C address 1Ch
- write bottom 8-bits of coefficient a1 in I^2C address 1Dh
- write top 8-bits of coefficient a2 in I^2C address 1Eh
- write middle 8-bits of coefficient a2 in I^2C address 1Fh
- write bottom 8-bits of coefficient a2 in I^2C address 20h
- write top 8-bits of coefficient b0 in I^2C address 21h
- write middle 8-bits of coefficient b0 in I^2C address 22h
- write bottom 8-bits of coefficient b0 in I^2C address 23h
- write 1 to WA bit in I^2C address 24h

The mechanism for writing a set of coefficients to RAM provides a method of updating the five coefficients corresponding to a given biquad (filter) simultaneously to avoid possible unpleasant acoustic side-effects. When using this technique, the 6-bit address would specify the address of the biquad b1 coefficient (e.g. 0, 5, 10, …, 20, … 35 decimal), and the STA320 will generate the RAM addresses as offsets from this base value to write the complete set of coefficient data.

5.14.22User-Defined EQ

The STA320 provides the ability to specify four EQ filters (biquads) per each of the two input channels. The biquads use the following equation:

$$Y[n] = 2(b_0/2)X[n] + 2(b_1/2)X[n-1] + b_2X[n-2] - 2(a_1/2)Y[n-1] - a_2Y[n-2]$$
$$= b_0X[n] + b_1X[n-1] + b_2X[n-2] - a_1Y[n-1] - a_2Y[n-2]$$

where Y[n] represents the output and X[n] represents the input. Multipliers are 24-bit signed fractional multipliers, with coefficient values in the range of 800000h (-1) to 7FFFFFh (0.9999998808).

Coefficients stored in the User Defined Coefficient RAM are referenced in the following manner:

CxHy0 = b1/2
CxHy1 = b2
CxHy2 = -a1/2
CxHy3 = -a2
CxHy4 = b0/2

where x represents the channel and the y the biquad number. For example C2H41 is the b_2 coefficient in the fourth biquad for channel 2.

Additionally, the STA320 allows specification of a high-pass filter (processing channels 1 and 2) and a lo-pass filter (processing channel 3) to be used for bass-management crossover when the XO setting is "000" (user-defined).

Both of these filters when defined by the user (rather than using the preset crossover filters) are 2nd order filters that use the biquad equation noted above. They are loaded into the C12H0-4 and C3Hy0-4 areas of RAM noted in the table below.

By default, all user-defined filters are "pass-thru" where all coefficients are set to 0, except the b0/2 coefficient which is set to 400000h (representing 0.5)

5.14.23Pre-Scale

The STA320 provides a multiplication for each input channel for the purpose of scaling the input prior to EQ. This pre-EQ scaling is accomplished by using a 24-bit signed fractional multiplier, with 800000h = -1 and 7FFFFFh = 0.9999998808.

The scale factor for this multiply is loaded into RAM using the same I^2C registers as the biquad coefficients and the bass-management. All channels can use the channel 1 pre-scale factor by setting the Biquad link bit. By default, all pre-scale factors are set to 7FFFFFh.

5.14.24Post-Scale

The STA320 provides one additional multiplication after the last interpolation stage and the distortion compensation on each channel. This post-scaling is accomplished by using a 24-bit signed fractional multiplier, with 800000h = -1 and 7FFFFFh = 0.9999998808.

The scale factor for this multiply is loaded into RAM using the same I^2C registers as the biquad coefficients and the bass-management.

This post-scale factor can be used in conjunction with an ADC equipped micro-controller to perform power-supply error correction. All channels can use the channel 1 post-scale factor by setting the post-scale link bit. By default, all post-scale factors are set to 7FFFFFh.

5.14.25Over-current Post-Scale

The STA320 provides a simple mechanism for reacting to over-current detection in the power-device. When the ocdetect input is asserted, the over-current post-scale value is used in place of the normal post-scale value to provide output attenuation on all channels.

The default setting provides 3dB of output attenuation when ocdetect is asserted. The amount of attenuation to be applied in this situation can be adjusted by modifying the Over-current Post-scale value.

As with the normal post-scale, this scaling value is a 24-bit signed fractional multiplier, with 800000h = -1 and 7FFFFFh = 0.9999998808. By default, the over-current post-scale factor is set to 5A9DF7h. Once the over-current attenuation is applied, it remains until the device is reset.

Table 32. RAM Block for Biquads, Mixing, and Bass Management

Index (Decimal)	Index (Hex)		Coefficient	Default
0	00h	Channel 1 – Biquad 1	C1H10(b1/2)	000000h
1	01h		C1H11(b2)	000000h
2	02h		C1H12(a1/2)	000000h
3	03h		C1H13(a2)	000000h
4	04h		C1H14(b0/2)	400000h
5	05h	Channel 1 – Biquad 2	C1H20	000000h
…	…	…	…	…
19	13h	Channel 1 – Biquad 4	C1H44	400000h
20	14h	Channel 2 – Biquad 1	C2H10	000000h
21	15h		C2H11	000000h
…	…	…	…	…
39	27h	Channel 2 – Biquad 4	C2H44	400000h
40	28h	Hi-Pass 2nd Order Filter for XO=000	C12H0(b1/2)	000000h
41	29h		C12H1(b2)	000000h
42	2Ah		C12H2(a1/2)	000000h
43	2Bh		C12H3(a2)	000000h
44	2Ch		C12H4(b0/2)	400000h
45	2Dh	Lo-Pass 2nd Order Filter for XO=000	C3H0(b1/2)	000000h
46	2Eh		C3H1(b2)	000000h
47	2Fh		C3H2(a1/2)	000000h
48	30h		C3H3(a2)	000000h
49	31h		C3H4(b0/2)	400000h
50	32h	Channel 1 – Pre-Scale	C1PreS	7FFFFFh
51	33h	Channel 2 – Pre-Scale	C2PreS	7FFFFFh
52	34h	Channel 1 – Post-Scale	C1PstS	7FFFFFh
53	35h	Channel 2 – Post-Scale	C2PstS	7FFFFFh
54	36h	Channel 3 – Post-Scale	C3PstS	7FFFFFh
55	37h	Over-Current – Post-Scale	OCPstS	5A9DF7h
56	38h	Channel 1 – Mix 1	C1MX1	7FFFFFh
57	39h	Channel 1 – Mix 2	C1MX2	000000h
58	3Ah	Channel 2 – Mix 1	C2MX1	000000h
59	3Bh	Channel 2 – Mix 2	C2MX2	7FFFFFh
60	3Ch	Channel 3 – Mix 1	C3MX1	400000h
61	3Dh	Channel 3 – Mix 2	C3MX2	400000h
62	3Eh	UNUSED		
63	3Fh	UNUSED		

5.15 Variable Max Power Correction Registers (Addresses 27-29h):

MPCC bits determine the 16 MSBs of the MPC compensation coefficient. This coefficient is used in place of the default coefficient when MPCV = 1

5.15.1.

D7	D6	D5	D4	D3	D2	D1	D0
MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0	0	1	0	1	1	0	1

5.15.2

D7	D6	D5	D4	D3	D2	D1	D0
MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
1	1	0	0	0	0	0	0

5.16 Fault Detect Recovery Constant Registers(Addresses 2B-2Ch)

FDRC bits specify the 16-bit Fault Detect Recovery time delay. When FAULT is asserted, the TRISTATE output will be immediately asserted lo and held lo for the time period specified by this constant. A constant value of 0001h in this register is ~.083ms. The default value of 000C specifies ~.1mSec.

5.16.1

D7	D6	D5	D4	D3	D2	D1	D0
FDRC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
0	0	0	0	0	0	0	0

5.16.2

D7	D6	D5	D4	D3	D2	D1	D0
FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
0	0	0	0	1	1	0	0

5.17 Device Status Register(Address 2Dh)

D7	D6	D5	D4	D3	D2	D1	D0
PLLUL				OCWARN	TFAULT	FAULT	TWARN
				1	1	1	1

This register provides Fault and Thermal-Warning status information from the power control block.

5.18 Reserved Registers(Address 2Fh)

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	RES	RES	RES	RES
0	1	1	1	0	0	0	0

5.19 Reserved Registers(Addresses 30h-31h)

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	RES	RES	RES	RES

5.19.1

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	RES	RES	RES	RES

For details see next AN.

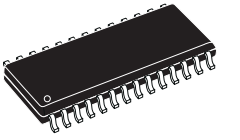
6 PACKAGE INFORMATION

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 6. SO28 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA



SO-28

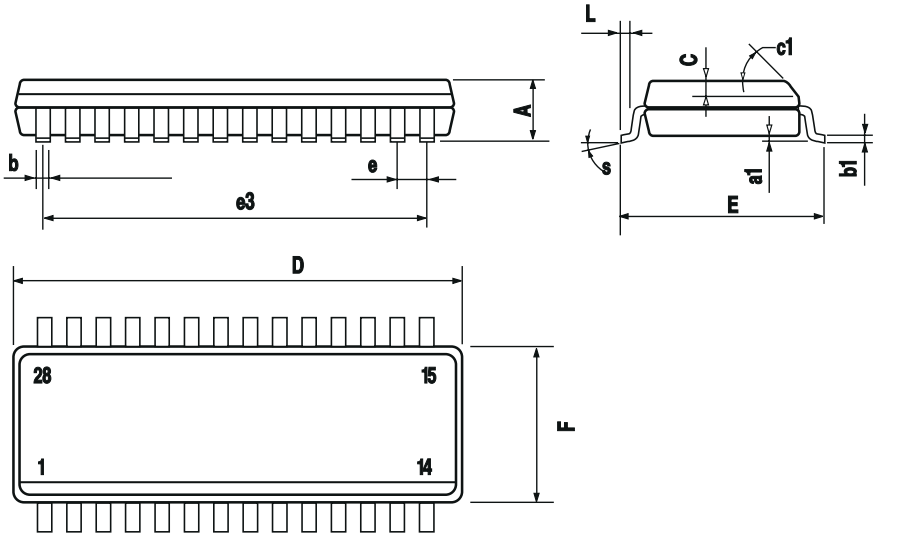


Table 33. Revision History

Date	Revision	Description of Changes
November 2004	1	First Issue