MB86276 'LIME'

Graphics Display Controller
Specifications

Revision 1.1a

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FUJITSU

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Revision history

Date	Version	Page count	Change
2005.2.10	0.1	176	First edition
2005.3.12	0.2	225	The description of Video Capture is added.
2005.6.15	0.92	237	The pin list and the description of modeis are added.
2005.7.14	0.93b	278	DC, AC characteristics are added. The description of Memory Map, Dual Monitor, and the capacity of SDRAM are updated. The table of the pin multiplex is updated. Other update.
2005.8.17	0.93c	278	The description of the unimplemented functions, the geometry registers and the analog RGB output, were deleted.
2005.9.19	0.93d	278	Misprint correction.
2005.10.17	0.94	282	P.14 The pin list of thermal balls is added. P.15-16 Several pins are renamed to "TESTH" or "TESTL". P.26 "TESTL" is added in the table of test pins. P.30 RDY_MODE, ENDIAN signals are added. P.31 The table of GMODE is updated. P.249 The lost character is displayed.
2006.1.18	0.95	281	P.18-19 The description "TOP VIEW" is inserted in Pin diagram. P.28 The description was doubled about RDY_MODE and BS_MODE is deleted. P.29-30 "Connection to CPU" is updated. P.31 The paragraph "Graphics memory interface" is moved from Chapter 3. P.64 The table of "Resolution and Display Frequency" is updated. P.150-151 The LOWD field of MMR register is updated. Other: Misprint correction.
2006.1.27	0.96	297	P.10 Connectable Memoey configuration is updated. P.21 The description of the symbol regarding VDD/GND is added. P.30 The connection between CPU and Lime is updated. P.31 The pin information of serial host interface is added. P.66 Connection with memory is updated. P.81 Chapter 6.8 in previous version is removed. P.153 The description of CCF register is added. P.160 The description of I2C I/F register is added. P.291 The note about AC timing specification of Host I/F is added. Other: Misprint correction.

Date	Version	Page count	Change
2006.2.14 2006.3.30	0.97 0.97a	327	P.23 The description "TESTL" is updated. P.47 The protocol for general call address is updated. P.47 Misprint about Acknowledge in the protocol for SCI are corrected. P.51 Line transfer of SCI is updated. P.52 The description of I2C interface was added at ver.0.96. P.138 SCI register list is added. P.160 The description of SCI registers are added. P.177 DCM,DCE,DCEE registers are changed to DCM0/1/2/3 registers. P.279 Timing chart of Host interface for SH3/4, V832, SPARClite are added. P.295 Timing chart of Host interface for 16bit CPU, 16bit AD-MUX CPU, 32bit AD-MUX CPU are added. Other: Misprint correction.
2006.6.5	1.0		P.28 Note of XRDY signal is updated. P.33 Connection of XWE1 signal is updated. P.47 Description of 16-bit CPU mode is added. P.161 Host register descriptions are added, DMA_ST_ADR, DMA_ED_ADR, ERR_ADR, ERR_DETECT, INT_MSK. P.172 Add Revision Register :PIO Base + 0x84 P.316 Video Capture AC Timing Hold 2ns => 0ns P.321 Clear the meaning of tr,tf
2010.3.20	1.1		Remove spec of I2C slave Add explanations and revise typos.
2010.5.17	1.1a		Clear the setting of reserverd area

Contents

1 GENERAL

1.1 Features

CMOS 0.18µm technology

Internal and memory frequency : 133MHz (generated by on-chip PLL)

Base-clock for display clocks : 400.9MHz (generated by on-chip PLL)

Display resolutions typically from 320x240 up to 1280x768

6 layers of overlay display (windows)

Alpha Plane and constant alpha value for each layer

Digital Video input (various formats including YUV,RGB)

Video Scaler (up/down scaling)

Brightness, Contrast, Saturation control for video input

RGB digital output (8bit x 3)

Built-in alpha blending, anti-aliasing and chroma-keying

Rendering Engine for various kinds of 2D graphic acceleration functions

Texture Mapping Unit for 2D polygon support up to 4096x4096 textures

Bit-Blt Unit for transfers up to 4096x4096 areas

Alpha Bit-Blt and ROP2 functions

External 32-bit SDRAM interface for up to 64MB graphic memory

Parallel host interface (FR,SH3,SH4,V850,SparcLite etc)

New additional serial control interface as host interface (I2C based)

Internal and external DMA support

I2C interface and GPIO inputs/outputs

Supply voltage 3.3V (I/O), 1.8V (Internal)

BGA-320 Package (1.27mm pitch)

Typical power consumption < 1.0W (estimated)

Temperature range -40..+85 °C

1.2 Functional Overview

1.2.1 Host CPU interface

Supported CPU

LIME can be connected to SH3 and SH4 manufactured by RENESAS, V832 by NEC, CPU with address and data multiplex bus like PowerPC by Freescale, FR and SPARClite (MB86833) by Fujitsu.

External Bus Clock

Can be connected at max. 66 MHz (when using SH4 interface)

Ready Mode

Supports normal ready/not ready.

Endian

Supports little endian. Big endian is also available in 16bit mode.

Access Mode

SRAM interface

FIFO interface (transfer destination address fixed)

DMA transfer

Supports 1-double word (32 bits) /8-double word (32 bytes) (only SH4) for transfer unit.

ACK used/unused mode can be selected as protocol (only for DAM in dual address mode)

Supports dual address/mode single address mode (only SH4).

Supports cycle steel/burst.

Supports local display list transfer.

Interrupt

Vertical (frame) synchronous detection

Field synchronous detection

External synchronous error detection

Drawing command error

Drawing command execution end

1.2.2 External memory interface

LIME can connect SDRAM that data bus width is 32 bits.

Max. 133 MHz is available for operating frequency.

Connectable memory configuration is as shown below.

External Memory Configuration

Type	Data bus width	Use count	Total capacity
SDRAM 64 Mbits (x32 Bits)	32 Bits	1	8 Mbytes
SDRAM 64 Mbits (x16 Bits)	32 Bits	2	16 Mbytes
SDRAM 128 Mbits (x32 Bits)	32 Bits	1	16 Mbytes
SDRAM 128 Mbits (x16 Bits)	32 Bits	2	32 Mbytes
SDRAM 256 Mbits (x32 Bits)	32 Bits	1	32 Mbytes
SDRAM 256 Mbits (x16 Bits)	32 Bits	2	64 Mbytes
SDRAM 512 Mbits (x32 Bits)	32 Bits	1	64 Mbytes

Please note that EMRS of SDRAM is not supported by LIME.

1.2.3 Display controller

Video data output

Only digital RGB video output is provided.

Screen resolution

LCD panels with wide range of resolutions are supported by using a programmable timing generator as follows:

Screen Resolutions

Resolutions
1280 × 768
1024 × 768
1024 × 600
800 × 600
854 × 480
640 × 480
480 × 234
400 × 234
320 × 234

Note:

These resolutions are mentioned for the sake of giving examples. In practice, any resolution corresponding to a pixel clock value of up to 80MHz can be supported. Note that higher resolution increases memory bandwidth consumption.

Hardware cursor

The LIME GDC supports two hardware cursor functions. Each of these hardware cursors is specified as a 64 × 64-pixel area. Each pixel of these hardware cursors is 8 bits and uses the same look-up table as indirect color mode.

Double buffer method

Double buffer method in which drawing window and display window is switched in units of 1 frame enables the smooth animation.

Flipping (switching of display window area) is performed in synchronization with the vertical blanking period using program.

Scroll method

Independent setting of drawing and display windows and their starting position enables the smooth scrolling.

Display colors

Supports indirect color mode which uses the look-up table (color palette) in 8 bits/pixels.

Entry for look-up table (color palette) corresponds to color code for 8 bits, in other words, 256. Color data is each 6 bits of RGB. Consequently, 256 colors can be displayed out of 260,000 colors.

Supports direct color mode which specifies RGB with 16 bits/pixels.

Supports direct color mode which specifies RGB with 24 bits/pixels.

Note:

Rendering is not supported in 24bpp color mode. The host CPU will have to write directly to the memory buffer in this color mode.

Overlay

Traditional compatibility mode

Up to four extra layers (C, W, M and B) can be displayed overlaid.

The overlay position for the hardware cursors is above/below the top layer (C).

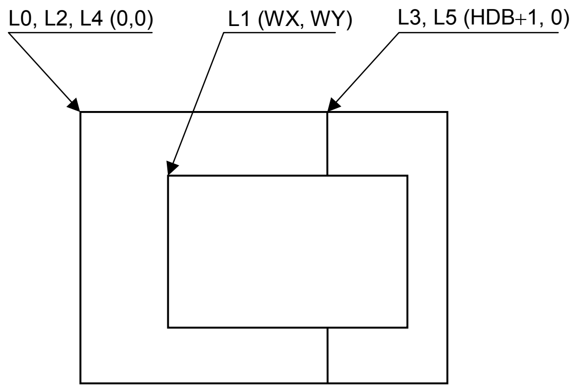
The transparent mode or the blend mode can be selected for overlay.

The M- and B-layers can be split into separate windows.

Window display can be performed for the W-layer.

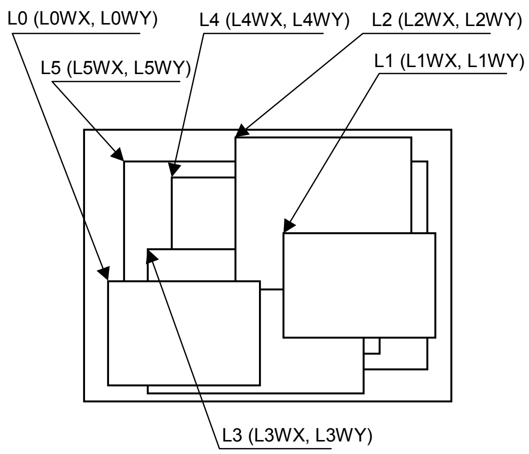
Two palettes are provided: C-layer and M-/B-layer.

The W-layer is used as the video input layer.



Window mode

- Up to six screens (L0 to 5) can be displayed overlaid.
- The overlay sequence of the L0- to L5-layers can be changed arbitrarily.
- The overlay position for the hardware cursors is above/below the L0-layer.
- The transparent mode or the blend mode can be selected for overlay.
- The L5-layer can be used as the blend coefficient plane (8 bits/pixel).
- Window display can be performed for all layers.
- Four palettes corresponded to L0 to 3 are provided.
- The L1-layer is used as the video input layer.
- Background color display is supported in window display for all layers.



1.2.4 2D Drawing

2D Primitives

The LIME GDC can perform 2D drawing for graphics memory (drawing plane) in direct color mode or indirect color mode.

Bold lines with width and broken lines can be drawn. With anti-aliasing smooth diagonal lines also can be drawn.

A triangle can be tiled in a single color or 2D pattern (tiling), or mapped with a texture pattern by specifying coordinates of the 2D pattern at each vertex (texture mapping). At texture mapping, drawing/non-drawing can be set in pixel units. Moreover, transparent processing can be performed using alpha blending. When drawing in single color or tiling without Gouraud shading or texture mapping, 2D Line with XY setup and 2D Triangle with XY setup can be used. Only vertex coordinates are set for these primitives. 2D Triangle with XY setup is also used to draw polygons.

2D Primitives

Primitive type	Description
Point	Plots point
Line	Draws line
Triangle	Draws triangle
2D Line with XY setup	Draws lines Compared to line, this reduces the host CPU processing load.
2D Triangle with XY setup	Draws ltriangles Compared to tiangle, this reduces the host CPU processing load.
Arbitrary polygon	Draws arbitrary closed polygon containing concave shapes consisting of vertices

Arbitrary polygon drawing

Using this function, arbitrary closed polygon containing concave shapes consisting of vertices can be drawn. (There is no restriction on the count of vertices, however, the polygon with its sides crossed are not supported.) In this case, as a work area for drawing, polygon drawing flag buffer is used on the graphics memory. In drawing polygon, draw triangle for polygon drawing flag buffer using 2D Triangle with XY setup. Decide any vertex as a starting point to draw triangle along the periphery. It enables you to draw final polygon form in single color or with tiling.

BLT/Rectangle drawing

This function draws a rectangle using logic operations. It is used to draw pattern and copy the image pattern within the drawing frame. It is also used for clearing drawing frame and Z buffer.

BLT Attributes

Attribute	Description
Raster operation	Selects two source logical operation mode
Transparent processing	Performs BLT without drawing pixel consistent with the transparent color.
Alpha blending	The alpha map and source in the memory is subjected to alpha blending and then copied to the destination.

Pattern (Text) drawing

This function draws a binary pattern (text) in a specified color.

Pattern (Text) Drawing Attributes

Attribute	Description
Enlarge	Vertically $\times$ 2 Horizontally $\times$ 2 Vertically and Horizontally $\times$ 2
Shrink	Vertically $\times$ 1/2 Horizontally 1/2 Vertically and Horizontally 1/2

Drawing clipping

This function sets a rectangle frame in drawing frame to prohibit the drawing of the outside the frame.

Hidden plane management (Optional function)

LIME GDC supports the Z buffer for hidden plane management as a optional function.

1.2.5 Special effects

Anti-aliasing

Anti-aliasing manipulates line borders of polygons in sub-pixel units and blend the pre-drawing pixel color with color to make the jaggies be seen smooth. It is used as a functional option for 2D drawing (in direct color mode only).

Bold line and broken line drawing

This function draws lines of a specific width and a broken line.

Line Drawing Attributes

Attribute	Description
Line width	Selectable from 1 to 32 pixels
Broken line	Set by 32 bit or 24 bit of broken line pattern

Not support the Anti-aliasing of dashed line patterns.

Alpha blending

Alpha blending blends two image colors to provide a transparent effect. LIME GDC supports two types of blending; blending two different colors at drawing, and blending overlay planes at display. Transparent color is not used for these blending options.

Set a transparent coefficient to the register; the transparent coefficient is applied for transparency processing of one plane.

In addition to the above, the following settings can be performed at texture mapping. When the most significant bit of each texture cell is 1, drawing or transparency can be set. When the most significant bit of each texture cell is 0, non-drawing can be set.

Alpha Blending

Type	Description
Drawing	Transparent ratio set in particular register While one primitive (polygon, pattern, etc.), being drawn, registered transparent ratio applied
Overlay display	Blends top layer pixel color with lower layer pixel color Transparent coefficient set in particular register Registered transparent coefficient applied during one frame scan

Gouraud Shading

Gouraud shading can be used in the direct color mode to provide real shading and color gradation.

Texture mapping

LIME GDC supports texture mapping to map an image pattern onto the surface of plane. The texture pattern can be laid out in the graphics memory. In this case, max. 4096 × 4096 pixels can be used.

Drawing of 8-/16- direct color is supported for the texture pattern. For drawing 8-bit direct color, only point sampling can be specified for texture interpolation; only de-curl can be specified for the blend mode.

Texture Mapping

Function	Description
Filtering	Point sample Bi-linear filter
Coordinates correction	Linear
Blend	De-curl Modulate Stencil
Alpha blend	Normal Stencil Stencil alpha
Wrap	Repeat Clamp Border

2 Pins

2.1 Pin assignment diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	VSS	VINF	VINVS	BI0	BI3	GI0	GI3	RI0	RI3	BO4	BO0	GO4	GO0	RO5	RO2	DCLKO	VSS	DCLKI	VSYNC	VSS
B	RGBCK	VSS	VINHS	BI1	BI4	GI1	GI4	RI1	RI4	BO5	BO1	GO5	GO1	RO6	RO3	RO0	HSYNC	CSYNC	VSS	GMOD0
C	XPLLT	XTST	VSS	BI2	BI5	GI2	GI5	RI2	RI5	BO6	BO2	GO6	GO2	RO7	RO4	RO1	DISP	VSS	GMOD1	GMOD2
D	XSM	SCL	SDA	VSS	VDDE	VDDE	VDDI	VDDE	VDDE	BO7	BO3	GO7	GO3	VDDI	VDDE	VDDE	VSS	GV	D31	D30
E	MD0	MD1	MD2	VDDE													VDDE	D29	D28	D27
F	MD3	MD4	MD5	VDDE													VDDE	D26	D25	D24
G	MD6	MD7	MD8	VDDI			VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VSS			VDDI	D23	D22	D21
H	MD9	MD10	MD11	VDDE			VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VSS			VDDE	D20	D19	D18
J	MD12	MD13	MD14	VDDE			VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VSS			VDDE	D17	D16	D15
K	MD15	MD16	MD17	MD18			VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VSS			VDDE	D14	D13	D12
L	MD19	MD20	MD21	VDDE			VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VSS			D11	D10	D9	D8
M	MD22	MD23	MD24	VDDE			VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VSS			VDDE	D7	D6	D5
N	MD25	MD26	MD27	VDDE			VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VSS			VDDE	D4	D3	D2
P	MD28	MD29	MD30	VDDI			VDDI	VDDI	VDDI	VDDI	VDDI	VSS	VSS	VSS			VDDI	D1	D0	DRACK
R	MD31	MDQM	MDQM	VDDE			TOP VIEW										VDDE	DTACK	XWE3	XWE2
T	MCLKI	MDQM	MDQM	VDDE													VDDE	XWE1	XWE0	A23
U	VSS	MA0	MA1	VSS	VDDE	VDDE	VDDI	PLLVS	PLLVD	MODE0	XINT	VDDE	VDDE	VDDI	VDDE	VDDE	VSS	A22	A21	A20
V	MCLKO	MA2	VSS	MA9	MA12	MRAS	CLKS0	XRST	CLKS1	BS_M	XRDY	XRD	A1	A4	A7	A10	A13	VSS	A19	A18
W	MA3	VSS	MA6	MA8	MA11	MA14	MWE	CKM	S	RDY_M	MODE1	XCS	A0	A3	A6	A9	A12	A15	VSS	A17
Y	VSS	MA4	MA5	MA7	MA10	MA13	MCAS	CLK	VPD	BCLKI	MODE2	DREQ	XBS	A2	A5	A8	A11	A14	A16	VSS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	1	76	75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58
B	2	77	144	143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128	57
C	3	78	145	204	203	202	201	200	199	198	197	196	195	194	193	192	191	190	127	56
D	4	79	146	205	256	255	254	253	252	251	250	249	248	247	246	245	244	189	126	55
E	5	80	147	206													243	188	125	54
F	6	81	148	207													242	187	124	53
G	7	82	149	208			257	284	283	282	281	280	279	278			241	186	123	52
H	8	83	150	209			258	285	304	303	302	301	300	277			240	185	122	51
J	9	84	151	210			259	286	305	316	315	314	299	276			239	184	121	50
K	10	85	152	211			260	287	306	317	320	313	298	275			238	183	120	49
L	11	86	153	212			261	288	307	318	319	312	297	274			237	182	119	48
M	12	87	154	213			262	289	308	309	310	311	296	273			236	181	118	47
N	13	88	155	214			263	290	291	292	293	294	295	272			235	180	117	46
P	14	89	156	215			264	265	266	267	268	269	270	271			234	179	116	45
R	15	90	157	216			TOP VIEW										233	178	115	44
T	16	91	158	217													232	177	114	43
U	17	92	159	218	219	220	221	222	223	224	225	226	227	228	229	230	231	176	113	42
V	18	93	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	112	41
W	19	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	40
Y	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39

2.2 Pin assignment table

Pin Number	JEDEC Number		Name	Pin Number	JEDEC Number		Name	Pin Number	JEDEC Number		Name	Pin Number	JEDEC Number		Name
1	A	1	VSS	65	A	13	GO0	129	B	18	CSYNC	193	C	15	RO4
2	B	1	RGBCK	66	A	12	GO4	130	B	17	HSYNC	194	C	14	RO7
3	C	1	XPLLT	67	A	11	BO0	131	B	16	RO0	195	C	13	GO2
4	D	1	XSM	68	A	10	BO4	132	B	15	RO3	196	C	12	GO6
5	E	1	MD0	69	A	9	RI3	133	B	14	RO6	197	C	11	BO2
6	F	1	MD3	70	A	8	RI0	134	B	13	GO1	198	C	10	BO6
7	G	1	MD6	71	A	7	GI3	135	B	12	GO5	199	C	9	RI5
8	H	1	MD9	72	A	6	GI0	136	B	11	BO1	200	C	8	RI2
9	J	1	MD12	73	A	5	BI3	137	B	10	BO5	201	C	7	GI5
10	K	1	MD15	74	A	4	BI0	138	B	9	RI4	202	C	6	GI2
11	L	1	MD19	75	A	3	VINVS	139	B	8	RI1	203	C	5	BI5
12	M	1	MD22	76	A	2	VINF	140	B	7	GI4	204	C	4	BI2
13	N	1	MD25	77	B	2	VSS	141	B	6	GI1	205	D	4	VSS
14	P	1	MD28	78	C	2	XTST	142	B	5	BI4	206	E	4	VDDE
15	R	1	MD31	79	D	2	SCL	143	B	4	BI1	207	F	4	VDDE
16	T	1	MCLKI	80	E	2	MD1	144	B	3	VINHS	208	G	4	VDDI
17	U	1	VSS	81	F	2	MD4	145	C	3	VSS	209	H	4	VDDE
18	V	1	MCLKO	82	G	2	MD7	146	D	3	SDA	210	J	4	VDDE
19	W	1	MA3	83	H	2	MD10	147	E	3	MD2	211	K	4	MD18
20	Y	1	VSS	84	J	2	MD13	148	F	3	MD5	212	L	4	VDDE
21	Y	2	MA4	85	K	2	MD16	149	G	3	MD8	213	M	4	VDDE
22	Y	3	MA5	86	L	2	MD20	150	H	3	MD11	214	N	4	VDDE
23	Y	4	MA7	87	M	2	MD23	151	J	3	MD14	215	P	4	VDDI
24	Y	5	MA10	88	N	2	MD26	152	K	3	MD17	216	R	4	VDDE
25	Y	6	MA13	89	P	2	MD29	153	L	3	MD21	217	T	4	VDDE
26	Y	7	MCAS	90	R	2	MDQM0	154	M	3	MD24	218	U	4	VSS
27	Y	8	CLK	91	T	2	MDQM2	155	N	3	MD27	219	U	5	VDDE
28	Y	9	VSS	92	U	2	MA0	156	P	3	MD30	220	U	6	VDDE
29	Y	10	BCLKI	93	V	2	MA2	157	R	3	MDQM1	221	U	7	VDDI
30	Y	11	MODE1	94	W	2	VSS	158	T	3	MDQM3	222	U	8	PLLVS
31	Y	12	DREQ	95	W	3	MA6	159	U	3	MA1	223	U	9	PLLVD
32	Y	13	XBS	96	W	4	MA8	160	V	3	VSS	224	U	10	MODE0
33	Y	14	A2	97	W	5	MA11	161	V	4	MA9	225	U	11	XINT
34	Y	15	A5	98	W	6	MA14	162	V	5	MA12	226	U	12	VDDE
35	Y	16	A8	99	W	7	MWE	163	V	6	MRAS	227	U	13	VDDE
36	Y	17	A11	100	W	8	CKM	164	V	7	CLKS0	228	U	14	VDDI
37	Y	18	A14	101	W	9	S	165	V	8	XRST	229	U	15	VDDE
38	Y	19	A16	102	W	10	RDY_M	166	V	9	CLKS1	230	U	16	VDDE
39	Y	20	VSS	103	W	11	MODE2	167	V	10	BS_M	231	U	17	VSS
40	W	20	A17	104	W	12	XCS	168	V	11	XRDY	232	T	17	VDDE
41	V	20	A18	105	W	13	A0	169	V	12	XRD	233	R	17	VDDE
42	U	20	A20	106	W	14	A3	170	V	13	A1	234	P	17	VDDI
43	T	20	A23	107	W	15	A6	171	V	14	A4	235	N	17	VDDE
44	R	20	XWE2	108	W	16	A9	172	V	15	A7	236	M	17	VDDE
45	P	20	DRACK	109	W	17	A12	173	V	16	A10	237	L	17	D11
46	N	20	D2	110	W	18	A15	174	V	17	A13	238	K	17	VDDE
47	M	20	D5	111	W	19	VSS	175	V	18	VSS	239	J	17	VDDE
48	L	20	D8	112	V	19	A19	176	U	18	A22	240	H	17	VDDE
49	K	20	D12	113	U	19	A21	177	T	18	XWE1	241	G	17	VDDI
50	J	20	D15	114	T	19	XWE0	178	R	18	DTACK	242	F	17	VDDE
51	H	20	D18	115	R	19	XWE3	179	P	18	D1	243	E	17	VDDE
52	G	20	D21	116	P	19	D0	180	N	18	D4	244	D	17	VSS
53	F	20	D24	117	N	19	D3	181	M	18	D7	245	D	16	VDDE
54	E	20	D27	118	M	19	D6	182	L	18	D10	246	D	15	VDDE
55	D	20	D30	119	L	19	D9	183	K	18	D14	247	D	14	VDDI
56	C	20	GMOD2	120	K	19	D13	184	J	18	D17	248	D	13	GO3
57	B	20	GMOD0	121	J	19	D16	185	H	18	D20	249	D	12	GO7
58	A	20	VSS	122	H	19	D19	186	G	18	D23	250	D	11	BO3
59	A	19	VSYNC	123	G	19	D22	187	F	18	D26	251	D	10	BO7
60	A	18	DCLKI	124	F	19	D25	188	E	18	D29	252	D	9	VDDE
61	A	17	VSS	125	E	19	D28	189	D	18	GV	253	D	8	VDDE
62	A	16	DCLKO	126	D	19	D31	190	C	18	VSS	254	D	7	VDDI
63	A	15	RO2	127	C	19	GMOD1	191	C	17	DISP	255	D	6	VDDE
64	A	14	RO5	128	B	19	VSS	192	C	16	RO1	256	D	5	VDDE

Pin Number	JEDEC Number		Name
257	G	7	VDDI
258	H	7	VDDI
259	J	7	VDDI
260	K	7	VDDI
261	L	7	VDDI
262	M	7	VDDI
263	N	7	VDDI
264	P	7	VDDI
265	P	8	VDDI
266	P	9	VDDI
267	P	10	VDDI
268	P	11	VDDI
269	P	12	VSS
270	P	13	VSS
271	P	14	VSS
272	N	14	VSS
273	M	14	VSS
274	L	14	VSS
275	K	14	VSS
276	J	14	VSS
277	H	14	VSS
278	G	14	VSS
279	G	13	VSS
280	G	12	VSS
281	G	11	VSS
282	G	10	VSS
283	G	9	VSS
284	G	8	VSS
285	H	8	VSS
286	J	8	VSS
287	K	8	VSS
288	L	8	VSS
289	M	8	VSS
290	N	8	VSS
291	N	9	VSS
292	N	10	VSS
293	N	11	VSS
294	N	12	VSS
295	N	13	VSS
296	M	13	VSS
297	L	13	VSS
298	K	13	VSS
299	J	13	VSS
300	H	13	VSS
301	H	12	VSS
302	H	11	VSS
303	H	10	VSS
304	H	9	VSS
305	J	9	VSS
306	K	9	VSS
307	L	9	VSS
308	M	9	VSS
309	M	10	VSS
310	M	11	VSS
311	M	12	VSS
312	L	12	VSS
313	K	12	VSS
314	J	12	VSS
315	J	11	VSS
316	J	10	VSS
317	K	10	VSS
318	L	10	VSS
319	L	11	VSS
320	K	11	VSS

Group	Symbol	description
GND group:	**VSS/PLLVSS/Low**	**Ground**
	TESTL	**Connect Ground.**
1.8V group:	**VDDL/VDDI**	**1.8-V power supply**
	PLLVDD	**PLL power supply (1.8 V)**
3.3V group:	**VDDH/VDDE**	**3.3-V power supply**
	TESTH	**Input a 3.3 V-power supply**

2.3 Pin mutiplex table

BGA Pin No.	PAD No.		pin name (GMODE[2:0]=0)	Func	I/O	DISP/CAP-MUX GMODE[2:0]			Host I/F MODE[2:0]		
						0x1	0x2	0x3	16bit	16bit AD-MUX	32bit AD-MUX
A2	1	1	VINFID	CAP	I						
A3	2	2	VINVSYNC	CAP	I						
B3	3	3	VINHSYNC	CAP	I						
B1	5	4	RGBCLK	CAP	I						
C1	8	5	TESTH	TEST	I	VDDE	VDDE	VDDE	VDDE	VDDE	VDDE
C2	9	6	TESTH	TEST	I	VDDE	VDDE	VDDE	VDDE	VDDE	VDDE
D1	10	7	TESTH	TEST	I	VDDE	VDDE	VDDE	VDDE	VDDE	VDDE
D2	11	8	SCL	I2C	IO						
D3	12	9	SDA	I2C	IO						
E1	16	10	MD0	MEC	IO						
E2	17	11	MD1	MEC	IO						
E3	18	12	MD2	MEC	IO						
F1	19	13	MD3	MEC	IO						
F2	23	14	MD4	MEC	IO						
F3	24	15	MD5	MEC	IO						
G1	25	16	MD6	MEC	IO						
G2	26	17	MD7	MEC	IO						
G3	27	18	MD8	MEC	IO						
H1	28	19	MD9	MEC	IO						
H2	29	20	MD10	MEC	IO						
H3	30	21	MD11	MEC	IO						
J1	31	22	MD12	MEC	IO						
J2	32	23	MD13	MEC	IO						
J3	34	24	MD14	MEC	IO						
K1	35	25	MD15	MEC	IO						
K2	36	26	MD16	MEC	IO						
K3	37	27	MD17	MEC	IO						
K4	38	28	MD18	MEC	IO						
L1	39	29	MD19	MEC	IO						
L2	40	30	MD20	MEC	IO						
L3	41	31	MD21	MEC	IO						
M1	42	32	MD22	MEC	IO						
M2	43	33	MD23	MEC	IO						
M3	47	34	MD24	MEC	IO						
N1	48	35	MD25	MEC	IO						
N2	49	36	MD26	MEC	IO						
N3	50	37	MD27	MEC	IO						
P1	51	38	MD28	MEC	IO						
P2	52	39	MD29	MEC	IO						
P3	53	40	MD30	MEC	IO						
R1	54	41	MD31	MEC	IO						
T1	58	42	MCLKI	MEC	I						
V1	60	43	MCLKO	MEC	O						
R2	62	44	MDQM0	MEC	O						
R3	63	45	MDQM1	MEC	O						
T2	64	46	MDQM2	MEC	O						
T3	65	47	MDQM3	MEC	O						
U2	66	48	MA0	MEC	O						
U3	67	49	MA1	MEC	O						

BGA Pin No.	PAD No.		pin name (GMODE[2:0]=0)	Func	I/O	DISP/CAP-MUX GMODE[2:0]			Host I/F MODE[2:0]		
						0x1	0x2	0x3	16bit	16bit AD-MUX	32bit AD-MUX
V2	68	50	MA2	MEC	O						
W1	69	51	MA3	MEC	O						
Y2	72	52	MA4	MEC	O						
Y3	73	53	MA5	MEC	O						
W3	74	54	MA6	MEC	O						
Y4	75	55	MA7	MEC	O						
W4	76	56	MA8	MEC	O						
V4	77	57	MA9	MEC	O						
Y5	78	58	MA10	MEC	O						
W5	79	59	MA11	MEC	O						
V5	81	60	MA12	MEC	O						
Y6	82	61	MA13	MEC	O						
W6	83	62	MA14	MEC	O						
V6	86	63	MRAS	MEC	O						
Y7	87	64	MCAS	MEC	O						
W7	88	65	MWE	MEC	O						
V7	91	66	CLKSEL0	CLOCK	I						
W8	92	67	CKM	CLOCK	I						
V8	93	68	XRST	Host I/F	I						
U8	94	69	PLLVSS	CLOCK	I						
Y8	95	70	CLK	CLOCK	I						
W9	96	71	S	CLOCK	I						
U9	97	72	PLLVDD	CLOCK	I						
V9	98	73	CLKSEL1	CLOCK	I						
W10	100	74	RDY_MODE	Host I/F	I				Low	Low	Low
V10	101	75	BS_MODE	Host I/F	I						
Y9	103	76	TESTL	TEST	I	VSS	VSS	VSS	VSS	VSS	VSS
U10	104	77	MODE0	Host I/F	I				Low	High	Low
Y11	105	78	MODE1	Host I/F	I				Low	Low	High
W11	106	79	MODE2	Host I/F	I				High	High	High
V11	109	80	XRDY	Host I/F	O(T)						
U11	110	81	XINT	Host I/F	O						
Y12	111	82	DREQ	Host I/F	O						
Y10	114	83	BCLKI	Host I/F	I						
W12	116	84	XCS	Host I/F	I						
V12	117	85	XRD	Host I/F	I						
Y13	118	86	XBS	Host I/F	I				Input Low when unused.		
W13	119	87	A0	Host I/F	I				A1	Low	Low
V13	120	88	A1	Host I/F	I				A2	Low	Low
Y14	121	89	A2	Host I/F	I				A3	Low	Low
W14	122	90	A3	Host I/F	I				A4	Low	Low
V14	126	91	A4	Host I/F	IO				A5	AD16	AD16
Y15	127	92	A5	Host I/F	IO				A6	AD17	AD17
W15	128	93	A6	Host I/F	IO				A7	AD18	AD18
V15	129	94	A7	Host I/F	IO				A8	AD19	AD19
Y16	130	95	A8	Host I/F	IO				A9	AD20	AD20
W16	131	96	A9	Host I/F	IO				A10	AD21	AD21
V16	132	97	A10	Host I/F	IO				A11	AD22	AD22
Y17	133	98	A11	Host I/F	IO				A12	AD23	AD23
W17	134	99	A12	Host I/F	IO				A13	Low	AD24
V17	138	100	A13	Host I/F	IO				A14	Low	AD25
Y18	139	101	A14	Host I/F	IO				A15	Low	AD26
W18	140	102	A15	Host I/F	IO				A16	Low	AD27

BGA Pin No.	PAD No.		pin name (GMODE[2:0]=0)	Func	I/O	DISP/CAP-MUX GMODE[2:0]			Host I/F MODE[2:0]		
						0x1	0x2	0x3	16bit	16bit AD-MUX	32bit AD-MUX
Y19	141	103	A16	Host I/F	IO				A17	Low	AD28
W20	142	104	A17	Host I/F	IO				A18	Low	AD29
V20	143	105	A18	Host I/F	IO				A19	Low	AD30
V19	144	106	A19	Host I/F	IO				A20	Low	AD31
U20	147	107	A20	Host I/F	I				A21	Low	Low
U19	148	108	A21	Host I/F	I				A22	Low	Low
U18	149	109	A22	Host I/F	I				A23	Low	Low
T20	150	110	A23	Host I/F	I				Low	Low	Low
T19	151	111	XWE0	Host I/F	I						
T18	152	112	XWE1	Host I/F	I						
R20	153	113	XWE2	Host I/F	I				RDYSW	RDYSW	RDYSW
R19	154	114	XWE3	Host I/F	I				ENDIAN	ENDIAN	Low
R18	155	115	DTACK	Host I/F	I				Input Low when unused.		
P20	156	116	DRACK	Host I/F	I				Input Low when unused.		
P19	160	117	D0	Host I/F	IO				D0	AD0	AD0
P18	161	118	D1	Host I/F	IO				D1	AD1	AD1
N20	162	119	D2	Host I/F	IO				D2	AD2	AD2
N19	163	120	D3	Host I/F	IO				D3	AD3	AD3
N18	164	121	D4	Host I/F	IO				D4	AD4	AD4
M20	165	122	D5	Host I/F	IO				D5	AD5	AD5
M19	166	123	D6	Host I/F	IO				D6	AD6	AD6
M18	167	124	D7	Host I/F	IO				D7	AD7	AD7
L20	171	125	D8	Host I/F	IO				D8	AD8	AD8
L19	172	126	D9	Host I/F	IO				D9	AD9	AD9
L18	173	127	D10	Host I/F	IO				D10	AD10	AD10
L17	174	128	D11	Host I/F	IO				D11	AD11	AD11
K20	175	129	D12	Host I/F	IO				D12	AD12	AD12
K19	176	130	D13	Host I/F	IO				D13	AD13	AD13
K18	178	131	D14	Host I/F	IO				D14	AD14	AD14
J20	179	132	D15	Host I/F	IO				D15	AD15	AD15
J19	184	133	D16	Host I/F	IO	D16	SR00	SR02			
J18	185	134	D17	Host I/F	IO	D17	SR01	SR03			
H20	186	135	D18	Host I/F	IO	D18	SR02	SR04			
H19	187	136	D19	Host I/F	IO	D19	SR03	SR05			
H18	188	137	D20	Host I/F	IO	D20	SR04	SR06			
G20	189	138	D21	Host I/F	IO	D21	SR05	SR07			
G19	191	139	D22	Host I/F	IO	D22	SR06	SG02			
G18	192	140	D23	Host I/F	IO	D23	SR07	SG03			
F20	193	141	D24	Host I/F	IO	D24	SG00	SG04			
F19	194	142	D25	Host I/F	IO	D25	SG01	SG05			
F18	195	143	D26	Host I/F	IO	D26	SG02	SG06			
E20	196	144	D27	Host I/F	IO	D27	SG03	SG07			
E19	197	145	D28	Host I/F	IO	D28	SG04	SB02			
E18	198	146	D29	Host I/F	IO	D29	SG05	SB03			
D20	202	147	D30	Host I/F	IO	D30	SG06	SB04			
D19	203	148	D31	Host I/F	IO	D31	SG07	SB05			
C20	206	149	GMODE2	Others	I	Low	Low	Low			
C19	207	150	GMODE1	Others	I	Low	High	High			
B20	208	151	GMODE0	Others	I	High	Low	High			

BGA Pin No.	PAD No.		pin name (GMODE[2:0]=0)	Func	I/O	DISP/CAP-MUX GMODE[2:0]			Host I/F MODE[2:0]		
						0x1	0x2	0x3	16bit	16bit AD-MUX	32bit AD-MUX
D18	209	152	GV	DISP	O						
C17	202	153	DISPE	DISP	O						
B18	213	154	CSYNC	DISP	O						
A19	214	155	VSYNC	DISP	IO						
B17	215	156	HSYNC	DISP	IO						
A18	218	157	DCLKI	DISP	I						
A16	220	158	DCLKO	DISP	O						
B16	223	159	RO0	DISP	O	RO0	SBO0	SBO6			
C16	224	160	RO1	DISP	O	RO1	SBO1	SBO7			
A15	226	161	RO2	DISP	O	RO2	SBO2	RO2			
B15	227	162	RO3	DISP	O	RO3	SBO3	RO3			
C15	228	163	RO4	DISP	O	RO4	SBO4	RO4			
A14	229	164	RO5	DISP	O	RO5	SBO5	RO5			
B14	230	165	RO6	DISP	O	RO6	SBO6	RO6			
C14	233	166	RO7	DISP	O	RO7	SBO7	RO7			
A13	234	167	GO0	DISP	O	GO0	RO2	GO2			
B13	236	168	GO1	DISP	O	GO1	RO3	GO3			
C13	237	169	GO2	DISP	O	GO2	RO4	GO4			
D13	238	170	GO3	DISP	O	GO3	RO5	GO5			
A12	239	171	GO4	DISP	O	GO4	RO6	GO6			
B12	240	172	GO5	DISP	O	GO5	RO7	GO7			
C12	241	173	GO6	DISP	O	GO6	GO2	BO2			
D12	242	174	GO7	DISP	O	GO7	GO3	BO3			
A11	245	175	BO0	DISP	O	BO0	GO4	BO4			
B11	246	176	BO1	DISP	O	BO1	GO5	BO5			
C11	247	177	BO2	DISP	O	BO2	GO6	BO6			
D11	249	178	BO3	DISP	O	BO3	GO7	BO7			
A10	250	179	BO4	DISP	O	BO4	BO2				
B10	251	180	BO5	DISP	O	BO5	BO3				
C10	252	181	BO6	DISP	O	BO6	BO4				
D10	253	182	BO7	DISP	O	BO7	BO5				
C9	259	183	RI5	CAP	I/O	GPIO0	BO6	RI5			
B9	260	184	RI4	CAP	I/O	GPIO1	BO7	RI4			
A9	261	185	RI3	CAP	I/O	GPIO2	GPIO0	RI3			
C8	262	186	RI2	CAP	I/O	GPIO3	GPIO1	RI2			
B8	263	187	RI1	CAP	I/O	GPIO4	GPIO2	RI1			
A8	266	188	RI0	CAP	I			RI0			
C7	267	189	GI5	CAP	I			GI5			
B7	268	190	GI4	CAP	I			GI4			
A7	269	191	GI3	CAP	I			GI3			
C6	270	192	GI2	CAP	I			GI2			
B6	274	193	GI1	CAP	I	VIN7	VIN7	GI1			
A6	275	194	GI0	CAP	I	VIN6	VIN6	GI0			
C5	276	195	BI5	CAP	I	VIN5	VIN5	BI5			
B5	277	196	BI4	CAP	I	VIN4	VIN4	BI4			
A5	279	197	BI3	CAP	I	VIN3	VIN3	BI3			
C4	280	198	BI2	CAP	I	VIN2	VIN2	BI2			
B4	281	199	BI1	CAP	I	VIN1	VIN1	BI1			
A4	282	200	BI0	CAP	I	VIN0	VIN0	BI0			

2.4 Host CPU interface

1) Parallel interface mode

Table 2-1 Host CPU Interface Pins

Pin name	I/O	Description
MODE0-2	Input	Host CPU mode select
RDY_MODE	Input	Normally ready, Not ready select
BS_MODE	Input	BS signal with/without select
XRST	Input	Hardware reset (“L”=Reset, Set to low level when power-on)
D0-31	In/Out	Host CPU bus data
A0-A23	Input	Host CPU bus address (In the V832 mode, A[24] is connected to XMWR.)
BCLKI	Input	Host CPU bus clock
XBS	Input	Bus cycle start signal
XCS	Input	Chip select signal
XRD	Input	Read strobe signal
XWE0	Input	Write strobe for D0 to D7 signal
XWE1	Input	Write strobe for D8 to D15 signal
XWE2	Input	Write strobe for D16 to D23 signal
XWE3	Input	Write strobe for D24 to D31 signal
XRDY	Output Tri-state *(1)	Wait request signal (In the SH3 mode, when this signal is “0”, it indicates the wait state; in the SH4, V832 and SPARClite modes, when this signal is “1”, it indicates the wait state.)
DREQ	Output	DMA request signal (This signal is low-active in both the SH mode and V832 mode.)
DRACK/DMAAK	Input	Acknowledge signal in response to DMA request (DMAAK is used in the V832 mode; this signal is high-active in both the SH mode and V832 mode.)
DTACK/XTC	Input	DMA transfer strobe signal (XTC is used in the V832 mode. In the SH mode, this signal is high-active; in the V832 mode, it is low-active.)
XINT	Output	Interrupt signal issued to host CPU (In the SH mode, and SPARClite this signal is low-active; in the V832 mode, it is high-active)

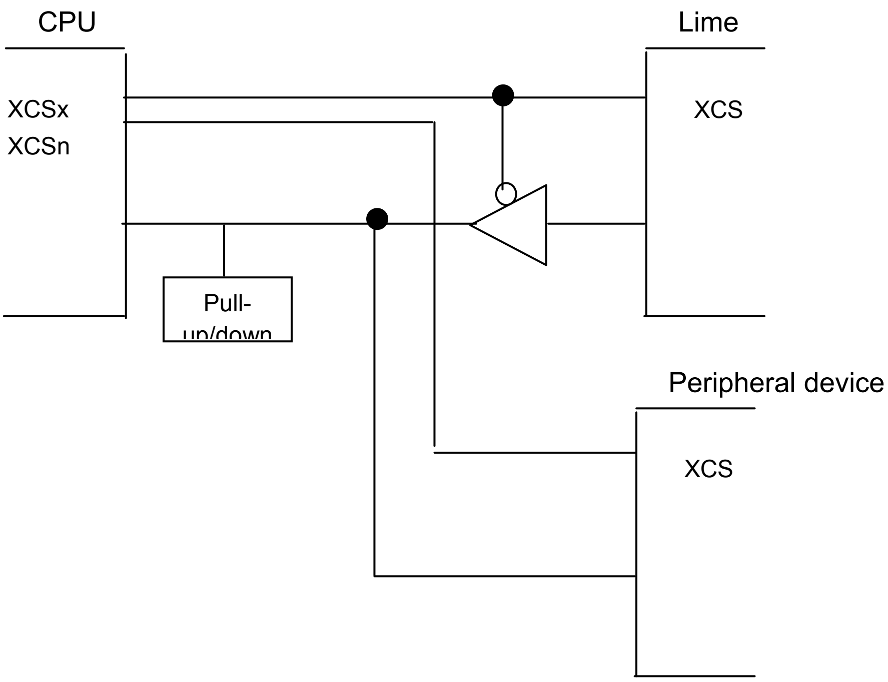
With regard to BCLKI and XRST, the details, please refer “14.3.2 Note at power-on”.

*(1) Tri-state output of XRDY is valid in SH3, SH4, V832, and SPARClite. In 16-bit SRAM I/F, 16-bit AD I/F, and 32-bit AD I/F, it drives “High” or “Low”. When more than two devices are connected to 16-bit SRAM I/F, 16-bit AD I/F, and 32-bit AD I/F, insert the tri-state buffer between XRDY of LIME and the CPU. Refer to the following note.

Case 1:
If there is no peripheral device to drive the hardware wait and it is possible for the CPU to ignore the XRDY signal in other than from Lime, then it is not necessary to account for this problem. Simply connect the XRDY of Lime to the XRDY of the CPU.

Case 2:

If the condition is other than the above, put the tri-state buffer between Lime's XRDY and CPU's XRDY as shown below.



LIME can be connected to the Renesas SH4 (SH7750), SH3 (SH7709) NEC V832 and Fujitsu SPARClite (MB86833) without external circuit. In the SRAM interface mode, LIME can be used with any other CPU as well. The host CPU is specified by the MODE0 to 2 pins.

MODE 2	MODE 1	MODE 0	CPU
L	L	L	SH3
L	L	H	SH4
L	H	L	V832
L	H	H	SPARClite
H	L	L	General-purpose 16bit CPU with SRAM interface
H	L	H	General-porpose 16bit CPU with address and data multiplex interface
H	H	L	General-purpose 32bit CPU with address and data multiplex interface
H	H	H	Reserved

2.4.1 Ready signal mode

The MODE2 pin can be used to set the ready signal level when the bus cycle of the host CPU terminates. For the normally not ready mode, set the software wait to 0 or 1 cycles. When using this device in the normally ready mode, set the software wait to 2 cycles. When using this device in the normally not ready mode, set the software wait to one cycle. (When ***BS_MODE* = *H***, three cycles are needed for the software wait.)

The 'normally not ready mode' is the mode in which the LIME XRDY signal is always in the wait state and Ready is returned only when read/write is ready.

The 'normal ready mode' is the mode in which the LIME XRDY signal is always in the Ready state and it is put into the wait state only when read/write cannot be performed immediately.

Ready Signal Mode

RDY_MODE	Ready signal operation
L	Recognizes XRDY signal as 'not ready level' and terminates bus cycle (normally not ready mode)
H	Recognizes XRDY signal as 'ready level' and terminates bus cycle (normally ready mode)

RDYSW is for an active signal level on 16bit SRAM I/F, 16bit A/D multiplexed I/F, and 32bit A/D multiplexed I/F modes. High active or low active can be selected.

Active level of ready signal for 16bit CPU and A/D multiplexed CPU

RDYSW	RDYSW signal operation
L	Recognizes XRDY signal as 'not ready level' and terminates bus cycle (normally not ready mode)
H	Recognizes XRDY signal as 'ready level' and terminates bus cycle (normally ready mode)

2.4.2 BS signal mode

Connection to a CPU without the BS signal can be made via the ***BS_MODE*** signal. This setting can be performed for all CPU modes. To connect to a CPU without the BS signal, set the ***BS_MODE*** signal to "High" level.

When not using the BS signal, fix the BS pin of LIME at "High" level.

When using the ***BS_MODE*** signal as "High" level, with the normally ready mode established, set the CPU software wait to three cycles.

BS Signal Mode

BS_MODE	Operation of BS signal
L	Connects to CPU with BS signal
H	Connects to CPU without BS signal

2.4.3 Endian

LIME has bi-endian mode for a halfword ordering of 16bit CPU.

ENDIAN signal is for 16bit SRAM I/F and 16bit A/D multiplexed I/F modes.The half word ordering of Lime can be selected from either little or big.

In the case of CPUs with the byte swapping, please note it.

LIME operates in little-endian mode. All the register address descriptions in the specifications are byte address in little endian. When using a big-endian CPU, note that the byte-or word-addresses are different from these descriptions.

Endian Mode for 16-bit CPU

ENDIAN	Operation of BS signal
L	Little endian for the halfword ordering
H	Big endian for the halfword ordering

2.4.4 Note about the connection to CPU

The data signal is 32 bits (fixed).

The address signal is 32 bits (per one double-word) × 24, and has a 64-Mbyte address field. (16-MByte address space is provided for V832 and SPARClite.)

The external bus operating frequency is up to 66 MHz.

In the SH4, V832, and SPARClite modes, when the XRDY signal is low, it is in the ready state. However, in the SH3 mode, when the XRDY signal is low, it is in the wait state. This signal is a tri-state output that is synchronized with the rising edge of BCLKI.

DMA data transfer is supported using an external DMA controller.

An interrupt signal is generated to the host CPU.

The XRST input must be kept low for at least 300 μs after setting the S (PLL reset) signal to high.

In the V832 mode, LIME signals are connected to the V832 CPU as follows:

LIME Pins	V832 Signals
A24	XMWR
DTACK	XTC
DRACK	DMAAK

How to connect between Lime and CPUs is shown as the following table.

Pin name	In/Out	SH4(SH7750)	SH3(SH7709)	V832	V832
BCLKI	I	CKIO	CKIO	CLKOUT	CLKOUT
A3-A0	I	A5-A2	A5-A2	A5-A2	A5-A2
A11-A4	I	A13-A6	A13-A6	A13-A6	A13-A6
A19-A12	I	A21-A14	A21-A14	A21-A14	A21-A14
A21-A20	I	A23-A22	A23-A22	A23-A22	A23-A22
A22	I	A24	A24	-	-
A23	I	A25	A25	-	-
XCS	I	CSn	CSn	CSn	CSn
D15-0	IO	D15-D0	D15-D0	D15-D0	D15-D0
D31-16	IO	D31-D16	D31-D16	D31-D16	D31-D16
XRD	I	RD	RD	IORD/MRD	IORD/MRD
XWE0	I	WEn	WEn	IOWR/xxBEN/MWR	IOWR/xxBEN/MWR
XWE1	I				
XWE2	I				
XWE3	I				
XBS	I	BS	BS	BCYST	BCYST
XRDY	O	RDY	WAIT	READY	READY
DREQ	O	DREQ	DREQ	DMARQ	DMARQ
DRACK	I	DRAK	DRAK	DMAAK	DMAAK
DTACK	I	DACK	DACK	TC	TC
XINT	O				
MODE0-2	I				
RDY_MODE	I				
BS_MODE	I				

Pin name	In/Out	MB90F334	MB90F37x	MB91F46x (16-bit)	MB91F46x (32-bit)
BCLKI	I			SYSCLK	SYSCLK
A3-A0	I			A04-A01	A04-A01
A11-A4	I			A12-A05	A12-A05
A19-A12	I			A20-A13	A20-A13
A21-A20	I			A22-A21	A22-A21
A22	I			A23	A23
A23	I			-	-
XCS	I			CSnX	CSnX
D15-0	IO			D31-D16	D31-D16
D31-16	IO			-	-
XRD	I			IORDX	IORDX
XWE0	I			IOWRX	IOWRX
XWE1	I			-	-
XWE2	I			-	-
XWE3	I			-	-
XBS	I			ASX	ASX
XRDY	O			RDY	RDY
DREQ	O			-	-
DRACK	I			-	-
DTACK	I			-	-
XINT	O				
MODE0-2	I				
RDY_MODE	I				
BS_MODE	I				

Pin name	In/Out	MB90F38x 16-bit non-MUX
BCLKI	I	CLK
A0	I	Open
A8-A1	I	P11_7-P11_0
A15-A9	I	P12_6-P12_0
A20-A16	I	P03_3-P03_0
A23-A21	I	P08_6-P08_4
XCS	I	CS3
D7-D0	IO	P00_7-P00_0
D15-D8	IO	P02_7-P02_0
XRD	I	RDX
XWE0	I	WRLX
XWE1	I	WRHX
XWE2	I	-
XWE3	I	-
XBS	I	ALE / ASX
XRDY	O	RDY
DREQ	O	-
DRACK	I	-
DTACK	I	-
XINT	O	-
MODE0	I	GND
MODE1	I	GND
MODE2	I	VCC
RDY_MODE	I	GND
BS_MODE	I	GND
ENDIAN	I	GND
RDTSW	I	VCC

Notes:

Not supported:

- ARM7
- MPC5200
- M16C

2.5 Graphics memory interface

Graphics memory interface pins

Pin name	I/O	Description
MD31 - MD0	I/O	Graphics memory bus data
MA14 - MA0	Output	Graphics memory bus data
MRAS	Output	Row address strobe
MCAS	Output	Column address strobe
MWE	Output	Write enable
DQM3 - DQM0	Output	Data mask
MCLKI	Input	Graphics memory clock input
MCLKO	Output	Graphics memory clock output

Connect the interface to the external memory used as memory for image data. The interface can be connected to 64-/128-/256-Mbit SDRAM (16- or 32-bit length data bus) without using any external circuit.

Connect MCLKI to MCLK0.

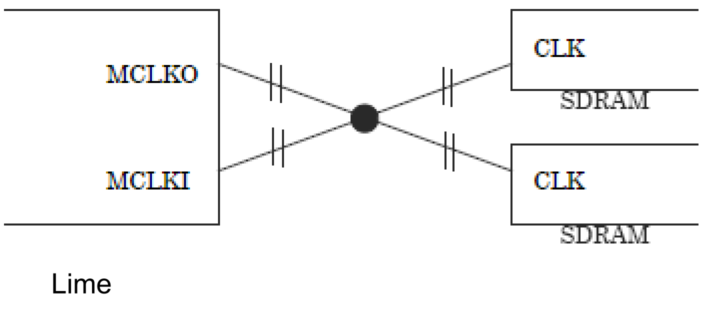
Connect XCS of SDRAM to GND.

Connect CKE of SDRAM to VCC 3V3.

Important:

The length of each PCB trace connecting Lime's MCLKI and MCLKO pins and SDRAM's CLK pin together should be the same. Please note that there could be just one piece of SDRAM used. The recommendation should be followed in that case as well. Please see below for a graphical description.

Also, take note of the AC spec of graphics memory interface.



The length of each PCB trace connecting Lime's MCLKI and MCLKO pins and SDRAM's CLK pin together should be the same. Please note that there could be just one piece of SDRAM used. The recommendation should be followed in that case as well.

2.6 Video output interface

Video Output Interface Pins

Pin name	I/O	Description
DCKI	Input	Dot clock signal input
DISPE	Output	Display Enable
DCLKI	Input	Display Clock Input
DCLKO	Output	Display Clock Output
HSYN	I/O	Horizontal sync signal output Horizontal sync input <in external sync mode>
VSYN	I/O	Vertical sync signal output Vertical sync input <in external sync mode>
CSYN	Output	Composite sync signal output
GV	Output	Graphics/video switch

Additional setting of external circuits can generate composite video signal.

Synchronous to external video signal display can be performed.

Either mode which is synchronous to DCLKI signal or one which is synchronous to dot clock, as for normal display can be selected.

Since HSYNC and VSYNC signals are set to input state after reset, these signals must be pulled up LSI externally.

The GV signal switches graphics and video at chroma key operation. When video is selected, the “Low” level is output.

2.7 Video capture interface

1) ITU-656 Input Signals

Table 2-3 Video Capture Interface Pins

Pin name	I/O	Description
(CCLK)	Input	Digital video input clock signal input This pin is multiplexed RGBCLK. Please see RGBCLK.
VIN7-0	Input	ITU656 Digital video data input. These pins are multiplexed MD63-MD56.
VINFID	Input	Field Input (Pullup/Pulldown)

Inputs ITU-RBT-656 format digital video signal

2)RGB Input Signals

The signals used for video capture are not assigned on dedicated pins but share the same pins with other functions. There is a set of signals corresponding to the RGB capture modes.

There is a possibility of sharing these pins with other pins. (TBD)

Direct Input Mode

Pin name	I/O	Description
RGBCLK	Input	Clock for RGB input. This pin is multiplexed CCLK.
RI5-0	Input	Red component value.
GI5-0	Input	Green component value.
BI5-0	Input	Blue component value.
VINSYNC	Input	Vertical sync for RGB capture.
HINSYNC	Input	Horizontal sync for RGB capture.

Note :
- the RGB bit of VCM(video capture mode) register enables RGB input mode of video capture.

2.8 I^{2}C interface

Pin name	I/O	Description
SDA	I/O	I^{2}C serial data line.
SCL	I/O	I^{2}C serial clock line.

Note)

Input voltage level is 3.3V. Please be careful, it does not support to 5V input.

(The device whose output voltage is 5V is not connectable.)

2.9 GPIO interface

Pin name	I/O	Description
GPIO4-0	I/O	General-purpose IO pin. A direct value is controlled and read by the inside register. Moreover, interruption can be generated with the value of a pin. These pins are pull-up in the chip.

2.10 General purpose mode pins

GMODE 2	GMODE 1	GMODE 0	PIN Multiplex				
			Host Interface	Primary RGB output	Secondary RGB output	Video Capture	GPIO
L	L	L	32bit CPU	RGB888	--	Native RGB666	--
L	L	H	32bit CPU	RGB888	--	RBT656/601	GPIO[4:0]
L	H	L	16bit CPU	RGB888	RGB666	RBT656/601	GPIO[2:0]
L	H	H	16bit CPU	RGB666	RGB666	Native RGB666	--
H	L	L	Reserved	Reserved	Reserved	Reserved	Reserved
H	L	H	Reserved	Reserved	Reserved	Reserved	Reserved
H	H	L	Reserved	Reserved	Reserved	Reserved	Reserved
H	H	H	Reserved	Reserved	Reserved	Reserved	Reserved

2.11 Clock input

Pin name	I/O	Description
CLK	Input	Clock input signal
S	Input	PLL reset signal
CKM	Input	Clock mode signal
CLKSEL [1:0]	Input	Clock rate select signal

Inputs source clock for internal operation clock and display dot clock. Normally, 4 Fsc (= 14.31818 MHz: NTSC) is input. An internal PLL generates the internal operation clock of 133 MHz/100 MHz and the display base clock of 400 MHz. Even if don’t use an internal PLL (use BCLKI as internal clock and use DCLKI as dot clock), don’t stop the PLL (Not fixed the S pin to low level).

CKM	Clock mode
L	Output from internal PLL selected
H	BLCKI clock selected

When CKM = L, selects input clock frequency when built-in PLL used according to setting of CSL pins

CSL1	CSL0	Input clock frequency	Multiplication rate	Display reference clock
L	L	Inputs 13.5-MHz clock frequency	× 29	391.5 MHz
L	H	Inputs 14.32-MHz clock frequency	× 28	400.96 MHz
H	L	Inputs 17.73-MHz clock frequency	× 22	390.06 MHz
H	H	Inputs 33.33-MHz clock frequency	× 12	399.96

Please connect the crystal oscillator directly with the terminal CLK. CLK value to -1% of it is supported.

2.12 Test pins

Table 2-5 Test Pins

Pin name	I/O	Description
TESTL	Input	Input 0-V power.
TESTH	Input	Input 3.3-V power.

2.13 Reset sequence

See 14.3.2 Note at power-on.

2.14 How to switch internal operating frequency

Switch the operating frequency immediately after a reset (before rewriting MMR mode register of external memory interface).

Any operating frequency can be selected from the combinations shown in ***Table 2-6***.

Table 2-6 Frequency Setting Combinations

Clock for Rendering Engine and Memory interface
133 MHz
100 MHz

3 PROCEDURE OF THE HARDWARE INITIALIZATION

3.1 Hardware reset

1.Do the hardware reset.

2.After the hardware reset, set the CCF(Change of Frequency) register (section 12.1 Host interface registers).
In being unstable cycle after the hardware reset, keep 32 bus cycles open.

3.Set the graphics memory interface register, MMR (Memory I/F Mode Register).
After setting the CCF register, take 200 us to set the MMR register.
In being unstable memory access cycle, keep 32 bus cycles open.

4.Other registers, except for the CCF register and the MMR register, should be set after setting the CCF register.
In case of not using memory access, the MMR register could be set in any order after the CCF register is set.

3.2 Re-reset

1. Reset XRST signal.

2. See section x.x for registers setting after the procedure of re-reset.

3.3 Software reset

1. Set the value of the SRST register for re-reset.

2. It is not necessary to reset the CCF register and the MMR register again.

4 HOST INTERFACE

Select the host CPU by setting the MODE0 to MODE2 signals as follows:

Table 4-1 CPU Type Setting

MODE 2	MODE 1	MODE 0	CPU
L	L	L	SH3
L	L	H	SH4
L	H	L	V832
L	H	H	SPARClite
H	L	L	General 16bit CPU with SRAM interface
H	L	H	General 16bit CPU with address and data multiplex interface
H	H	L	General 32bit CPU with address and data multiplex interface
H	H	H	Reserved

4.1 Access Mode

4.1.1 SRAM interface

Data can be transferred to/from LIME using SRAM access protocol. LIME internal registers and graphics memory are all mapped to the physical address area of the host processor.

LIME uses hardware wait based on the XRDY signal, enabling the hardware wait setting of the host CPU. When using the normally not ready mode, set the software wait to "1". When using the normally ready mode, set the software wait to "2". (When using the ***BS_MODE*** signal as "High" level, with the normally ready mode established, set the CPU software wait to three cycles.) Switch the ready mode using the ***RDY_MODE*** signal.

CPU Read

The host processor reads data from internal registers and memory of LIME in double-word (32 bit) units. Valid data is output continuously while XRD and XCS are being asserted at a "Low" level after XRDY has been asserted.

CPU Write

The host CPU writes data to internal registers and memory of LIME in byte, word(16 bit) and double-word(32 bit) units.

4.1.2 FIFO interface (fixed transfer destination address)

This interface transfers display lists stored in host memory. Display list information is transferred efficiently using a single address mode DMA transfer. Data can be transferred to FIFO in relation to FIFO buffer area mapped in memory area using SRAM interface or dual address mode.

4.2 DMA Transfer

4.2.1 Data transfer unit

DMA transfer is performed in double-word (32 bits) units or 8 double-word (32 bytes) units. Byte and word access is not supported.

Note: 8 double-word transfer is supported only in the SH4 mode.

4.2.2 Address mode

Dual address mode (mode using ACK)

DMA is performed at memory-to-memory transfer between host memory and registers mapped in memory space or graphics memory (destination). Both the host memory address and LIME is used. In the SH4 mode, the 1 double-word transfer (32 bits) and 8 double-word transfer (32 bytes) can be used.

When the CPU transfer destination address is fixed, data can also be transferred to the FIFO interface. However, in this case, even the SH4 mode supports only the 1 double-word transfer.

DREQ and DRACK pins and SRAM interface signals are used. In V832, the DREQ, DMAAK, and XTC pins and SRAM interface signals are used.

Note: The SH3 mode supports the direct address mode; it does not support the indirect address mode.

Dual address mode (mode not using ACK)

When not using the ACK signal with the dual address mode established, set bit3 at HostBase+0004h (DNA: Dual address No Ack mode) to 1.

When the ACK is not used, the DREQ signal is in the edge mode and the DREQ signal is negated per transfer and then reasserted it in the next cycle. If processing cannot be performed immediately inside LIME, the DREQ signal remains negated.

The transfer count register (DTC) of LIME is not used, so in order to end DMA transfer, write “1” to the DMA transfer stop register (DTS) from the CPU.

Note 1: In the dual DMA mode (mode without ACK), the destination address can be used only for the FIFO.

In DMA transfer to the graphics memory, etc., use the dual DMA mode.

Note 2: DMA read is not supported.

Single address mode (FIFO interface)

Data is transferred between host memory (source) and FIFO (destination). Only the address output from the host memory is used, and the data is transferred to the FIFO. This mode does not support data write to the host memory. When the FIFO is full, the DMA transfer is suspended.

The 1 double-word transfer (32 bits) and the 8 double-word transfer (32 B) can be used.

DREQ, DTACK, and DRACK signal are used.

Note: The single-address mode is supported only in the SH4 mode.

4.2.3 Bus mode

LIME supports the DMA transfer cycle steal mode and burst mode according to setting of external DMA mode.

Cycle steal mode (In the V832 mode, the burst mode is called the single transfer mode.)

In the cycle steal mode, the right to use the bus is obtained or released at every data transfer of 1 unit. The DMA transfer unit can be selected from between the 1 double-word (32 bits) and 8 double-words (32 B).

Burst mode (In the V832 mode, the burst mode is called the demand transfer mode.)

When DMA transfer is started, the right to use the bus is acquired and the transfer begins. The data transfer unit can be selected from between 1 double-word (32 bits) and 8 double-words.

Note: When performing DMA transfer in the dual-address mode, a function for automatically negating DREQ is provided based on the setting of the DBMbit in DSU register.

4.2.4 DMA transfer request

Single-address mode

DMA is started when the LIME issues an external request to DMAC of the host processor.

Set the transfer count in the transfer count register of the LIME and then issue DREQ.

Fix the CPU destination address to the FIFO address.

Dual-address mode

DMA is started by two procedures: LIME issues an external request to DMAC of the host processor, or the CPU itself is started (auto request mode, etc.). In Ack use mode, set the transfer count in the transfer count register of LIME and then issue DREQ.

Note: In the Ack unused mode and the V832 mode requires no setting of the transfer count register.

4.2.5 Ending DMA transfer

SH3/SH4

When the LIME transfer count register is set to 0, DMA transfer ends and DREQ is negated.

V832

When the XTC signal from the CPU is low-asserted while the DMAAK signal to S LIME is high-asserted, the end of DMA transfer is recognized and DREQ is negated.

The end of DMA transfer is detected in two ways: the DMA status register (DST) is polled, and an interrupt to end the drawing command ($FD000000_H$) is added to the display list and the interrupt is detected.

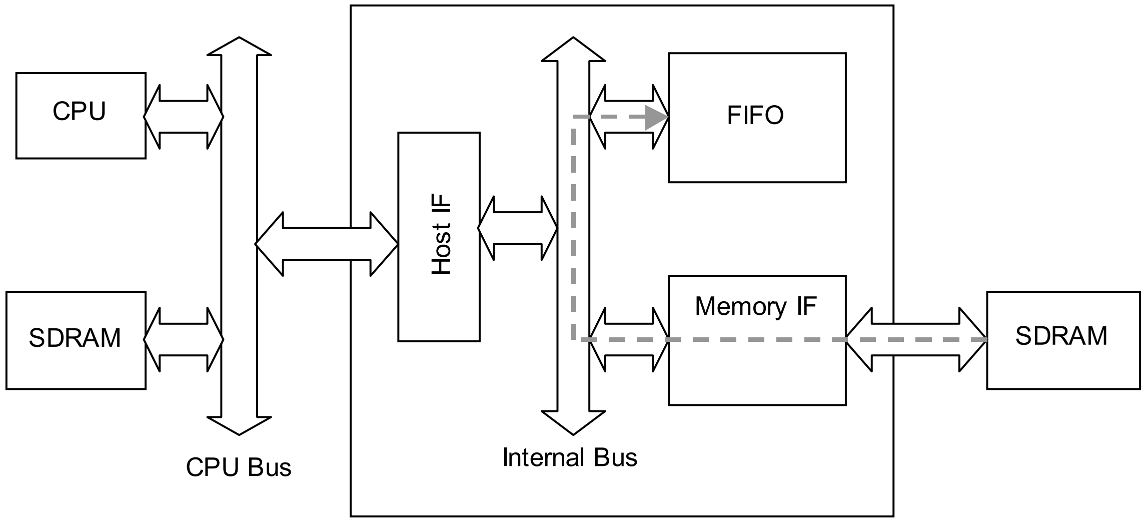
In the dual address mode (mode not using ACK), the DMA transfer count register (DTC) is not used, so the DMA ending cannot be determined. The DREQ signal can be negated to end DMA by writing 1 from the CPU to the DMA transfer stop register (DTS) of LIME at DMA transfer end.

4.3 Transfer of Local Display List

This is the mode in which the LIME internal bus is used to transfer the display list stored in the graphics memory to the FIFO interface.

During transfer of the local display list, the host bus can be used for CPU read/write.

How to transfer list: Store the display list in the local memory of LIME, set the transfer source local address (LSA) and the transfer count (LCO), and then issue a request (LREQ). Whether or not the local display list is currently being transferred is checked using the local transfer status register (LSTA).



Transfer Path for Local Display List

4.4 Interrupt

LIME issues interrupt requests to the host CPU. Following shows the types of interrupt factor and they can be enabled/disabled by IMASK (Interrupt Mask Register).

Vertical synchronization detect

Field synchronization detect

External synchronization error detect

Drawing command error

Drawing command execution end

GPIO pinmonitoring

4.4.1 Address Error Interrupt

Certain addresses are invalid depending on operation. For example the Burst Controller cannot access the Host Interface internal registers. If an attempt is made to do this then the access will be terminated and an Address Error Interrupt triggered.

4.5 SH3 Mode

In the SH3 mode, operation is assured under the following conditions:

Normally not ready mode

BCLK (CPU bus clock) is 50 MHz or less.

The XWAIT setup time is 9.0 ns or less.

Normally ready mode

Three cycles or more are set for the software wait.

4.6 Wait

Software wait

The software wait is a wait performed on the CPU side; this wait specifies how many cycles of the ready signal (XRDY) sampling timing is ignored.

Hardware wait

The hardware wait is a wait on the LIME side that occurs when LIME itself cannot read/write data immediately.

4.7 16-bit CPU mode

In the 16-bit CPU mode (16-bit SRAM I/F, 16-bit AD I/F), the data is accessed in the following rules.

1. The data is accessed in the following order, lower 16-bit of 32-bit and upper 16-bit of 32-bit continuosly.

2. The address is accessed ountinuosly.

If those rules are not kept, it returns an error. Refer to the related Host Interface register in details.

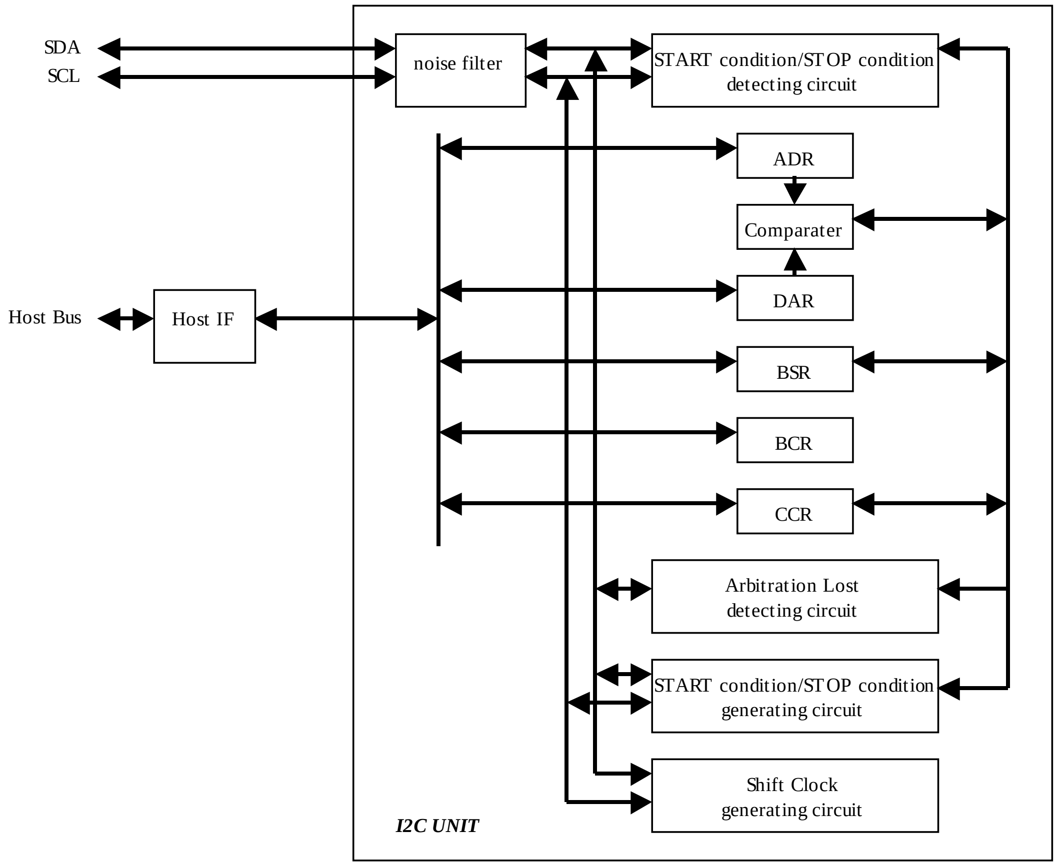
5 I^{2}C Interface Controller

5.1 Features

- Master transmission and receipt
- Slave transmission and receipt
- Arbitration
- Clock synchronization
- Detection of slave address
- Detection of general call address
- Detection of transfer direction
- Repeated generation and detection of START condition
- Detection of bus error
- Correspondence to standard-mode (100kbit/s) / high-speed-mode (400kbit/s)

5.2 Block diagram

5.2.1 Block Diagram



5.2.2 Block Function Overview

START condition / STOP condition detecting circuit
This circuit performs detection of START condition and STOP condition from the state of SDA and SCL.

START condition / STOP condition generating circuit
This circuit performs generation of START condition and STOP condition by changing the state of SDA and SCL.

Arbitration Lost detecting circuit
This circuit compares the data output to the SDA line with the data input into the SDA line at the time of data transmission, and it checks whether the data is identical. If not identical, the circuit detects this as an arbitration lost state.

Shift Clock generating circuit
This circuit performs generating timing count of the clock for serial data transfer, and output control of SCL clock by setup of a clock control register.

Comparater
Comparater compares whether the received address and the self-address appointed to be the address register is in agreement, and whether the received address is a global address.

ADR
ADR is the 7-bit register which appoints a slave address.

DAR
DAR is the 8-bit register used by serial data transfer.

BSR
BSR is the 8-bit register for the state of I2C bus etc. This register has following functions:
- detection of repeated START condition
- detection of arbitration lost
- storage of acknowledge bit
- data transfer direction
- detection of addressing
- detection of general call address
- detection of the 1st byte

BCR
BCR is the 8-bit register which performs control and interruption of I2C bus. This register has following functions:
- request / permission of interruption
- generation of START condition
- selection of master / slave
- permission to generate acknowledge

CCR

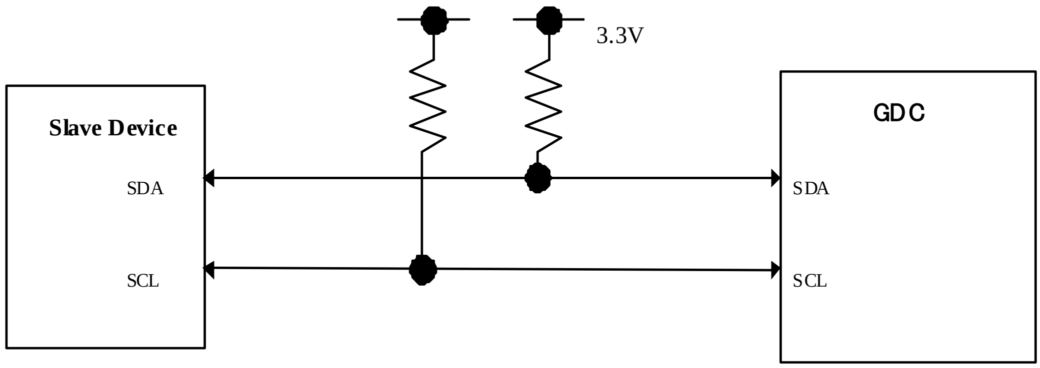
CCR is the 7-bit register used by serial data transfer. This register has following functions:
- permission of operation
- setup of a serial clock frequency
- selection of standard-mode / high-speed-mode

Noise filter

This noise filter consists of a 3 step shift register. When all three value that carried out the continuation sampling of the SCL/SDA input signals is “1”, the filter output is “1”. Conversely when all three value is “0”, the filter output is “0”. To other samplings it holds the state before 1 clock.

5.3 Example application

5.3.1 Connection Diagram



5.4 Function overview

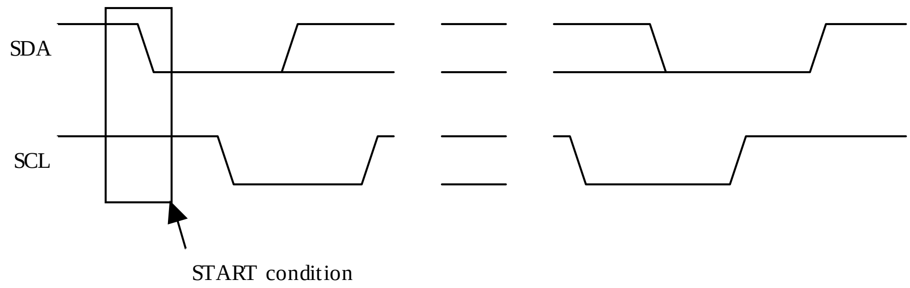
Two bi-directional buses, serial data line (SDA) and serial clock line (SCL), carry information at I2C-bus. Scarlet I2C interface has SDA input (SDAI) and SDA output (SDAO) for SDA and is connected to SDA line via open-drain I/O cell. And this interface also has SCL input (SCLI) and SCL output (SCLO) for SCL line and is connected to SCL line via open-drain I/O cell. The wired theory is used when the interface is connected to SDA line and SCL line.

5.3.2 START condition

If “1” is written to MSS bit while the bus is free, this module will become a master mode and will generate START condition simultaneously. In a master mode, even if a bus is in a use state (BB=1), START condition can be generated again by writing “1” to SCC bit.

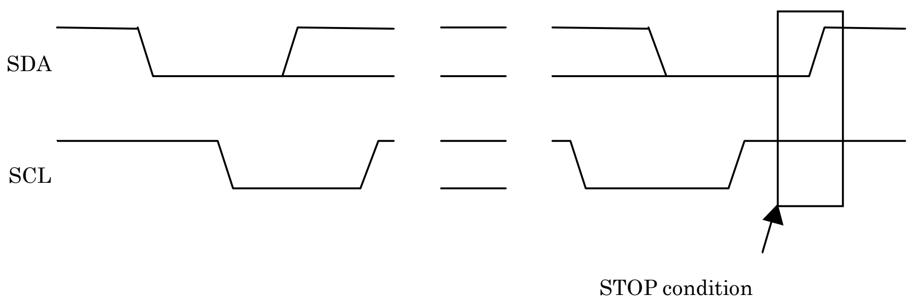
There are two conditions to generate START condition.
- “1” writing to MSS bit in the state where the bus is not used (MSS=0 & BB=0 & INT=0 & AL=0)
- “1” writing to SCC bit in the interruption state in a master mode (MSS=1 & BB=1 & INT=1 & AL=0)

If “1” writing is performed to MSS bit in an idol state, AL bit will be set to “1”. “1” writing to MSS bit other than the above is disregarded.



5.3.3 STOP condition

If “0” is written to MSS bit in a master mode (MSS=1), this module will generate STOP condition and will become a slave mode.
There is a condition to generate STOP condition.
- “0” writing to MSS bit in the interruption state in a master mode (MSS=1 & BB=1 & INT=1 & AL=0)
“0” writing to MSS bit other than the above is disregarded.



5.3.4 Addressing

In a master mode, it is set to BB="1" and TRX="0" after generation of START condition, and the contents of DAR register are output from MSB. When this module receives acknowledge after transmission of address data, the bit-0 of transmitting data (bit-0 of DRA register after transmission) is reversed and it is stored in TRX bit.

- Transfer format of slave address

A transfer format of slave address is shown below:

MSB							LSB	
A6	A5	A4	A3	A2	A1	A0	R/W	ACK

← → slave address

- Map of slave address

A map of slave address is shown below:

slave address	R/W	Description
0 0 0 0 0 0 0	0	General call address
0 0 0 0 0 0 0	1	START byte
0 0 0 0 0 0 1	X	CBUS address
0 0 0 0 0 1 0	X	Reserved
0 0 0 0 0 1 1	X	Reserved
0 0 0 0 1XX	X	Reserved
0 0 0 1 XXX ¦ 1 1 1 0 XXX	X	Available slave address
1 1 1 1 0 XX	X	10-bit slave addressing*1
1 1 1 1 1 XX	X	Reserved

*1 This module does not support 10-bit slave address.

5.3.5 Synchronization of SCL

When two or more I2C devices turn into a master device almost simultaneously and drive SCL line, each devices senses the state of SCL line and adjusts the drive timing of SCL line automatically in accordance with the timing of the latest device.

5.3.6 Arbitration

When other masters have transmitted data simultaneously at the time of master transmission, arbitration takes places. When its own transmitting data is “1” and the data on SDA line is “0”, the master considers that the arbitration was lost and sets “1” to AL. And if the master is going to generate START condition while the bus is in use by other master, it will consider that arbitration was lost and will set “1” to AL.
When the START condition which other masters generated is detected by the time the master actually generated START condition, even when it checked the bus is in nonuse state and wrote in MSS=”1”, it considers that the arbitration was lost and sets “1” to AL.
When AL bit is set to “1”, a master will set MSS=”0” and TRX= “0” and it will be a slave receiving mode.
When the arbitration is lost (it has no royalty of a bus), a master stops a drive of SDA. However, a drive of SCL is not stopped until 1 byte transfer is completed and interruption is cleared.

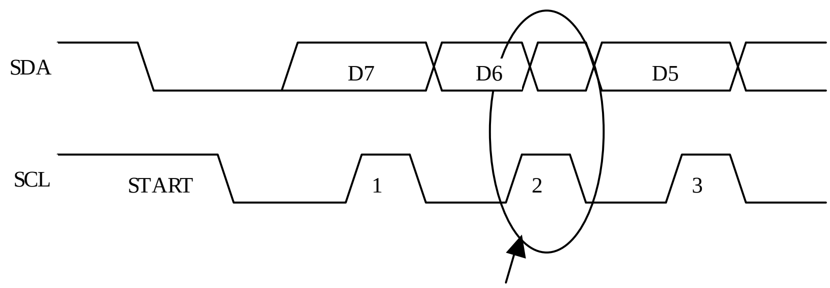
5.3.7 Acknowledge

Acknowledge is transmitted from a reception side to a transmission side. At the time of data reception, acknowledge is stored in LRB bit by ACK bit.
When the acknowledge from a master reception side is not received at the time of slave transmission, it sets TRX=”0” and becomes slave receiving mode. Thereby, a master can generate STOP condition when a slave opens SCL.

5.3.8 Bus error

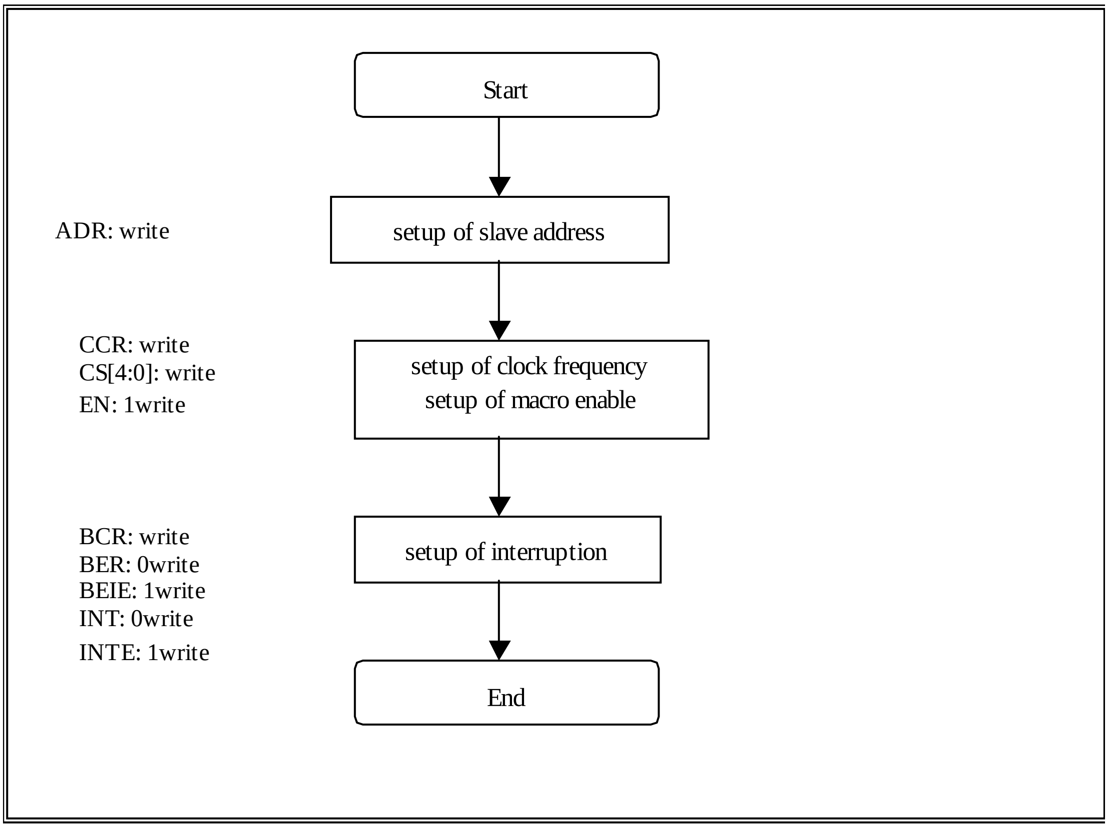
When the following conditions are satisfied, it is judged as a bus error, and this interface will be in a stop state.

- Detection of the basic regulation violation on I2C-bus under data transfer (including ACK bit)
- Detection of STOP condition in a master mode
- Detection of the basic regulation violation on I2C-bus at the time of bus idol

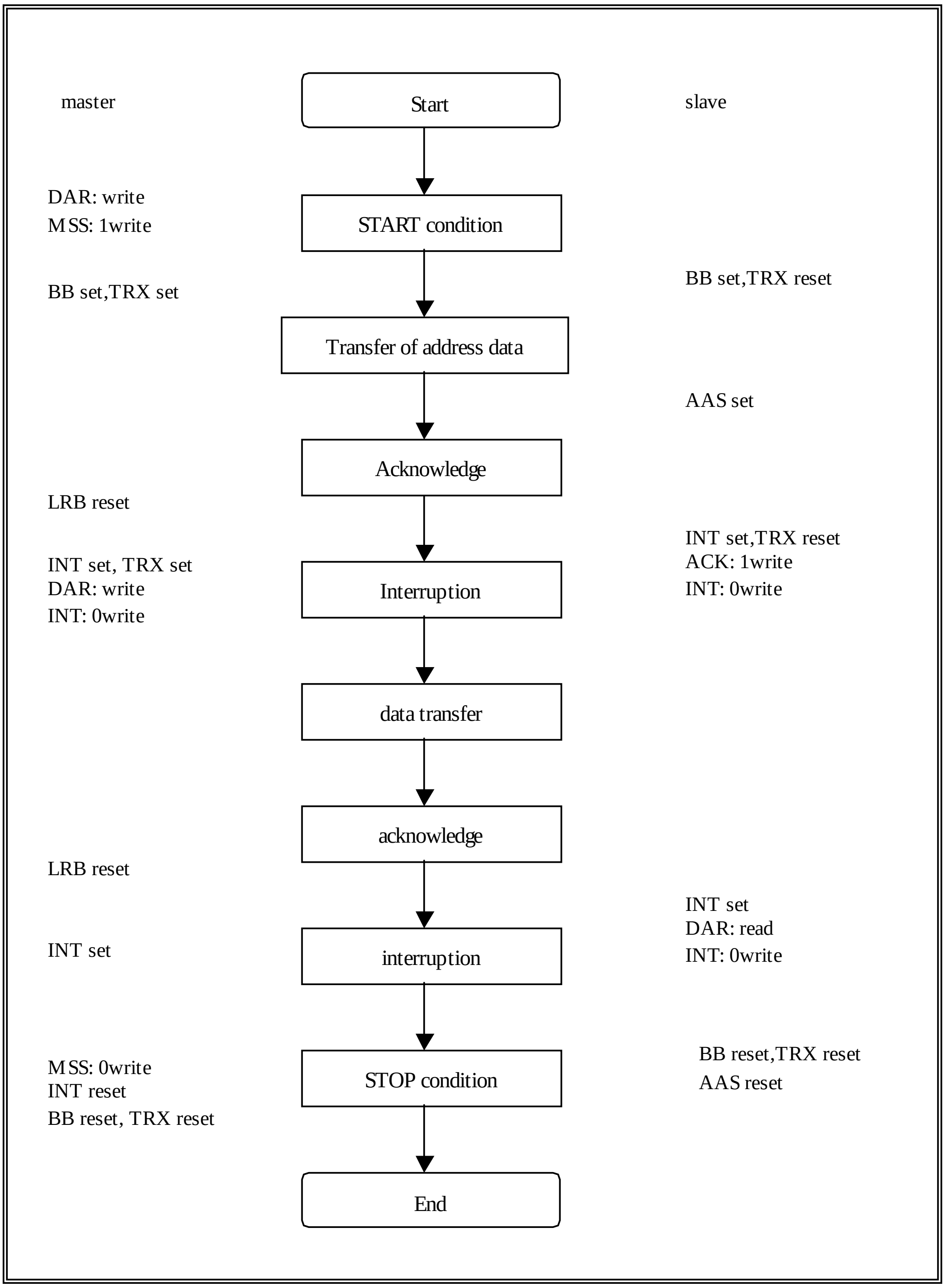


SDA changed under data transmission (SCL=H). It becomes bus error.

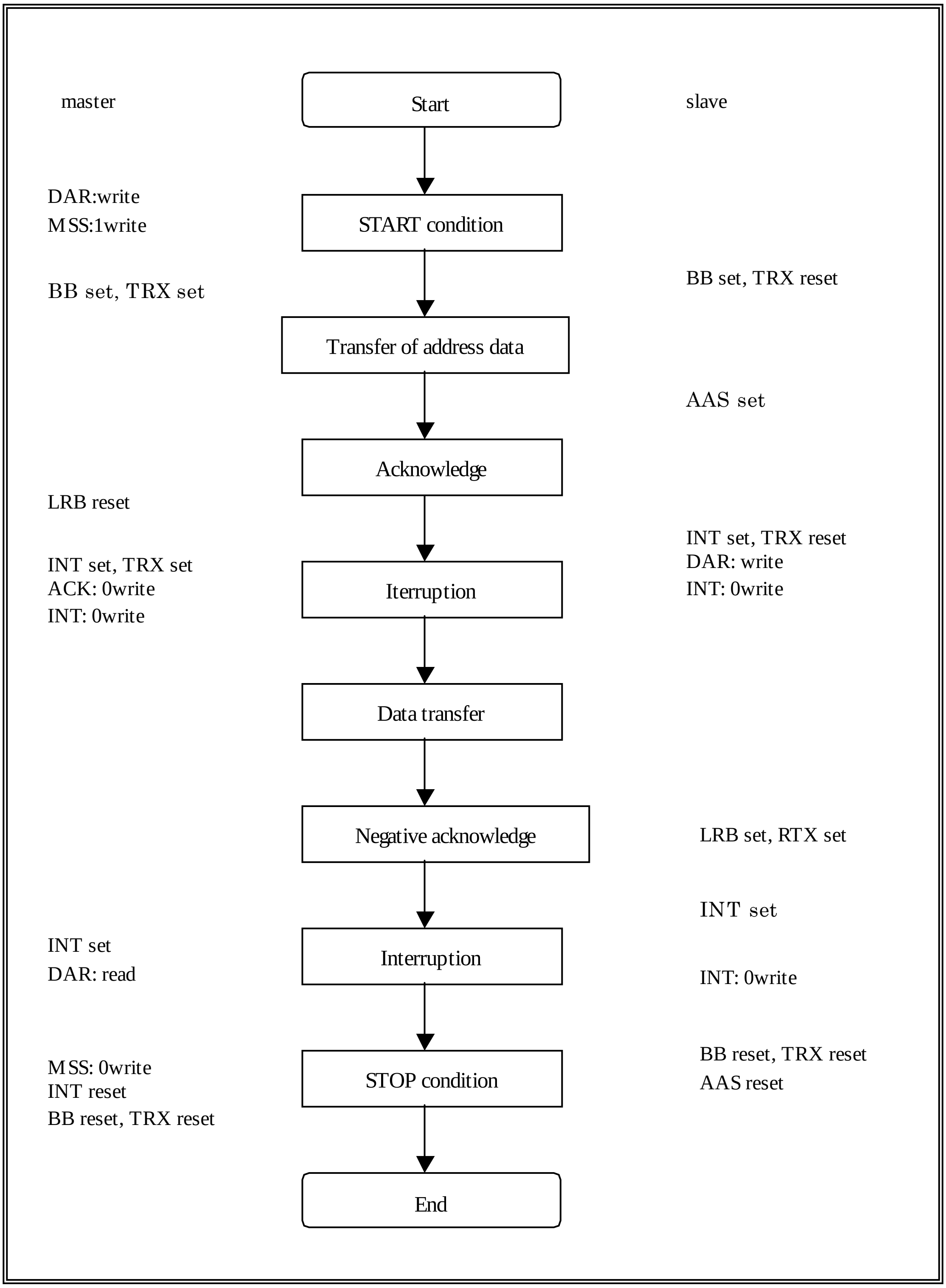
5.3.9 Initialize



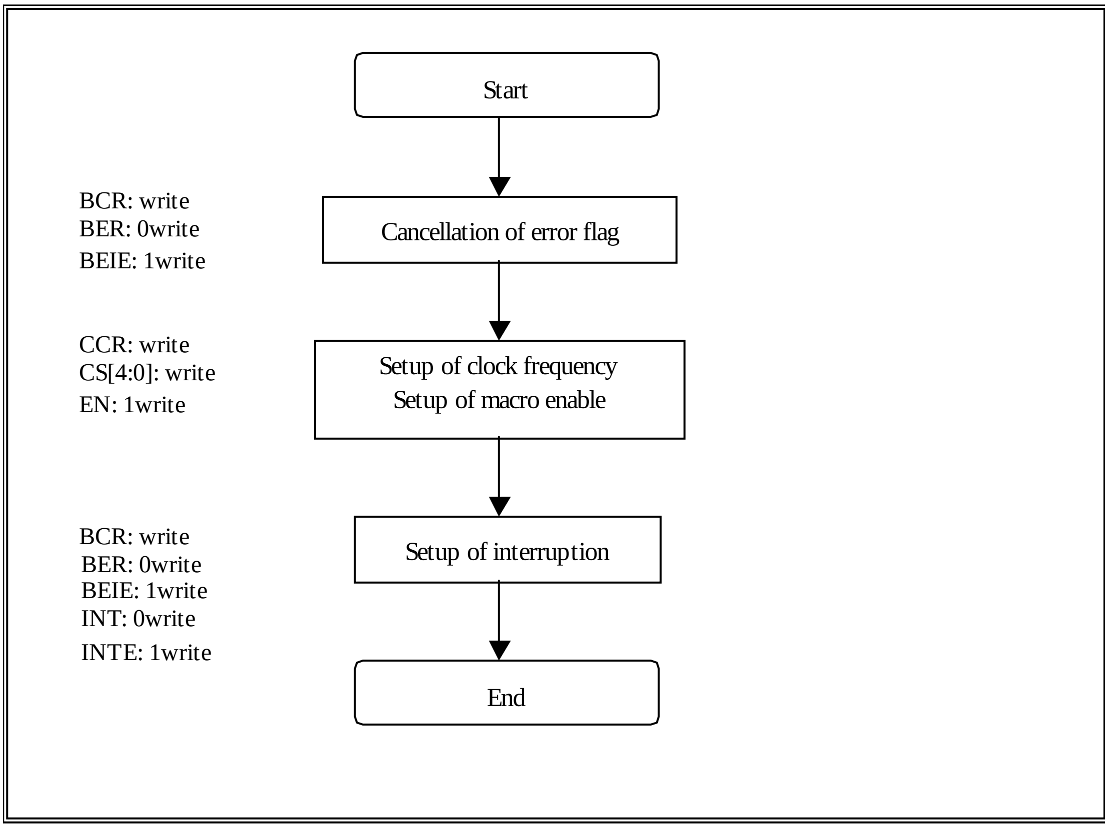
5.3.10 1-byte transfer from master to slave



5.3.11 1-byte transfer from slave to master



5.3.12 Recovery from bus error



5.4 Note

A) About a 10-bit slave address

This module does not support the 10-bit slave address. Therefore, please do not specify the slave address of from 78H to 7bH to this module. If it is specified by mistake, a normal transfer cannot be performed although acknowledge bit is returned at the time of 1 byte reception.

B) About competition of SCC, MSS, and INT bit

Competition of the following byte transfer, generation of START condition, and generation of STOP condition happens by the simultaneous writing of SCC, MSS, and INT bit. At this time the priority is as follows.

1) The following byte transfer and generation of STOP condition
   If “0” is written to INT bit and “0” is written to MSS bit, priority will be given to “0” writing to MSS bit and STOP condition will be generated.
2) The following byte transfer and generation of START condition
   If “0” is written to INT bit and “1” is written to SCC bit, priority will be given to “1” writing to SCC bit and START condition will be generated.
3) Generation of START condition and generation of STOP condition
   The simultaneous writing of “1” in SCC bit and “0” to MSS bit is prohibition.

C) About setup of S serial transfer clock

When the delay of the positive edge of SCL terminal is large or when the clock is extended by the slave device, it may become smaller than setting value (calculation value) because of generation of overhead.

6 Graphics Memory

6.1 Configuration

The LIME GDC uses local external memory (Graphics memory) for drawing and display management. The configuration of this Graphics memory is described as follows:

6.1.1 Data type

The LIME GDC handles the following types of data. Display list can be stored in the host (main) memory as well. Texture/tile pattern and text pattern can be defined by a display list as well.

Drawing Frame

This is a rectangular image data field for 2D drawing. The LIME GDC is able to have plural drawing frames and display a part of these area if it is set to be bigger than display size. The maximum size is 4096x4096 pixel in 32 pixel units. And both indirect color (8 bits / pixel) and direct color (16 bits / pixel) mode are applicable.

Display Frame

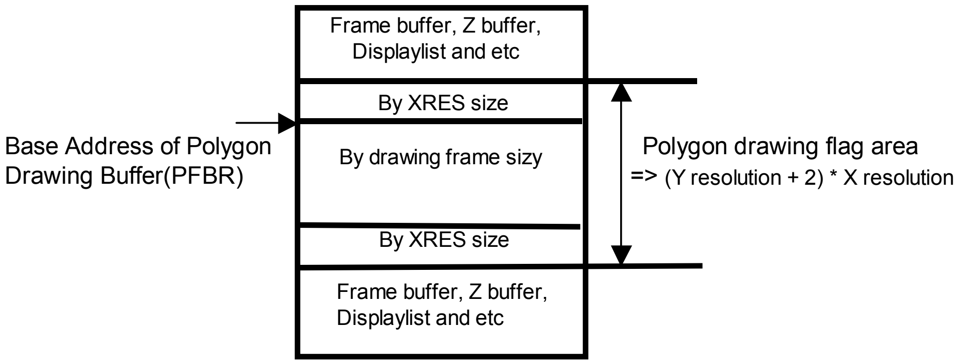
This is a rectangle picture area for display. The LIME GDC is able to set display layer up to 6 layers.

Z Buffer

Z buffer is required for eliminating hidden surfaces. In 16 bits modes, 2 bytes and in 8 bits mode, 1 byte are required per 1 pixel. This area has to be cleared before drawing.

Polygon Drawing Flag Buffer

This area is used for polygon drawing. It requires 1 bit of memory per 1 pixel and 1 x-axis line area both before and after it. Initially, this area has to be cleared.



Specially, when you use Polygon with Shadow, required area is depending on geometory view volume clip parameter. (Normally depending on drawing clipping parameter) Above “Y resolution” is “Possible_view_clipped_Max_Ydc-Possible_view_clipped_Min_Ydc+1+6”. (+6 mergin must be needed)

Displaylist Buffer

The displaylist is a list of drawing commands and parameters.

Texture Pattern

This pattern is used for texture mapping. The maximum size is up to 4096 x 4096 pixels.

Cursor Pattern

This is used for hardware cursor. The data format is indirect color (8 bits / pixel) mode. And the LIME GDC is able to display two cursor of 64 x 64 pixel size.

6.1.2 Memory Mapping

A graphics memory is mapped linearly to host CPU address field. Each of these above data is able to be allocated anywhere in the Graphics memory according to the respective register setting. (However there are some restrictions of an addressing boundary depending on a data type.)

The following shows the memory map of LIME to the host CPU memory space. The address is mapped differently in SH3, SH4 , V832, 16bit CPU etc.

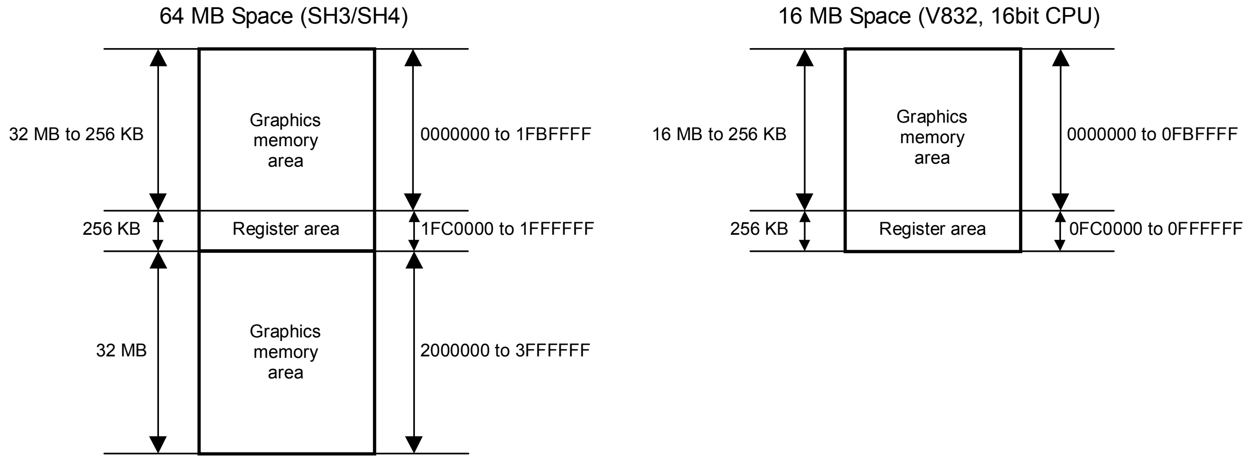


Fig. 5.1 Memory Map

Table 5-1 Address Space in SH4, SH3 Mode

Size	Resource	Base address	(Name)
32 MB to 256 KB		00000000	
64 KB	Host interface registers	01FC0000	(HostBase)
32 KB	Display registers	01FD0000	(DisplayBase)
32 KB	Capture registers	01FD8000	(CaptureBase)
32 KB	Drawing registers	01FF0000	(DrawBase)
32 KB	Peripheral I/O registers	01FF8000	(PIOBase)
32 MB	Graphics memory	02000000	

Table 4-5 Address Space in V832, 16bit CPU Mode

Size	Resource	Base address	(Name)
16 MB to 256 KB	Graphics memory	00000000	
64 KB	Host interface registers	00FC0000	(HostBase)
32 KB	Display registers	00FD0000	(DisplayBase)
32 KB	Capture registers	00FD8000	(CaptureBase)
32 KB	Drawing registers	00FF0000	(DrawBase)
32 KB	Peripheral I/O registers	00FF8000	(PIOBase)

When the SH3 or SH4 mode is used, the register area can be moved by writing 1 to bit 0 at HostBase + 005Ch (RSW: Register location Switch). In the initial state, the register space is at the center (1FC0000) of the 64 MB space; access LIME after about 20 bus clocks after writing 1 to RSW.

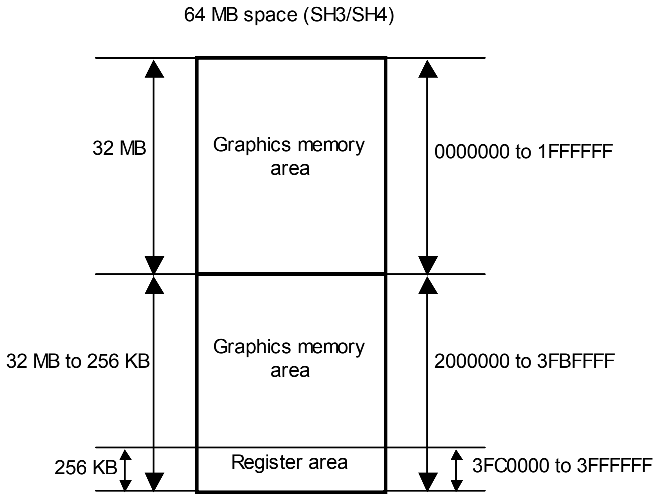


Fig. 4.2 Memory Map

Table 4-6 Address Mapping in SH3/SH4 Mode

Size	Resource	Base address	(Name)
64 MB to 256 KB	Graphics memory	00000000	
64 KB	Host interface registers	03FC0000	(HostBase)
32 KB	Display registers	03FD0000	(DisplayBase)
32 KB	Capture registers	03FD8000	(CaptureBase)
32 KB	Drawing registers	03FF0000	(DrawBase)
32 KB	Peripheral I/O registers	03FF8000	(PIOBase)

6.1.3 Data Format

Direct Color (16 bits / pixel)

This data format is described RGB as each 5 bit. Bit15 is used for alpha bit of layer blending.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A	R					G					B				

Indirect Color (8 bits / pixel)

This data format is a color index code for looking up table (palette).

7	6	5	4	3	2	1	0
Color Code							

Z Value(Optional function)

It is possible to use Z value as 8 bits or 16 bits. These data format are unsigned integer.

1) 16 bits mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Unsigned Integer															

2) 8 bits mode

7	6	5	4	3	2	1	0
Unsigned Integer							

Polygon Drawing Flag

This data format is 1 bit per 1 pixel.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16

Texture / Tile Pattern

It is possible to use a pattern as direct color mode (16 bits / pixel) or indirect color mode (8 bits / pixel).

1) Direct color mode (16 bits / pixel)

This data format is described RGB as each 5 bit. Bit15 is used for alpha bit of stencil or stencil blending. (Only texture mapping)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A	R					G					B				

2) Indirect color mode (8 bits / pixel)

This data format is a color index code for looking up table (palette).

7	6	5	4	3	2	1	0
Color Code							

Cursor Pattern

This data format is a color index code for looking up table (palette).

7	6	5	4	3	2	1	0
Color Code							

6.2 Frame Management

6.2.1 Single Buffer

The entire or partial area of the drawing frame is assigned as a display frame. The display field is scrolled by relocating the position of the display frame. When the display frame crosses the border of the drawing frame, the other side of the drawing frame is displayed, assuming that the drawing frame is rolled over (top and left edges assumed logically connected to bottom and right edges, respectively). To avoid the affect of drawing on display, the drawing data can be transferred to the Graphics Memory in the blanking time period.

6.2.2 Double Buffer

Two drawing frames are set. While one frame is displayed, drawing is done at the other frame. Flicker-less animation can be performed by flipping these two frames back and forth. Flipping is done in the blanking time period. There are two flipping modes: automatically at every scan frame period, and by user control. The double buffer is assigned independently for the L2, L3, L4, L5 layers.

6.3 Memory Access

6.3.1 Priority of memory accessing

The priority of Graphics memory accessing is the follows:

1. Refresh
2. Video Capture
3. Display processing
4. Host CPU accessing
5. Drawing accessing

6.4 Connection with memory

6.4.1 Connection with memory

The memory controller of LIME GDC supports simple connection with SDRAM by setting MMR(Memory Mode Register).
If there is N(=11 to 13) address pins in SDRAM, please connect the SDRAM address(A[n]) pin to the LIME's memory address(MA[n]) pin and SDRAM bank pin to the LIME's next address(MA[N]) pin. Then please set MMR by a number and type of memory.

The follows are the connection table between LIME pin and SDRAM pin.

64M bit SDRAM(x16 bit)

LIME pins	SDRAM pins
MA[11:0]	A[11:0]
MA12	BA0
MA13	BA1

64M bit SDRAM(x32 bit)

LIME pins	SDRAM pins
MA[10:0]	A[10:0]
MA11	BA0
MA12	BA1

128M bit SDRAM(x16 bit)

LIME pins	SDRAM pins
MA[11:0]	A[11:0]
MA12	BA0
MA13	BA1

128M bit SDRAM(x32 bit)

LIME pins	SDRAM pins
MA[11:0]	A[11:0]
MA12	BA0
MA13	BA1

256M bit SDRAM(x16 bit)

LIME pins	SDRAM pins
MA[12:0]	A[12:0]
MA13	BA0
MA14	BA1

256M bit SDRAM(x32 bit)

LIME pins	SDRAM pins
MA[11:0]	A[11:0]
MA12	BA0
MA13	BA1

512M bit SDRAM(x32 bit)

LIME pins	SDRAM pins
MA[12:0]	A[12:0]
MA13	BA0
MA14	BA1

7 DISPLAY CONTROLLER

7.1 Overview

Display control

Window display can be performed for six layers. Window scrolling, etc., can also be performed.

Backward compatibility

Backward compatibility with previous products is supported in the four-layer display mode or in the left/right split display mode.

Video timing generator

The video display timing is generated according to the display resolution (from 320 × 240 to 1280x768).

Color look-up

There are two sets of color look-up tables by palette RAM for the indirect color mode (8 bits/pixel).

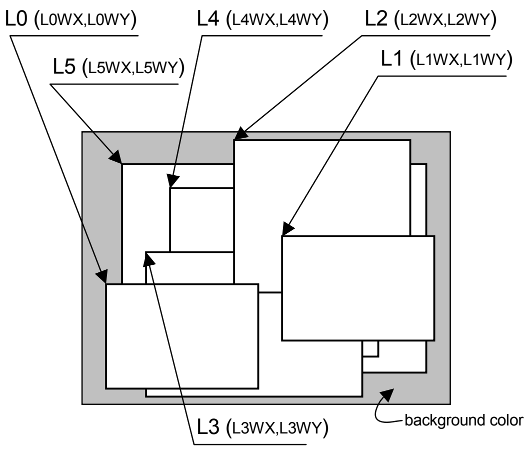
Cursor

Two sets of hardware cursor patterns (8 bits/pixel, 64 × 64 pixels each) can be used.

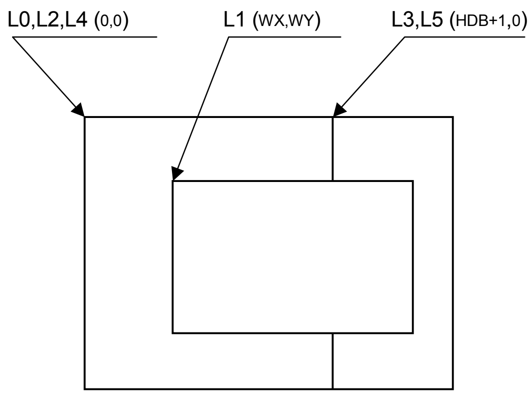
7.2 Display Function

7.2.1 Layer configuration

Six-layer window display is performed. Layer overlay sequence can be set in any order. A four-layer display mode and left/right split display mode are also provided, supporting backward compatibility with previous products.



(a) Six layerd window display



(b) Four layered display for downward compatibility

Configuration of Display Layers

The correspondence between the display layers for this product and for previous products is shown below.

Layer correspondence		Coordinates of starting point		Width/height	
		Window mode	Compatibility mode	Window mode	Compatibility mode
L0	C	(L0WX, L0WY)	(0, 0)	(L0WW, L0WH + 1)	(HDP + 1, VDP + 1)
L1	W	(L1WX, L1WY)	(WX, WY)	(L1WW, L1WH + 1)	(WW, WH + 1)
L2	ML	(L2WX, L2WY)	(0, 0)	(L2WW, L2WH + 1)	(HDB + 1, VDP + 1)
L3	MR	(L3WX, L3WY)	(HDB, 0)	(L3WW, L3WH + 1)	(HDP − HDB, VDP + 1)
L4	BL	(L4WX, L4WY)	(0, 0)	(L4WW, L4WH + 1)	(HDB + 1, VDP + 1)
L5	BR	(L5WX, L5WY)	(HDB, 0)	(L5WW, L5WH + 1)	(HDP − HDB, VDP + 1)

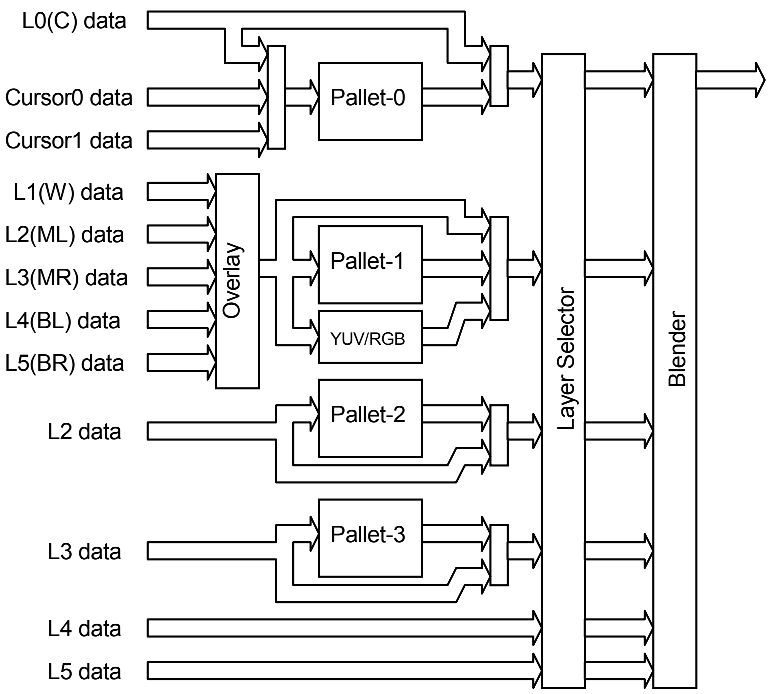
C, W, ML, MR, BL, and BR above are layers provided for compatibility to previous products. The window mode or the compatibility mode can be selected for each layer. It is possible to set window mode or compatibility mode in layer base.

However, if high resolutions are displayed, the count of layers that can be displayed simultaneously and pixel data may be restricted according to the graphics memory ability to supply data.

7.2.2 Overlay

(1) Overview

Image data for the six layers (L0 to L5) is processed as shown below.



The fundamental flow is: Palette → Layer selection → Blending. The palettes convert 8-bit color codes to the RGB format. The layer selector exchanges the layer overlay sequence arbitrarily. The blender performs blending using the blend coefficient defined for each layer or overlays in accordance with the transparent-color definition.

The L0 layer corresponds to the C layer for previous products and shares the palettes with the cursor. As a result, the L0 layer and cursor are overlaid before blend operation.

The L1 layer corresponds to the W layer for previous products. To implement backward compatibility with previous products, the L1 layer and lower layers are overlaid before blend operation.

The L2 to L5 layers have two paths; in one path, these layers are input to the blender separately and in the other, these layers and the L1 layer are overlaid and then are input to the blender. When performing processing using the extended mode, select the former; when performing the same processing as previous products, select the latter. It is possible to specify which one to select for each layer.

(2) Overlay mode

Image layer overlay is performed in two modes: simple priority mode, and blend mode.

In the simple priority mode, processing is performed according to the transparent color defined for each layer. When the color is a transparent color, the value of the lower layer is used as the image value for the next stage; when the color is not a transparent color, the value of the layer is used as the image value for the next stage.

$$D_{view} = D_{new} \text{ (when } D_{new} \text{ does not match transparent color)}$$
$$= D_{lower} \text{ (when } D_{new} \text{ matches transparent color)}$$

When the L1 layer is in the YCbCr mode, transparent color checking is not performed for the L1 layer; processing is always performed assuming that transparent color is not used.

In the blend mode, the blend ratio “r” defined for each layer is specified using 8-bit tolerance, and the following operation is performed:

$$D_{view} = D_{new}*r + D_{lower*}(1 – r)$$

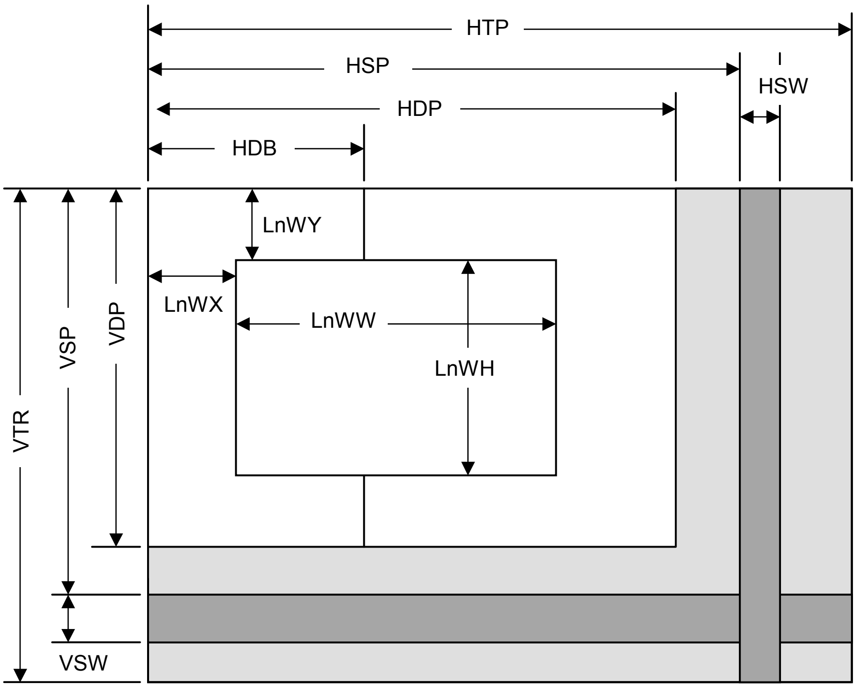
Blending is enabled for each layer by mode setting and a specific bit of the pixel is set to “1”. For 8 bits/pixel, the MSB of RAM data enables blending; for 16 bits/pixel, the MSB of data of the relevant layer enables blending; for 24 bits/pixel, the MSB of the word enables blending.

(3) Blend coefficient layer

In the normal blend mode, the blend coefficient is fixed for each layer. However, in the blend coefficient layer mode, the L5 layer can be used as the blend coefficient layer. In this mode, the blend coefficient can be specified for each pixel, providing gradation, for example. When using this mode, set the L5 layer to 8 bits/pixel, widow display mode and extend overlay mode.

7.2.3 Display parameters

The display area is defined according to the following parameters. Each parameter is set independently at the respective register.



Display Parameters

Note: The actual parameter settings are little different from the above. The details, please refer “14.3.1 Interlaced mode”.

HTP	Horizontal Total Pixels
HSP	Horizontal Synchronize pulse Position
HSW	Horizontal Synchronize pulse Width
HDP	Horizontal Display Period
HDB	Horizontal Display Boundary
VTR	Vertical Total Raster
VSP	Vertical Synchronize pulse Position
VSW	Vertical Synchronize pulse Width
VDP	Vertical Display Period
LnWX	Layer n Window position X
LnWY	Layer n Window position Y
LnWW	Layer n Window Width
LnWH	Layer n Window Height

When not splitting the window, set HDP to HDB and display only the left side of the window. The settings must meet the following relationship:

$0 < HDB \leq HDP < HSP < HSP + HSW + 1 < HTP$

$0 < VDP < VSP < VSP + VSW + 1 < VTR$

7.2.4 Display position control

The graphic image data to be displayed is located in the logical 2D coordinates space (logical graphics space) in the Graphics Memory. There are six logical graphics spaces as follows:

L0 layer

L1 layer

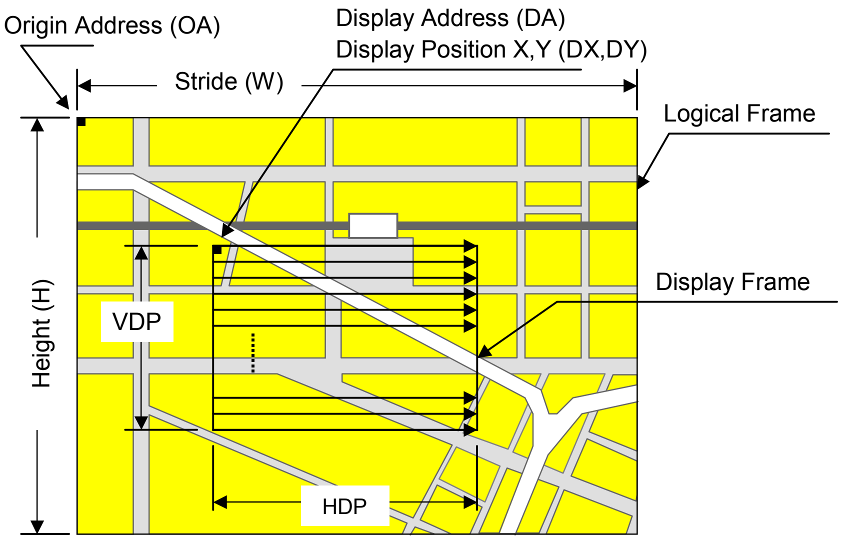
L2 layer

L3 layer

L4 layer

L5 layer

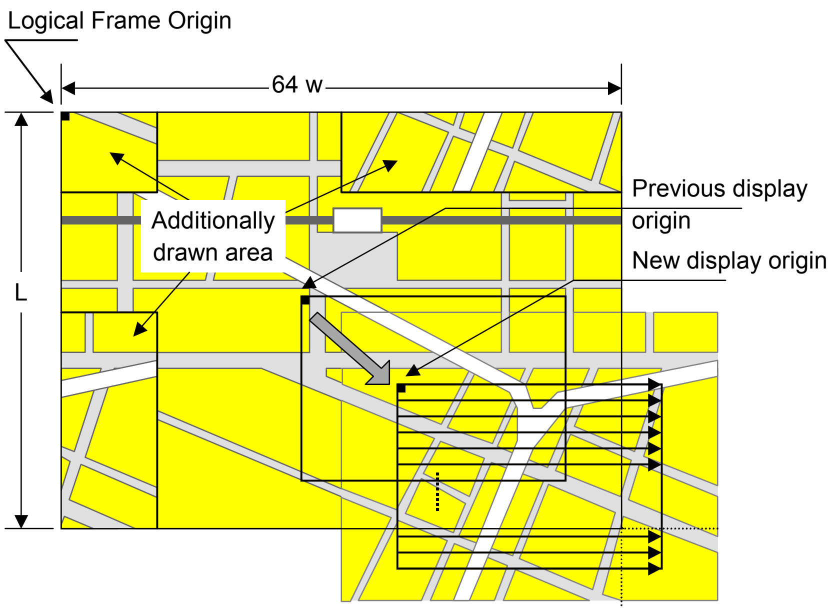
The relation between the logical graphics space and display position is defined as follows:



Display Position Parameters

OA	Origin Address	Origin address of logical graphics space. Memory address of top left edge pixel in logical frame origin
W	Stride	Width of logical graphics space. Defined in 64-byte unit
H	Height	Height of logical graphics space. Total raster (pixel) count of field
DA	Display Address	Display origin address. Top left position address of display frame origin
DX DY	Display Position	Display origin coordinates. Coordinates in logical frame space of display frame origin

MB86276 scans the logical graphics space as if the entire space is rolled over in both the horizontal and vertical directions. Using this function, if the display frame crosses the border of the logical graphics space, the part outside the border is covered with the other side of the logical graphics space, which is assumed to be connected cyclically as shown below:



Wrap Around of Display Frame

The expression of the X and Y coordinates in the frame and their corresponding linear addresses (in bytes) is shown below.

$A(x,y) = x \times bpp/8 + 64wy$ (bpp = 8 or 16)

The origin of the displayed coordinates has to be within the frame. To be more specific, the parameters are subject to the following constraints:

$0 \leq DX < w \times 64 \times 8/bpp$ (bpp = 8 or 16)

$0 \leq DY < H$

DX, DY, and DA have to indicate the same point within the frame. In short, the following relationship must be satisfied.

$DA = OA + DX \times bpp/8 + 64w \times DY$ (bpp = 8 or 16)

7.3 Display Color

Color data is displayed in the following modes:

Indirect color (8 bits/pixel)

In this mode, the index of the palette RAM is displayed. Data is converted to image data consisting of 6 bits for R, G, and B via the palette RAM and is then displayed.

Direct color (16 bits/pixel)

Each level of R, G, and B is represented using 5 bits.

Direct color (24 bits/pixel)

Each level of R, G, and B is represented using 8 bits.

YCbCr color (16 bits/pixel)

In this mode, image data is displayed with YCbCr = 4:2:2. Data is converted to image data consisting of 8 bits for R, G, and B using the operation circuit and is then displayed.

The display colors for each layer are shown below.

Layer	Compatibility mode	Extended mode
L0	Direct color (16, 24), Indirect color (P0)	Direct color (16, 24), Indirect color (P0)
L1	Direct color (16, 24), Indirect color (P1), YCbCr	Direct color (16, 24), Indirect color (P1), YCbCr
L2	Direct color (16, 24), Indirect color (P1)	Direct color (16, 24), Indirect color (P2)
L3	Direct color (16, 24), Indirect color (P1)	Direct color (16, 24), Indirect color (P3)
L4	Direct color (16, 24), Indirect color (P1)	Direct color (16, 24)
L5	Direct color (16, 24), Indirect color (P1)	Direct color (16, 24)

"Pn" stands for the corresponding palette RAM. Four palettes are used as follows:

Palette 0 (P0)

This palette corresponds to the C-layer palette for previous products. This palette is used for the L0 layer. This palette can also be used for the cursor.

Palette 1 (P1)

This palette corresponds to the M/B layer palette for previous products. In the compatibility mode, this palette is common to layers L1 to 5. In the extended mode, this palette is dedicated to the L1 layer.

Palette 2 (P2)

This palette is dedicated to the L2 layer. This palette can be used only for the extended mode.

Palette 3 (P3)

This palette is dedicated to the L3 layer. This palette can be used only for the extended mode.

7.4 Cursor

7.4.1 Cursor display function

LIME GDC can display two hardware cursors. Each cursor is specified as 64 × 64 pixels, and the cursor pattern is set in the Graphics Memory. The indirect color mode (8 bits/pixel) is used and the L0 layer palette is used. However, transparent color control (handling of transparent color code and code 0) is independent of L0 layer. Blending with lower layer is not performed.

7.4.2 Cursor control

The display priority for hardware cursors is programmable. The cursor can be displayed either on upper or lower the L0 layer using this feature. A separate setting can be made for each hardware cursor. If part of a hardware cursor crosses the display frame border, the part outside the border is not shown.

Usually, cursor 0 is preferred to cursor 1. However, with cursor 1 displayed upper the L0 layer and cursor 0 displayed lower the L0 layer, the cursor 1 display is preferred to the cursor 0.

7.5 Display Scan Control

7.5.1 Applicable display

The following table shows typical display resolutions and their synchronous signal frequencies. The pixel clock frequency is determined by setting the division rate of the display reference clock. The display reference clock is either the internal PLL (400.9 MHz at input frequency of 14.318 MHz), or the clock supplied to the DCLKI input pin. The following table gives the clock division rate used when the internal PLL is the display reference clock:

Resolution and Display Frequency

Resolution	Division rate of reference clock	Pixel frequency	Horizontal total pixel count	Horizontal frequency	Vertical total raster count	Vertical frequency
320 × 240	1/60	6.7 MHz	424	15.76 kHz	263	59.9 Hz
400 × 240	1/48	8.4 MHz	530	15.76 kHz	263	59.9 Hz
480 × 240	1/40	10.0 MHz	636	15.76 kHz	263	59.9 Hz
640 × 480	1/16	25.1 MHz	800	31.5 kHz	525	59.7 Hz
854 × 480	1/12	33.4 MHz	1062	31.3 kHz	525	59.9 Hz
800 × 600	1/10	40.1 MHz	1056	38.0 kHz	633	60.0 Hz
1024 × 768	1/6	66.8 MHz	1389	48.1 kHz	806	59.9 Hz

Pixel frequency = 14.318 MHz × 28 × reference clock division rate (when internal PLL selected)

= DCLKI input frequency × reference clock division rate (when DCLKI selected)

Horizontal frequency = Pixel frequency/Horizontal total pixel count

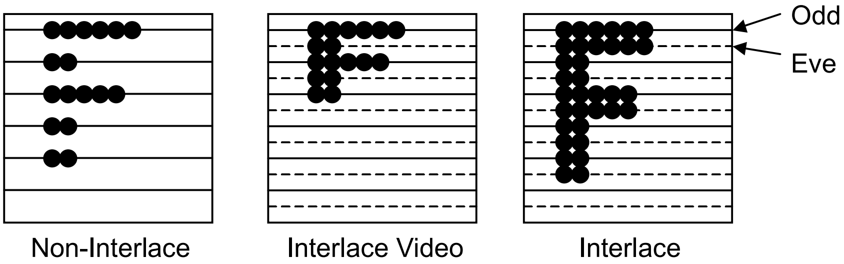
Vertical frequency = Horizontal frequency/Vertical total raster count

7.5.2 Interlace display

LIME GDC can perform both a non-interlace display and an interlace display.

When the DCM register synchronization mode is set to interlace video (11), images in memory are output in odd and even rasters alternately to each field, and one frame (odd + even fields) forms one screen.

When the DCM register synchronization mode is set to interlace (10), images in memory are output in raster order. The same image data is output to odd fields and even fields. Consequently, the count of rasters on the screen is half of that of interlace video. However, unlike the non-interlace mode, there is a distinction between odd and even fields depending on the phase relationship between the horizontal and vertical synchronous signals.

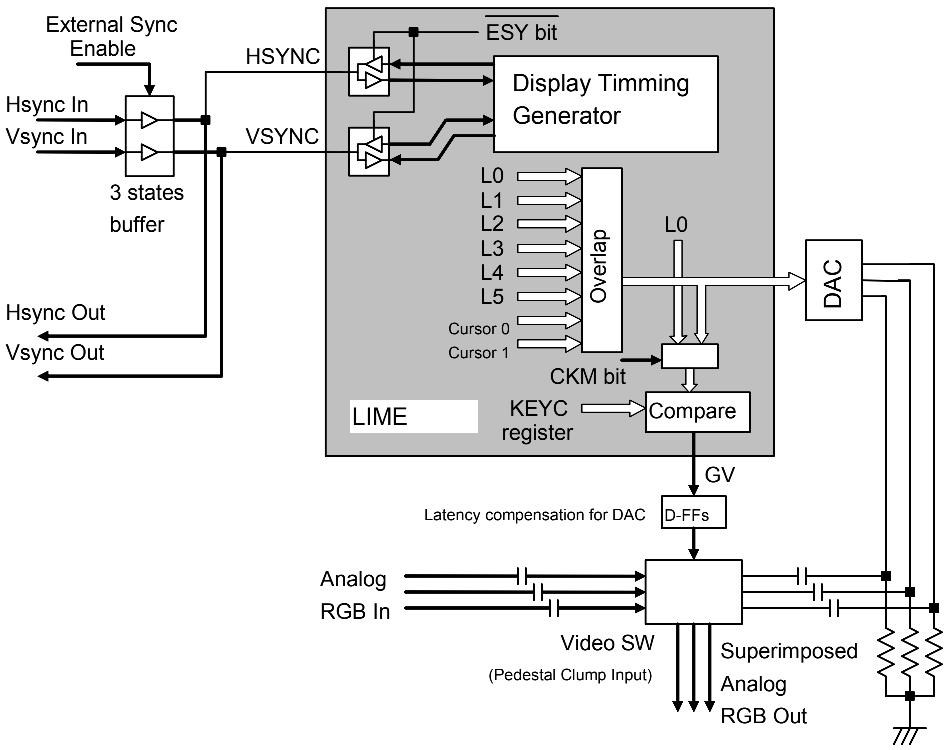


Display Difference between Synchronization Modes

7.6 The external synchronous signal

The display scan can be performed by synchronizing horizontal/vertical synchronous signal from the external.

In selecting the external synchronization mode, LIME is sampling the HSYNC signal and displays the synchronizing the external video signal. Either the internal PLL clock or the DCLKI input signal could be selected for the sampling clock. Also, the superimposed analog output is performed by the chroma key process. The following diagram shows an example of the external synchronization circuit.



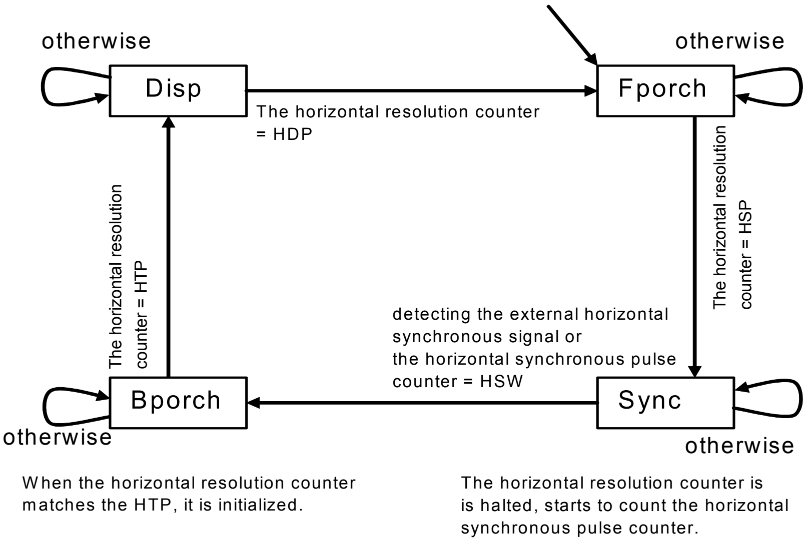
7.7 An example of the external synchronization circuit

The external synchronization mode is performed by setting the ESY bit of the DCM register. In setting the external synchronization mode, HSYNC, VSYNC, and EO pin of LIME is changed to the input mode. After that it needs to be provided the synchronous signal by using the 3 state buffer from the external. When turning off the external synchronization mode, LIME internal ESY bit needs to be switched OFF after disconnecting the synchronous input signal from the external.

The buffer of the external synchronization signal must not be switched ON when the synchronous output signal of LIME is ON. Follow the previous instruction to prevent simultaneous ON from occurring.

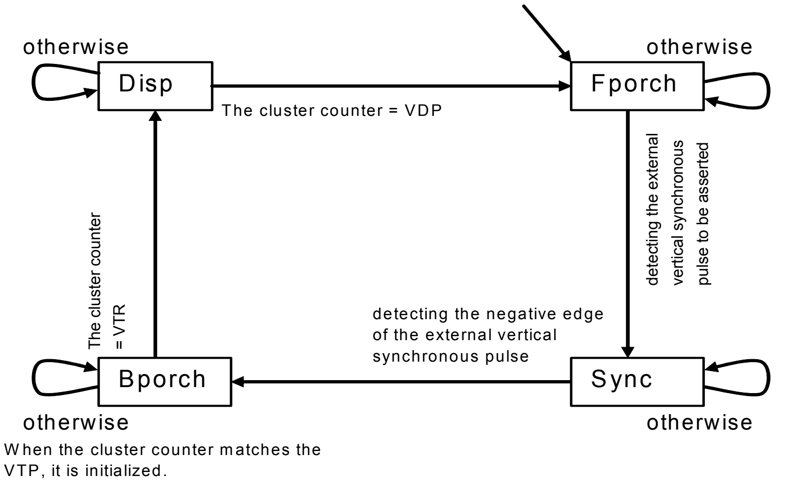
In using the external synchronous signal with the display clock based on the internal PLL, LIME extends the clock period and fits the clock phase with the horizontal synchronous signal phase after inputting the horizontal synchronous pulse. The following caution is necessary. In case of connecting the high speed transmit signal, such as LVDS, with the digital RGB output, PLL with a built-in the high speed serial transmission is temporally unstable due to this connection. Therefore, the external synchronous signal based on the internal PLL must not be used with high speed synchronous transmit signal.

The synchronization of the horizontal direction is controlled by the following state diagram.



The finite state diagram is controlled by the horizontal resolution counter. The period of outputting the signal is assigned the Disp state. When the value of the horizontal resolution counter matches that of the HDP register, it ends to output the signal and the current state is transmitted from Disp state to Fporch state (front porch). In the Fporch state, when the value of the vertical resolution register matches that of the HSP register, the current state is transmitted to the Sync state. In this state, it waits for the horizontal synchronous signal from the external. LIME detects the negative edge of the horizontal synchronous pulse from the external and synchronizes it. In detecting the horizontal synchronous signal from the external, the current state is transmitted to the Bporch state (back porch). The horizontal resolution register does not count in the Sync state, instead the horizontal synchronous counter is incremented from zero. When the value of this counter matches the setting value of the HSW register, the current state is transmitted to the Bporch state without detecting the horizontal synchronous signal form the external. When the value of the horizontal resolution counter matches that of the HTP register in the Bporch state, the horizontal resolution counter is reset, and also the current state is transmitted to the Disp state and it begins to display the next cluster.

The synchronization of vertical direction is controlled by the following state diagram.



The state diagram of the vertical direction is controlled by the value of the cluster counter. The period of outputting the signal is assigned the Disp state. When the value of the cluster counter matches the value of the VDP register, it ends to output the signal and the current state is transmitted from the Disp state to the Fporch state. In the Fporch state, it waits the external synchronous pulse to be asserted. In detecting the external synchronous pulse to be asserted, the current state is transmitted to the Sync state. In the Sync state, it waits for the negative edge of the external synchronous signal. In detecting the negative edge, the current state is transmitted to the Bporch state. When the value of the cluster counter matches the values of the VTR register, the cluster counter is reset, and also the current state is transmitted to the Disp state and it starts to display the next field.

7.8 Programmable YCbCr/RGB conversion for L1-layer display

L1-layer can display video data in YCbCr format but RGB conversion coefficients are hard-wired and fixed about previous products. LIME can program RGB conversion coefficients by registers.

YCbCr data is converted by following expression.

$R = a_{11}*Y + a_{12}*(Cb-128) + a_{13}*(Cr-128) + b_1$

$G = a_{21}*Y + a_{22}*(Cb-128) + a_{23}*(Cr-128) + b_2$

$B = a_{31}*Y + a_{32}*(Cb-128) + a_{33}*(Cr-128) + b_3$

a_{ij} ---- 11bit signed real (lower 8bit is fraction, two's complement)

b_i ----- 9bit signed integer (two's complement)

It is represented by matrix operation.

$$\begin{pmatrix} R \\ G \\ B \end{pmatrix} = \mathbf{A} \begin{pmatrix} Y \\ Cb-128 \\ Cr-128 \end{pmatrix} + \boldsymbol{b} \quad \text{where} \quad \mathbf{A} = \begin{pmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{pmatrix}, \ \boldsymbol{b} = \begin{pmatrix} b_1 \\ b_2 \\ b_3 \end{pmatrix}$$

These parameters are set on registers shown bellow.

L1YCR0 (a_{12},a_{11}), L1YCR1(b_1,a_{13})

L1YCG0 (a_{22},a_{21}), L1YCG1(b_2,a_{23})

L1YCB0 (a_{32},a_{31}), L1YCB1(b_3,a_{33})

Same conversion with previous products is applied by initial values of these registers after reset.

The register values just after reset is as follow.

a_{11} = 0x12b (299/256) , a_{12} = 0x0, a_{13} = 0x198 (408/256)

a_{21} = 0x12b (299/256), a_{22} = 0x79c (-100/256), a_{23} = 0x72f (-209/256)

a_{31} = 0x12b (299/256), a_{32} = 0x204 (516/256), a_{33} = 0x0

b_1= b_2= b_3= 0x1f0 (-16)

It is possible to control brightness, contrast, hue , color saturation by change these parameters.

Addition of a constant value into ***b*** means inclease of brightness.

Multiplication of a constant scalar value greater than one into **A** means increase of contrast.

Two dimentional rotation of Cb-128 and Cr-128 means change of hue.

Color saturation is intensity of color, relative to Y-component.

New coefficients including these changes can be got by following expression.

$$\mathbf{A} = c_1 \mathbf{A}_0 \begin{pmatrix} 1 & 0 & 0 \\ 0 & \cos(t) & \sin(t) \\ 0 & -\sin(t) & \cos(t) \end{pmatrix} \begin{pmatrix} 1 & 0 & 0 \\ 0 & c_2 & 0 \\ 0 & 0 & c_2 \end{pmatrix} = \mathbf{A}_0 \begin{pmatrix} c_1 & 0 & 0 \\ 0 & \cos(t)c_1c_2 & \sin(t)c_1c_2 \\ 0 & -\sin(t)c_1c_2 & \cos(t)c_1c_2 \end{pmatrix}$$

$$\boldsymbol{b} = \boldsymbol{b}_0 + \begin{pmatrix} c_3 \\ c_3 \\ c_3 \end{pmatrix}$$

$\mathbf{A}_0$, $\boldsymbol{b}_0$: initial value

c_1: contrast parameter, 1 is standard. 1.2 is stronger, for example.

c_2: color saturation parameter, 1 is standard. 0 means mono chrome image.

c_3: brightness parameter, 0 is standard.

t : hue rotation parameter, 0-deg is standard

Note: new a_{ij} and b_i should be clipped in valid range of value for corresponding registers.

7.9 DCLKO shift

1) Delay

DCLKO delay function is available if internal PLL is used for DCLK. DCKD field in DCM3 register defines delay value by internal PLL clock cycle.

DCKD	delay
000000	No additional delay
000010	+2 PLL clock
000100	+3 PLL clock
000110	+4 PLL clock
:	:
111110	+33 PLL clock

2) Inversion

DCLKO inversion is also available with/without delay function. This function is effective with no relation to DCLK clock source.

CKinv-bit of DCM3 enables this function.

7.10 Syncronous register update of display

To update position related parameters without disturbing display, it is need to update synchronously with VSYNC interrupt and finish at a time.

This synchronous register update mode eases this limitation. In this mode, written parameters are hold in intermediate registers and update at once synchronously with VSYNC.

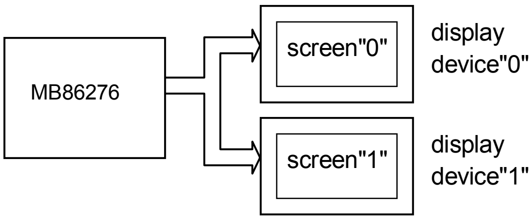
RUM-bit of DCM2 register enables this mode.

RUF-bit of DCM2 register controls start of update and shows whether update is done or not.

7.11 Dual Display

7.11.1 Overview

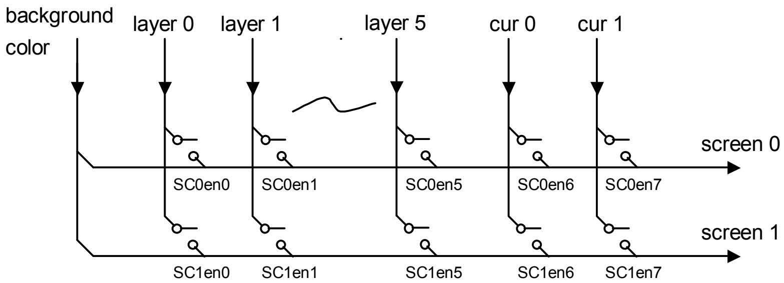
This function enables to display two screens on two display devices. It is possible to control which layer is included in a screen. It is assumed here that display device "0" has screen "0" and display device "1" has screen "1".



7.11.2 Destination Control

A layer or cursor can be included in both screens or one screen. If a layer is NOT included into a screen, this layer is treated as "transparent" . If all bits of a screen are set "0", then background color is displayed on the screen.

This destination control can be thought virtually as crosspoint switch shown next



MDen (multi display enable) bit of MDC(multi display control) register enables this function.

SC0en (screen"0" enable) field of MDC register defines which layers and cursors are included in screen “0”.

SC1en (screeen"1" enable) field of MDC register defines which layers and cursors are included in screen “1”.

bit-0 ---- L0 is included

bit-1 ---- L1 is included

:

bit-5 ---- L5 is included

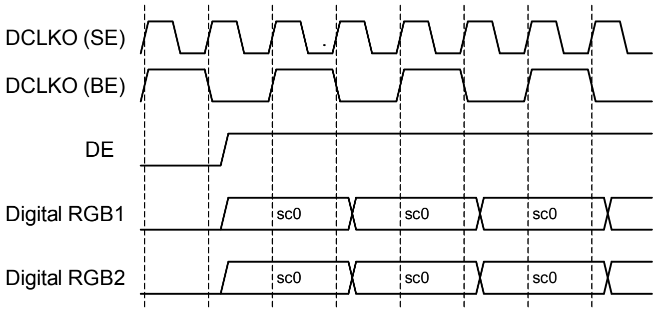
bit-6 ---- Cursor0 is included

bit-7 ---- Cursor1 is included

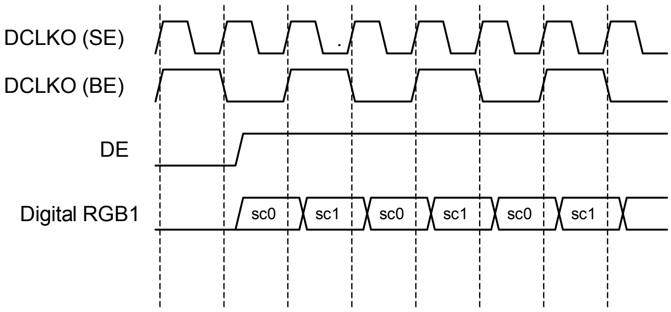
7.11.3 Output Signal Control

There are two modes to output two screens. In parallel mode, one screen is output at digital RGB1 while another screen is output at digital RGB2. In multiplex mode, two screens are multiplexed and output at digital RGB1.

(1) parallel output mode

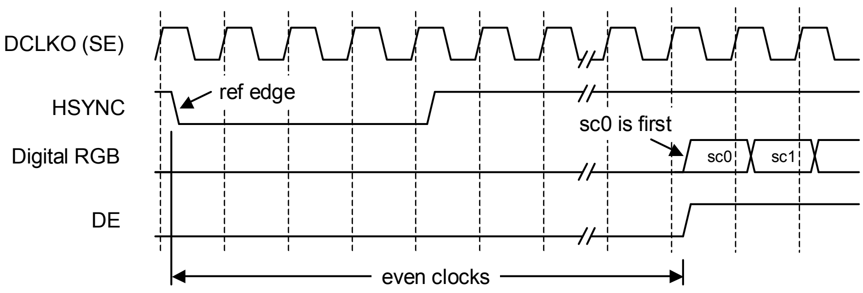


(2) multiplex output mode



In BE (bi-edge) DCLKO mode, two ouput phases can be identified both edge of DCLKO.

In SE (single-edge) DCLKO mode, two output phases cab be identified an edge of HSYNC or DE.



POM(parallel output mode) bit in DCM3 register defines which output mode is used, parallel or multiplex. POM=0 means multiplex, POM=1 means parallel, respectively.

DCKed(clock edge) bit in DCM3 register defines which DCLKO clock mode is used, BE(bi-edge) or SE(single-edge). DCKed=0

7.11.4 Output Circuit Example

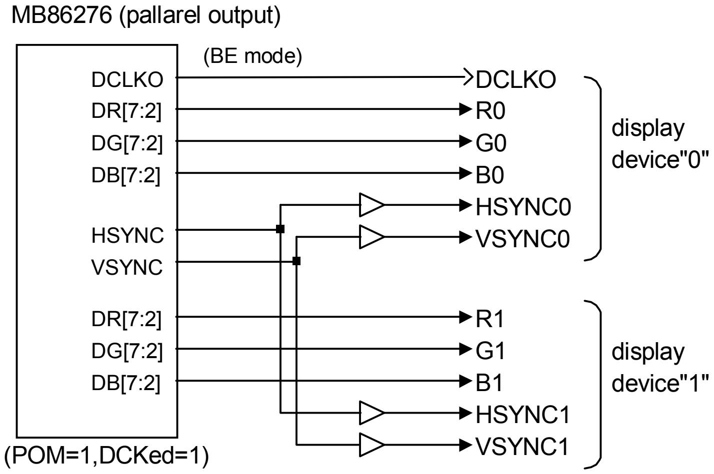
There are three types of output circuit for dual display, primalry.

Parallel, Digital Multiplex(SE), Digital Multiplex(BE)

Here these three examples are described.

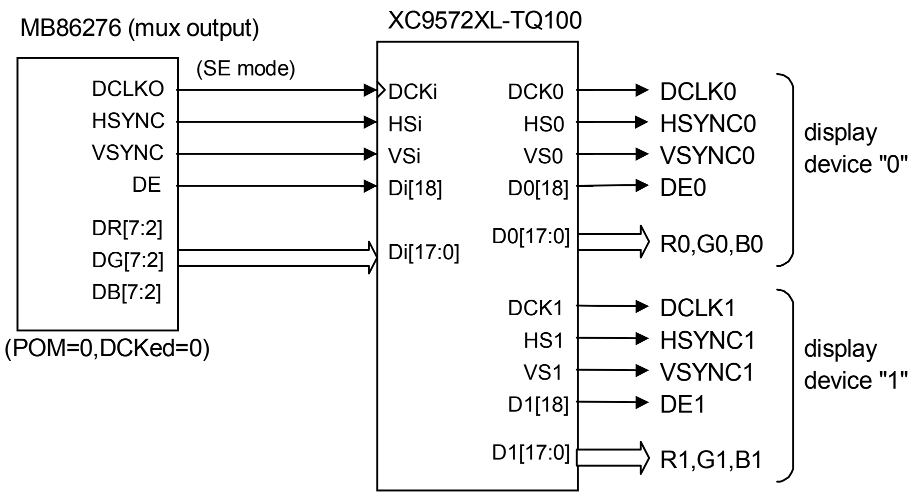
(1) Parallel output

Two screens are given as digital signals in this example.

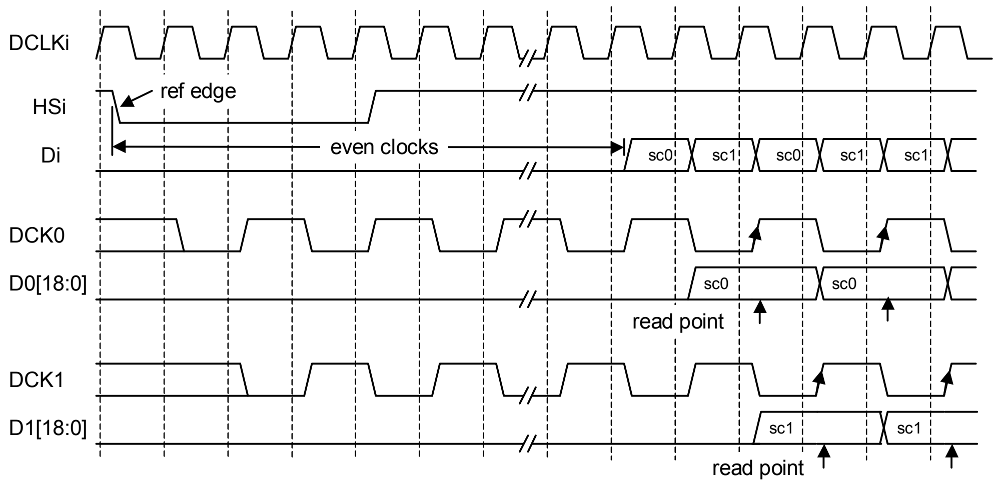


(2) Multiplexed digital output with SE mode DCLKO

In this case, CPLD can be used to demultiplex two digital streams of each screen. In following example, one economical CPLD demultiplexes RGB 6bit/component video data stream.

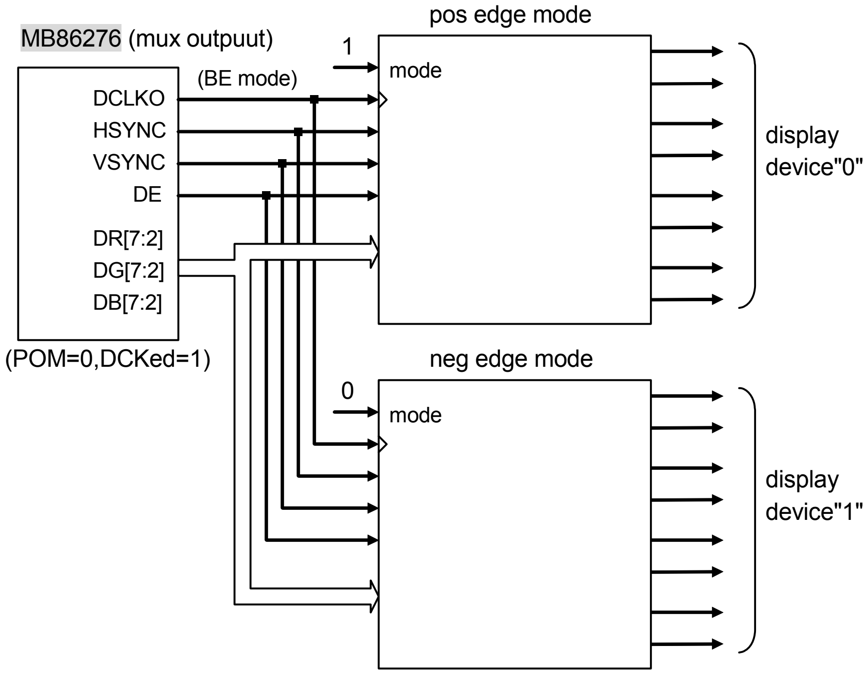


```
module XC9572XL ( DCKi, HSi,VSi,Di,  DCK0,HS0,VS0,D0,  DCK1,HS1,VS1,D1 );
    input DCKi,HSi,VSi;
    input[18:0] Di;
    output DCK0,HS0,VS0, DCK1,HS1,VS1;
    output[18:0] D0,D1;
    reg HS0,HS1, VS0,VS1, DCK0,DCK1;
    reg[18:0] D0,D1;
    always @(posedge DCKi) begin
        HS0 <= HSi; HS1 <= HS0;
        VS0 <= VSi; VS1 <= VS0;
        DCK0 <= (HS0&!HSi)? 0: !DCK0; // sync to ref edge : flip
        DCK1 <= DCK0;
        if(DCK0) D0 <= Di;
        if(DCK1) D1 <= Di;
    end
endmodule
```



(3) Multiplexed digital output with BE mode DCLKO

If a receiving device can select data strobe edge, it can be used to demultiplex two screens with rising and falling edge of DCLKO.



7.11.5 Display Clock and Timing

It is need to supply display clock of twice frequency for dual display function to work. VGA display uses 25MHz display clock, typically in single display mode while 50MHz display clock is need for dual display mode. The timing parameters such as HTP except scaling ratio (SC) are same.

Maximum display clock frequency determines maximum available resolution. It is 800 x 480. 66MHz DCLK clock is need for it.

7.11.6 Limitation

Two display devices has same scan rate and resolution with common sync signals.

The external sync mode can not be used in dual display mode.

8 Video Capture

8.1 Video Capture function

8.1.1 Input data Formats

The digital video stream of ITU RBT-656 or RGB666 format conformity is inputted (for details refer to **8.5 external video signal input conditions**).

8.1.2 Capturing of Video Signal

"LIME" becomes effective when VIE of a video capture mode register (VCM) is 1, and it is CCLK. Synchronizing with a clock, video stream data is captured from 8-bit VI pin or 20-bit RGB input pin.

8.1.3 Non-interlace Transformation

Captured video graphics can be displayed in non-interlaced format. Two modes (BOB and WEAVE) can be selected at non-interlace transformation.

- BOB Mode

In odd fields, the even-field raster generated by average interpolation are added to produce one frame. In even fields, the odd-field raster generated by average interpolation are added to produce one frame.

In order to choose BOB mode, while enable vertical interpolation in VI bit of a VCM (Video Capture Mode) register, the L1IM bit of L1M (L1-layer Mode) register is set as 0.

- WEAVE Mode

Odd and even fields are merged in the video capture buffer to produce one frame. Vertical resolutions in the WEAVE mode are higher than those in the BOB mode but raster dislocation appears at moving places.

In order to choose WEAVE mode, while disable vertical interpolation in VI bit of a VCM (Video Capture Mode) register, the L1IM bit of L1M (L1-layer Mode) register is set as 1.

8.2 Video Buffer

8.2.1 Data Form

The video capture unit of MB86276 “LIME” accepts YUV422 video data primarily, but RGB video data is also accepted via an internal RGB preprocessor which converts RGB to YUV422.

Captured pixels are stored in YCbCr format in graphics memory, 16 bits per pixel. The video data is converted to RGB when it is displayed.

31 – 24	23 – 16	15 – 8	7 – 0
Y1	Cr	Y0	Cb

	7	6	5	4	3	2	1	0
Y0,Y1	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Cr,Cb	C7	C6	C5	C4	C3	C2	C1	C0

8.2.2 Synchronous Control

Writing to the graphics memory of video image data and scan for a display are performed independently. The graphics memory for video captures is controlled by the ring buffer system. It displays the frame, when the image data for one frame can be preparing on a memory. When the frame rate of a video capture differs from the frame rate of a display, the continuation display of top omission or the same frame occurs.

8.2.3 Area Allocation

Allocate an area of about 2.2 frames to the video capture buffer. The size of this area is equivalent to the size that considers the margin equivalent to the double buffer of the frame. Set the starting address and upper-limit address of the area in the CBOA/CBLA registers. Here, specify the raster start position as the upper-limit address.

To allocate n rasters as the video capture buffer, set the upper-limit value as follows:

$$CBLA = CBOA + 64\ (n-2) \times CBW$$

In addition, the head addresses of n+1 raster are 64n×CBW, and CBLA+2 raster becomes a buffer domain. For reduced display, allocate the buffer area of the reduced frame size.

8.2.4 Window Display

The captured video picture is displayed using L1 layer. The whole or a part captured picture can be displayed as the whole screen or a window.

When performing a capture display, L1 layer is set as capture synchronous mode (L1CS=1). In this mode, L1 layer display displays the newest frame in a video capture buffer. Usually, the display address used in the mode is disregarded.

The stride of L1 layer needs to be in agreement with the stride of a video capture buffer. When not in agreement, the picture distorted aslant is displayed.

The display size of L1 layer is made in agreement with the picture size after reduction of a video capture. Invalid data will be displayed if the display size of L1 layer is set up more greatly than capture picture size.

Although selection of a RGB display and a YCbCr display can be performed in L1 layer, in performing a video capture, it chooses YcbCr form (L1YC=1).

8.2.5 Interlace Display

It is possible to display the picture taken in to the video capture buffer in WEAVE mode in an interlace. A setup confirms WEAVE mode and chooses an interlace & video display with display scan.

However, when display scan is asynchronous, flicker will come out in a scene with a motion. In order to prevent this, OO (Odd Only) bit of a CBM (Capture Buffer Mode) register is set as 1.

When synchronizing display scan with a capture, a capture input and a display output can be made to correspond to 1 to 1. In this case, the difference of flicker of an input and an output is lost. Please refer to "8.8 Capture synchronous display."

8.2.6 RGB555 Mode

As an alternative method, a special RGB555-mode can be used which is dedicated for applications where grabbed pictures should be processed further. In this mode, a single buffer is used instead of a ring buffer. In addition, data is directly stored in LIME's RGB555 format in the L1-Layer (see settings of the CBM register). This makes it possible to copy rectangular areas from the L1-layer directly to the texture buffer or to other memory locations using the BitBlt function. Note that the input and output frame rate should be identical if a single buffer method is used and that the lower bits are ignored to form the RGB555 format.

8.3 Scaling

8.3.1 Down-scaling Function

When the CM bits of the video capture mode register (VCM) are 11, LIME reduces the video screen size. The reduction can be set independently in the vertical and horizontal scales. The reduction is set per line in the vertical direction and in 2-pixel units in the horizontal direction. The scale setting value is defined by an input/output value. It is a 16-bit fixed fraction where the integer is represented by 5 bits and the fraction is represented by 11 bits. Valid setting values are from 0800_H to $FFFF_H$. Set the vertical direction at bit 31 to bit 16 of the capture scale register (CSC) and the horizontal direction at bits 15 to bit 00. The initial value for this register is 08000800_H (once). An example of the expressions for setting a reduction in the vertical and horizontal directions is shown below (note 2048 is a fixed value):

Reduction in vertical direction	576 -> 490 lines	576/490 = 1.176
	1.176×2048=2408	-> 0968_H
Reduction in horizontal direction	720 -> 648 pixels	720/648 = 1.111
	1.111×2048=2275	-> $08E3_H$

Therefore, $096808E3_H$ is set in CSC.

The capture horizontal pixel register (CHP) is used to limit the number of pixels processed during scaling. It is not used to set scaling values. Clamp processing is performed on the video streaming data outside the values set in CHP. Usually, the defaults for these registers are used.

8.3.2 Up-scaling Function

LIME is able to enlarge the size of a video capture picture by the factor of 2 in both the horizontal and vertical directions. This feature can be used to realize full-screen modes of video input streams which have a resolution less than actual display size. In order to use magnify (up-scaling) mode, the horizontal and vertical factor must be less than one. Do not specify different scaling ways (reduction/enlargement) for horizontal and vertical factors ! Also initialize the following registers as follows :
Set the magnify flag in the L1-layer mode register of the display controller.

Set the picture source size (before magnification) into CMSHP and CMSVL.

Set the final picture size (after magnification) into CMDHP and CMDVL.

An example of the expressions for setting an enlargement in the vertical and horizontal directions is shown below :
If the input picture size is 480x360 and the display picture size is 640x480, then the parameters for each register are as follows.

HSCALE=(480/640)*2048=0x0600
VSCALE=(360/480)*2048=0x0600
CMSHP=0x00f0
CMSVL=0x0168
CMDHP=0x0140
CMDVL=0x01e0
L1WW=0x0280
L1WH=0x01df

Note:

- Smooth continuation operation to Down Scaling mode and Up Scaling mode cannot be performed. The picture disorder of some arises at the time of a change. This is the restrictions for Up Scaling mode and Down Scaling mode using the same interpolate circuit.

8.3.3 Flow of image processing

As for the capture image displayed on L1 layer window, image processing is performed by the following flow.

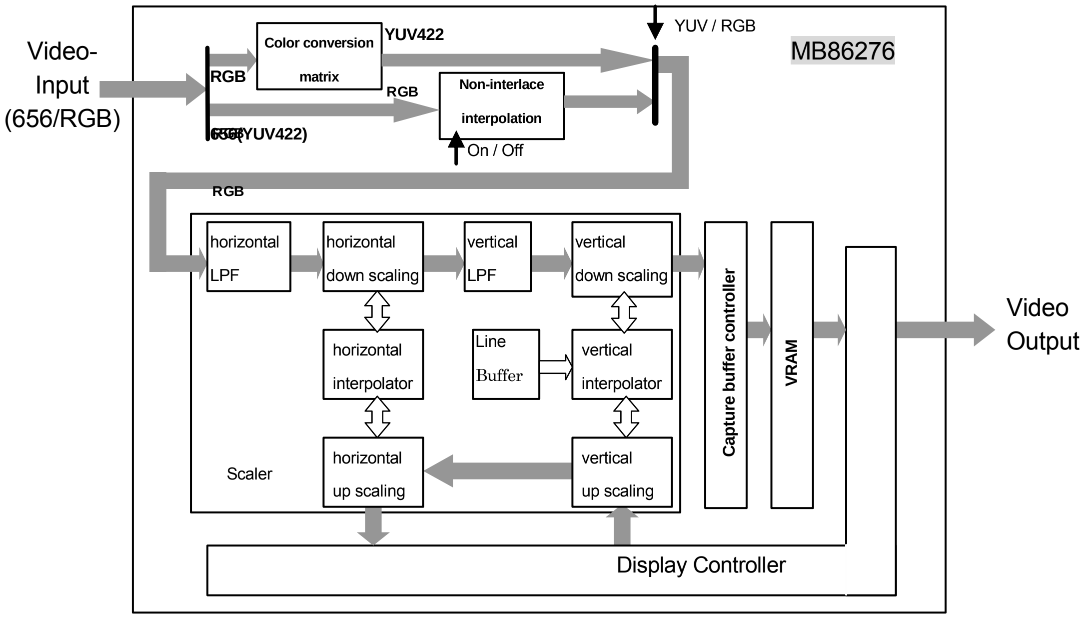


Figure 8.1 Flow of image processing

Non-interlace interpolation processing

When VI of a video capture mode register (VCM) is 0, an interlace screen is interpolated vertically using the data in the same field. A screen is doubled vertically. When VI is 1, it is not interpolated vertically.

Horizontal low-pass filter processing

As a preprocessing when scaling down a picture horizontally, a low-pass filter can be covered horizontally. Regardless of scaling up and scaling down of a picture, ON/OFF is possible for a level low path filter (LPF).

The horizontal low-pass filter consists of FIR filters of five taps. A coefficient is specified in the following register.

CHLPF_Y	Horizontal LPF Luminance element and RGB element coefficient code
CHLPF_C	Horizontal LPF chrominance element coefficient code

The coefficient is specified by the coefficient code in two bits independently by luminance (Y) signal and chrominance (Cb and Cr) signals. The coefficient is a symmetric coefficient.

CHLPF_x	K0	K1	K2	K3	K4
00	0	0	1	0	0
01	0	1/4	2/4	1/4	0
10	0	3/16	10/16	3/16	0
11	3/32	8/32	10/32	10/32	3/32

Horizontal LPF becomes turning off (through) because of the setting of the coefficient code "00".

Note:

- In the case of Native RGB mode (NRGB=1), only a setup of CHLPF_Y code becomes effective.

Down and Up scaling processing of horizontal direction

Please set bit15-00 of capture scale register (CSC) to do the down and up scaling processing of horizontal direction.

Horizontal direction is scaled down before writing in VRAM. Horizontal direction is scaled up after reading from VRAM.

The interpolation filter processing of luminance (Y) signal is done by cubic interpolation (Cubic Interpolate) method. The interpolation filter processing of chrominance (Cb and Cr) signal is done by BiLinear interpolation (BiLinear Interpolate) method. The interpolation filter processing of Native-RGB signal is done by cubic interpolation (Cubic Interpolate) method.

Vertical low-pass filter processing

The low-pass filter can be put on the vertical direction as a preprocessing when the image is scaled down to the vertical direction. Vertical low-pass filter (LPF) can be set to turning on regardless of the scaling up or down of the vertical direction.

A vertical low-pass filter is composed of the FIR filter of three taps. The coefficient is specified by the following register.

CVLPF_Y	Vertical LPF Luminance element and RGB element coefficient code
CVLPF_C	Vertical LPF chrominance element coefficient code

The coefficient is specified by the coefficient code in two bits independently by luminance (Y) signal and chrominance (Cb and Cr) signals. The coefficient is a symmetric coefficient.

CVLPF_x	K0	K1	K2
00	0	1	0
01	1/4	2/4	1/4
10	3/16	10/16	3/16
11	Prohibition of setting		

Vertical LPF becomes turning off (through) because of the setting of the coefficient code "00".

Note:

- In the case of Native RGB mode (NRGB=1), only a setup of CVLPF_Y code becomes effective.

Down and up scaling processing of Vertical direction

Please set bit31-16 of capture scale register (CSC) to do the down and up scaling processing in the vertical direction.

The vertical direction is scaled down before writing in VRAM. The vertical direction is scaled up after reading from VRAM.

The interpolation filter processing of luminance (Y) signal is done by cubic interpolation (Cubic Interpolate) method. The interpolation filter processing of chrominance (Cb and Cr) signal is done by BiLinear interpolation (BiLinear Interpolate) method. The interpolation filter processing of Native-RGB signal is done by cubic interpolation (Cubic Interpolate) method.

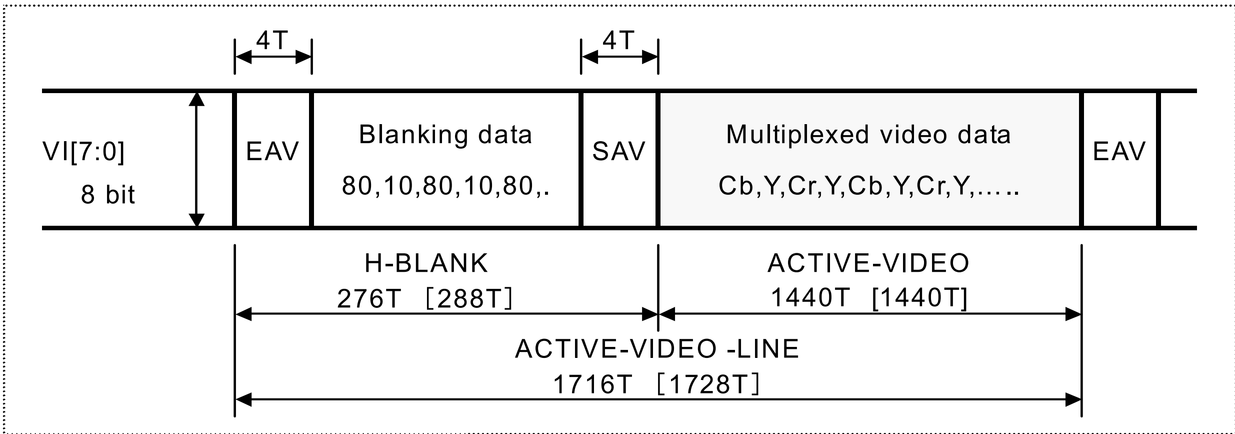
8.4 External video signal input conditions

8.4.1 RTB656 YUV422 input format

The ITU R.BT-656 format is widely used for digital transmission of NTSC and PAL signals. The format corresponds to YUV422. Interlaced video display signals can be captured and displayed non-interlaced with linear interpolation.
When the VIE bit of the video capture mode register (VCM) is 1, LIME is able to capture video stream data from the 8-bit VI pin in synchronization with the CCLK clock. In this mode, only a digital video stream conforming to ITU-RBT656 can be processed. For this reason, a Y,Cb,Cr 4:2:2 format to which timing reference codes are added is used. The video stream is captured according to the timing reference codes; LIME automatically supports both NTSC and PAL. However, to detect error codes, set NTSC/PAL in the VS bit of VCM. If NTSC is not set, reference the number of data in the capture data count register (CDCN). If PAL is not set, reference the number of data in the capture data counter register (CDCP). If the reference data does not match the stream data, bit 4 to bit 0 of the video capture status register (VCS) will be values other than 00000.

1) RTB656 input format VI[7:0]

Synchronous code and image data (Cb,Y,Cr,Y) are input as data of eight multiple bits synchronizing with 27MHz clock, and an valid pixel is transmitted while placed between a synchronous code named SAV and EAV.



SAV : Beginning code of active video data (4 Byte)

EAV : End code of active video data (4 Byte)

T : 27MHz

[ ] : 625/50 series (PAL)

BLANKING PERIOD			TIMING REF-CODE				720 PIXELS YUV4:2:2 DATA									TIMING REF-CODE				BLANKING PERIOD		
…	80	10	FF	00	00	SAV	Cb0	Y0	Cr0	Y1	Cb2	Y2	…	Cr718	Y719	FF	00	00	EAV	80	10	…

2) RTB656 synchronous code (4 Byte) format

Bit \ Word	SYNC code (static)			EAV/SAV
	first	second	third	forth
7	1	0	0	1 (static)
6	1	0	0	F 0:first field 1:second field
5	1	0	0	V 0:ACTIVE-VIDEO 1:VBI
4	1	0	0	H 0:SAV 1:EAV
3	1	0	0	P3 Guard bit
2	1	0	0	P2 Guard bit
1	1	0	0	P1 Guard bit
0	1	0	0	P0 Guard bit

3) SAV/EAV timing base signal

Bit	7	6	5	4	3	2	1	0
Function	static	F	V	H	P3	P2	P1	P0
80	1	0	0	0	0	0	0	0
9D	1	0	0	1	1	1	0	1
AB	1	0	1	0	1	0	1	1
B6	1	0	1	1	0	1	1	0
C7	1	1	0	0	0	1	1	1
DA	1	1	0	1	1	0	1	0
EC	1	1	1	0	1	1	0	0
F1	1	1	1	1	0	0	0	1

80 : SAV code of first field valid pixel period (Active-video)
9D : EAV code of first field valid pixel period (Active-video)
AB : SAV code of first field vertical retrace line period
B6 : EAV code of first field vertical retrace line period
C7 : SAV code of second field valid pixel period (Active-video)
DA : EAV code of second field valid pixel period (Active-video)
EC : SAV code of second field vertical retrace line period
F1 : EAV code of second field vertical retrace line period

8.4.2 RGB input format

There are the two data-processing methods in RGB input video capture function. One is the method of processing with Native RGB. Another is the method of converting RGB into YUV422 by the internal RGB pre processor.

RGB input function is suitable for relatively high speed non-interlaced video signals but the de-interlacing operation is not available in this mode. The maximum input rate is 66Mpixel/sec. RGB component data is 6bit.

Note:

- In Native RGB mode, NRGB=1 is set up.

1) RGB Input Signals

The signals used for RGB video capture are not assigned dedicated terminals but share same pins with other functions.

Name	I/O	Function
RGBCLK	Input	Clock for RGB input
RI5-0	Input	Red component value
GI5-0	Input	Green component value
BI5-0	Input	Blue component value
VSYNCI	Input	Vertical sync for RGB capture
HSYNCI	Input	Horizontal sync for RGB capture

Note :

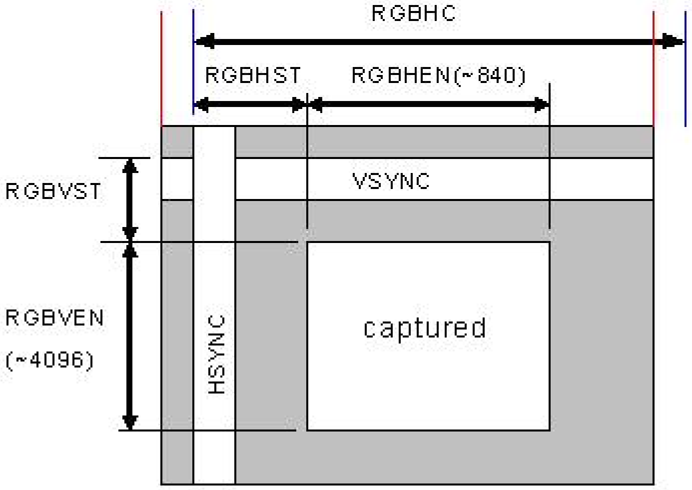
- input pins are shared with the ITU656 input and memory data bus.
- the VIS bit of the VCM (video capture mode) register selects which mode (ITU656 or RGB) is used.

2) Captured Range

Instead of embedded sync code method used in ITU656 mode, the capture range in RGB mode is specified by the following register parameters:

a) RGB input mode of capture: Set RGB666 input flag(VIS) in VCM.
In Native RGB mode, NRGB in VCM =1 is set up.
b) HSYNC Cycle: Set the number of HSYNC Cycles in RGBHC.
c) Horizontal Enable area: Set enables area start position and
enable picture size into RGBHST and RGBHEN.
d) Vertical Enable area: Set enables area start position and
enable picture size into RGBVST and RGBVEN.

The Captured area is defined according to the following parameters. Each parameter is set independently at the respective register.:



RGBHC	RGB input Hsync Cycle
RGBHST	RGB input Horizontal enable area STart position
RGBHEN	RGB input Horizontal enable area size
RGBVST	RGB input Vertical ENable area STart position
RGBVEN	RGB input Vertical ENable area size

Note: The actual parameter settings are little different from the above. The details, please refer “Explanation of Registers”.

e) Convert Matrix Coefficient

In order to change the color conversion matrix, set up RGBCMY, RGBCb, RGBCr and RGBCMb.

Note:

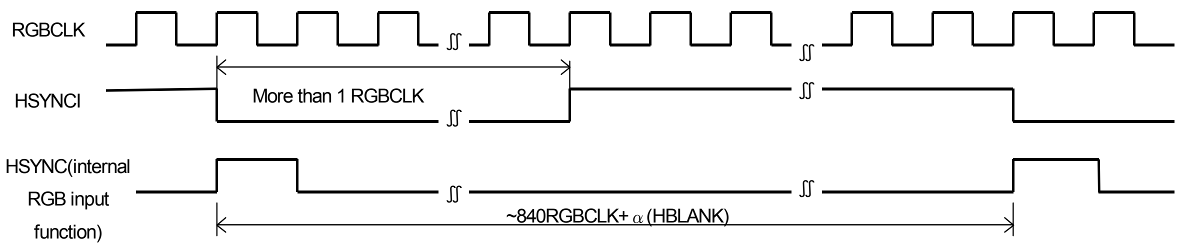
The maximum horizontal enable area size(RGBHEN) which can be captured is 840 pixels. This is the restriction by line buffer size in a video capture module.

3) Input Operation

At the time of a RGB input, the synchronization of data is taken by VSYNC and SYNCI, which are inputted with Data RI, GI and BI.

Input rule of HSYNCI

The positive or negative edge of VINHSYNC is considered as a horizontal synchronization by register setup(HP). Input the signal of 1 or more RGBCLKs –(840+α)RGBCLK cycle.



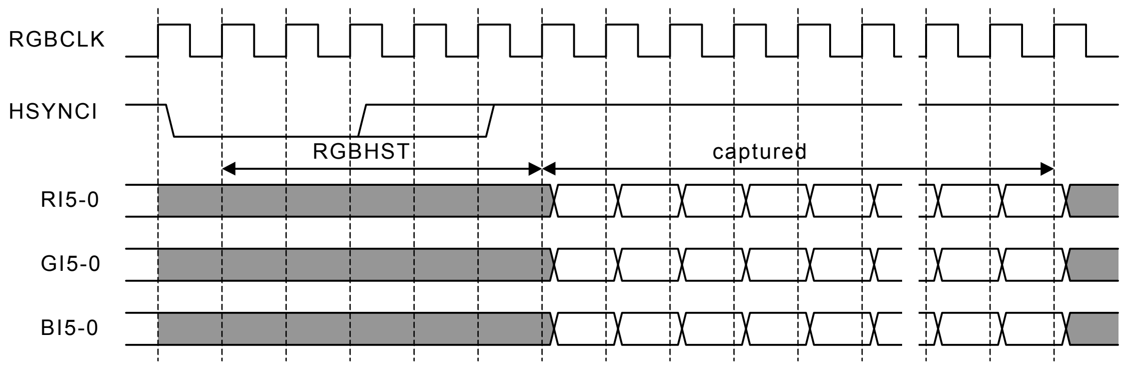
Note:

The maximum horizontal enable area size(RGBHEN) which can be captured is 840 pixels. This is the restriction by line buffer size in a video capture module.

Valid data input rule to HSYNC

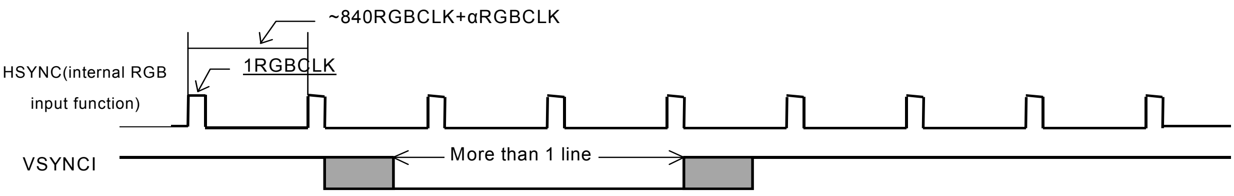
The valid image data input rule to HSYNC is shown.

Input data is inputted synchronizing with HSYNC of each line. (The synchronization of data needs to make a synchronization establish by HSYNC in each line unit. Since the sampling clock of image data is generated from HSYNC, it is because a clock may have jitter per line.)



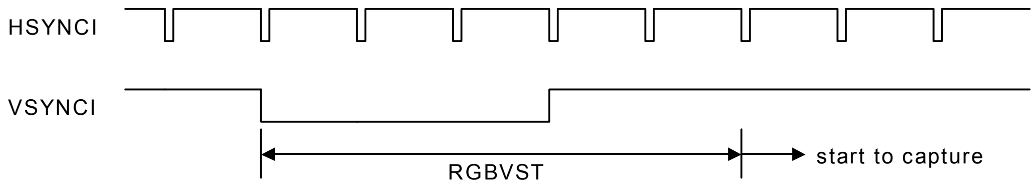
Input rule of VINVSYNC

A VSYNCI signal is synchronizing with HSYNCI. Moreover, VSYNCI is sampled by HSYNCI , and it considers as a VSYNC signal. Width is made into at least one line or more although a VSYNCI signal does not need to synchronize with HSYNC at this time. The positive or negative of VSYNCI is set to VSYNC by register setup(VP).



Valid line input rule to VSYNC

The valid image data input rule to VSYNC is shown.



4) Conversion Operation

RGB input data is converted to YCbCr by the following matrix operation :

Y =	a11*R + a12*G + a13*B + b1		
Cb=	a21*R + a22*G + a23*B + b2	a_{ij} :	10bit signed real (lower 8bit is fraction)
Cr=	a31*R + a32*G + a33*B + b3	b_i:	8bit unsigned integer

Note:
- registers can define each coefficient.
- Cb and Cr components are reduced to half after this operation to form in 4:2:2 format.

8.5 Input Video Signal Parameter Setup

A parameter setup of an input video signal changes with video formats inputted. A register to be set up is shown in the following figure.

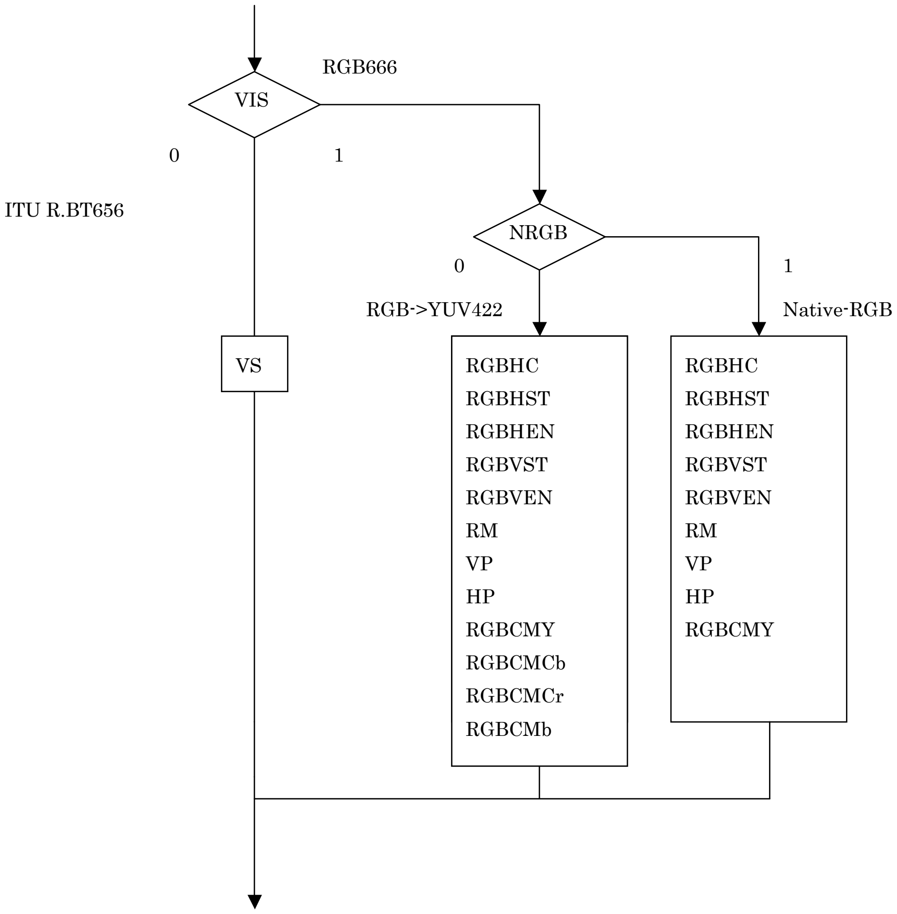


Figure 8.2 A register required for a setup according to format

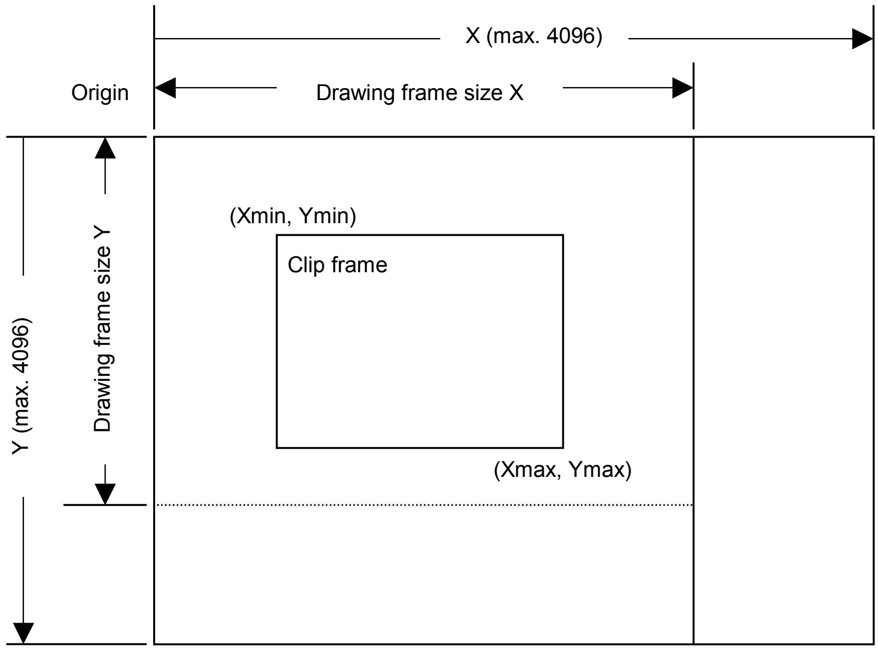
9 DRAWING PROCESSING

9.1 Coordinate System

9.1.1 Drawing coordinates

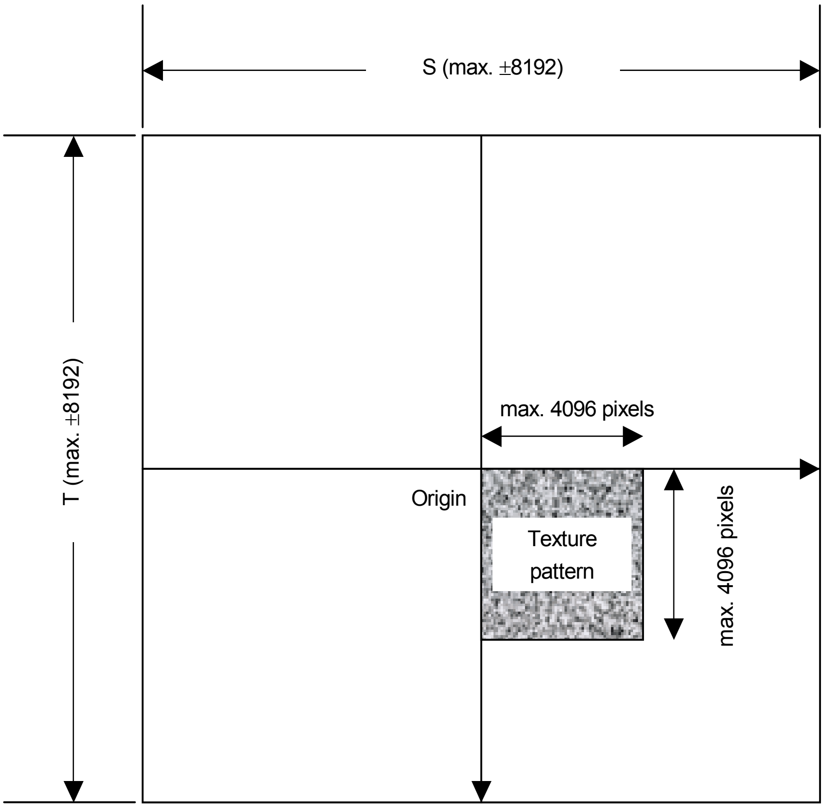
LIME GDC draws data in the drawing frame in the graphics memory that finally uses the drawing coordinates (device coordinates).

Drawing frame is treated as 2D coordinates with the origin at the top left as shown in the figure below. The maximum coordinates is 4096 × 4096. Each drawing frame is located in the Graphics Memory by setting the address of the origin and resolution of X direction (size). Although the size of Y direction does not need to be set, Y coordinates which are max. at drawing must not be overlapped with other area. In addition, at drawing, specifying the clip frame (top left and bottom right coordinates) can prevent the drawing of images outside the clip frame.



9.1.2 Texture coordinates

Texture coordinate is a 2D coordinate system represented as S and T (S: horizontal, T: vertical). Any integer in a range of –8192 to +8191 can be used as the S and T coordinates. The texture coordinates is correlated to the 2D coordinates of a vertex. One texture pattern can be applied to up to 4096 × 4096 pixels. The pattern size is set in the register. When the S and T coordinates exceed the maximum pattern size, the repeat, Clamp or border color option is selected.



9.1.3 Frame buffer

For drawing, the following area must be assigned to the Graphics Memory. The frame size (count of pixels on X direction) is common for these areas.

Drawing frame

The results of drawing are stored in the graphical image data area. Both the direct and indirect color mode are applicable.

Z buffer (Optional function)

Z buffer is required for eliminating hidden surfaces. In 16 bits mode, 2 bytes and in 8 bits mode, 1 byte are required per 1 pixel.

Polygon drawing flag buffer

This area is used for polygon drawing. 1 bit is required per 1 pixel.

9.2 Figure Drawing

9.2.1 Drawing primitives

LIME GDC is supported the rendering command that is compatible with the LIME. The following types of figure drawing primitives are compatible with the LIME.

Point

Line

Triangle

2DLine with XY setup

2DTriangle with XY setup

Polygon

9.2.2 Polygon drawing function

An irregular polygon (including concave shape) is drawn by hardware in the following manner:

1. Execute PolygonBegin command.

Initialize polygon drawing hardware.

2. Draw vertices.

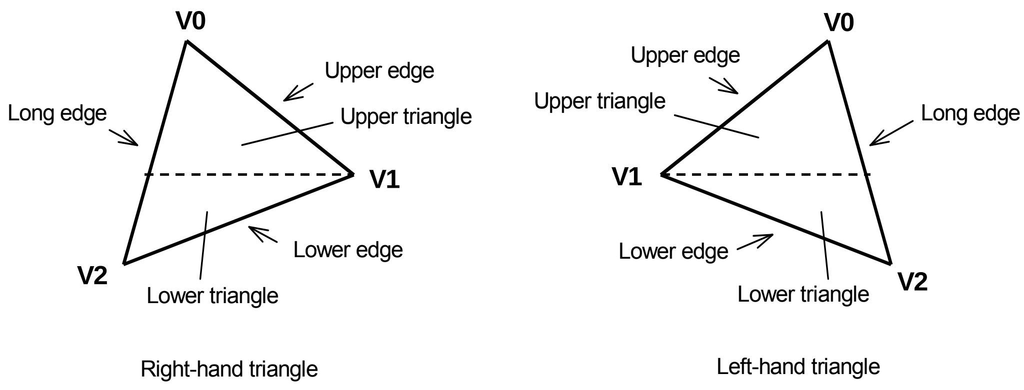
Draw outline of polygon and plot all vertices to polygon draw flag buffer using 2D Triangle with XY setup.

3. Execute PolygonEnd command.

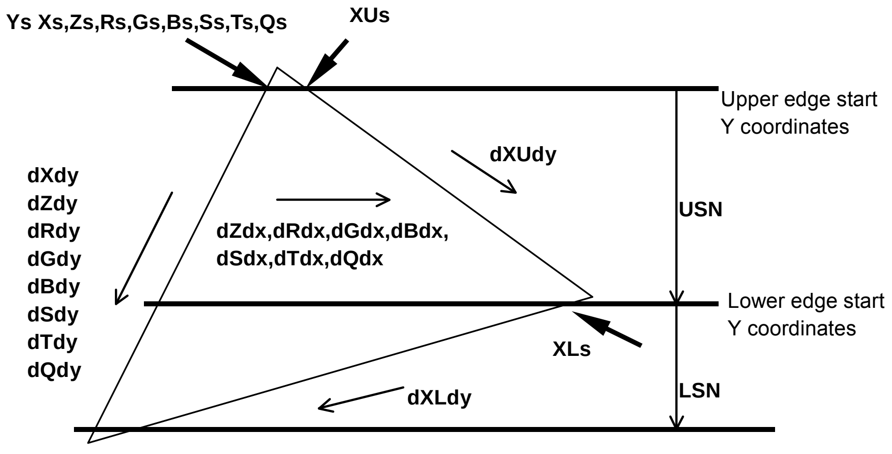
Copy shape in polygon draw flag buffer to drawing frame and fill shape with color or specified tiling pattern.

9.2.3 Drawing parameters

The triangles (Right triangle and Left triangle) are distinguished according to the locations of three vertices as follows (not used for 2D Triangle with XY setup):



The following parameters are required for drawing triangles (for 2D Triangle with XY setup, X and Y coordinates of each vertex are specified).



Note: Be careful about the positional relationship between coordinates Xs, XUs, and XLs.

For example, in the above diagram, when a right-hand triangle is drawn using the parameter that shows the coordinates positional relationship Xs (upper edge start Y coordinates) > XUs or Xs (lower edge start Y coordinates) > XLs, the appropriate picture may not be drawn.

Ys	Y coordinates start position of long edge in drawing triangle
Xs	X coordinates start position of long edge corresponding to Ys
XUs	X coordinates start position of upper edge
XLs	X coordinates start position of lower edge
Zs	Z coordinates start position of long edge corresponding to Ys
Rs	R color value of long edge corresponding to Ys
Gs	G color value of long edge corresponding to Ys
Bs	B color value of long edge corresponding to Ys
Ss	S coordinate of textures of long edge corresponding to Ys
Ts	T coordinate of textures of long edge corresponding to Ys
Qs	Q perspective correction value of texture of long edge corresponding to Ys
dXdy	X DDA value of long edge direction
dXUdy	X DDA value of upper edge direction
dXLdy	X DDA value of lower edge direction
dZdy	Z DDA value of long edge direction
dRdy	R DDA value of long edge direction
dGdy	G DDA value of long edge direction
dBdy	B DDA value of long edge direction
dSdy	S DDA value of long edge direction
dTdy	T DDA value of long edge direction
dQdy	Q DDA value of long edge direction
USN	Count of spans of upper triangle
LSN	Count of spans of lower triangle
dZdx	Z DDA value of horizontal direction
dRdx	R DDA value of horizontal direction
dGdx	G DDA value of horizontal direction
dBdx	B DDA value of horizontal direction
dSdx	S DDA value of horizontal direction
dTdx	T DDA value of horizontal direction
dQdx	Q DDA value of horizontal direction

9.2.4 Anti-aliasing function

LIME GDC performs anti-aliasing to make jaggies less noticeable and smooth on line edges. To use this function at the edges of primitives, redraw the primitive edges with anti-alias lines.

(The edge of line is blended with a frame buffer color at that time. Ideally please draw sequentially from father object.)

9.3 Bit Map Processing

9.3.1 BLT

A rectangular shape in pixel units can be transferred. There are following types of transfer:

1. Transfer from host CPU to Drawing frame memory
2. Transfer between Graphics Memories including Drawing frame

Concerning 1 and 2 above, 2-term logic operation is performed between source and destination data and its result can be stored.

Setting a transparent color enables a drawing of a specific pixel with transmission.

If part of the source and destination of the BLT field are physically overlapped in the display frame, the start address (from which vertex the BLT field to be transferred) must be set correctly.

9.3.2 Pattern data format

LIME GDC can handle three bit map data formats: indirect color mode (8 bits/pixel), direct color mode (16 bits/pixel), and binary bit map (1 bit/pixel).

The binary bit map is used for character/font patterns, where foreground color is used for bitmap = 1 pixel, and background color (background color can be set to be transparent by setting) is applied for bitmap = 0 pixels.

9.4 Texture Mapping

9.4.1 Texture size

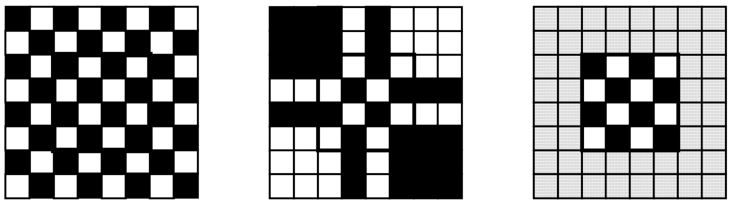
LIME GDC reads texel corresponding to the specified texture coordinates (S, T), and draws that data at the correlated pixel position of the polygon. For the S and T coordinates, the selectable texture data size is any value in the range from 4 to 4096 pixels represented as an exponent of 2.

9.4.2 Texture color

Drawing of 8-/16-bit direct color is supported for the texture pattern. For drawing 8-bit direct color, only point sampling can be specified for texture interpolation; only de-curl can be specified for the blend mode.

9.4.3 Texture Wrapping

If a negative or larger than the specified texture pattern size is specified as the texture coordinates (S, T), according to the setting, one of these options (repeat, Clamp or border) is selected for the 'out-of-range' texture mapping. The mapping image for each case is shown below:



Repeat Cramp Border

Repeat

This just simply masks the upper bits of the applied (S, T) coordinates. When the texture pattern size is 64 × 64 pixels, the lower 6 bits of the integer part of (S, T) coordinates are used for S and T coordinates.

Clamp

When the applied (S, T) coordinates is either negative or larger than the specified texture pattern size, Clamp the (S, T) coordinate as follows instead of texture:

S < 0	S = 0
S > Texture X size – 1	S = Texture X size – 1

Border

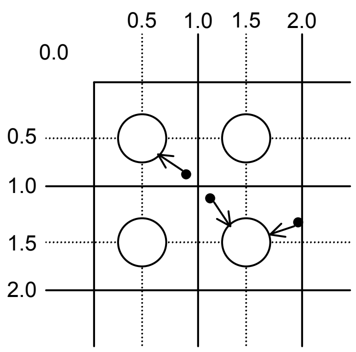
When the applied (S, T) coordinate is either negative or larger than the specified texture pattern size, the outside of the specified texture pattern is rendered in the 'border' color.

9.4.4 Filtering

LIME GDC supports two texture filtering modes: point filtering, and bi-linear filtering.

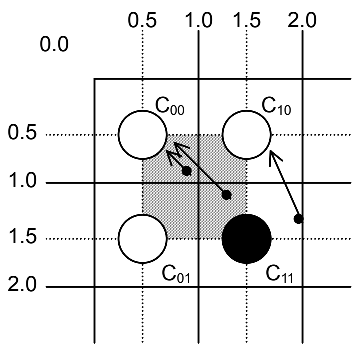
Point filtering

This mode uses the texture pixel specified by the (S, T) coordinates as they are for drawing. The nearest pixel in the texture pattern is chosen according to the calculated (S, T) coordinates.



Bi-linear filtering

The four nearest pixels specified with (S, T) coordinate are blended according to the distance from specified point and used in drawing.



9.4.5 8.4.5 Texture blending

LIME GDC supports the following three blend modes for texture mapping:

Decal

This mode displays the selected texture pixel color regardless of the polygon color.

Modulate

This mode multiplies the native polygon color (C_P) and selected texture pixel color (C_T) and the result is used for drawing. Rendering color is calculated as follows (C_O):

$$C_0 = C_T \times C_P$$

Stencil

This mode selects the display color from the texture color with MSB as a flag.

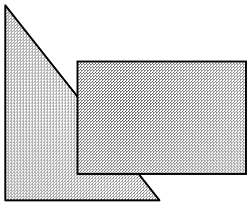
MSB = 1: Texture color

MSB = 0: Polygon color

9.5 Rendering

9.5.1 Tiling

Tiling reads the pixel color from the correlated tiling pattern and maps it onto the polygon. The tiling determines the pixel on the pattern read by pixel coordinates to be drawn, irrespective of position and size of primitive. Since the tiling pattern is stored in the texture memory, this function and texture mapping cannot be used at the same time. Also, the tiling pattern size is limited to within 64 × 64 pixels. (at 16-bit color)



Example of Tiling

9.5.2 Alpha blending

Alpha blending blends the drawn in frame buffer to-be-drawn pixel or pixel already according to the alpha value set in the alpha register. This function cannot be used simultaneously with logic operation drawing. It can be used only when the direct color mode (16 bits/pixel) is used. The blended color C is calculated as shown below when the color of the pixel to be drawn is C_P, the color of frame buffer is C_F, and the alpha value is A:

$$C = C_P \times A + (1\text{-}A) \times C_F$$

The alpha value is specified as 8-bit data. 00h means alpha value 0% and FFh means alpha value 100%. When the texture mapping function is enabled, the following blending modes can be selected:

Normal

Blends post texture mapping color with frame buffer color

Stencil

Uses MSB of texel color for ON/OFF control:

MSB = 1: Texel color

MSB = 0: Frame buffer color

Stencil alpha

Uses MSB of texel color for α/OFF control:

MSB = 1: Alpha blend texel color and current frame buffer color

MSB = 0: Frame buffer color

Note: MSB of frame buffer is drawn MSB of texel in both stencil and stencil alpha mode.

Therefore in case MSB of texel is MSB=0, a color of frame buffer is frame buffer, but MSB of frame buffer is set to 0.

9.5.3 Logic operation

This mode executes a logic operation between the pixel to be drawn and the one already drawn in frame buffer and its result is drawn. Alpha blending cannot be used when this function is specified.

Type	ID	Operation	Type	ID	Operation
CLEAR	0000	0	AND	0001	S & D
COPY	0011	S	OR	0111	S | D
NOP	0101	D	NAND	1110	! (S & D)
SET	1111	1	NOR	1000	! (S | D)
COPY INVERTED	1100	!S	XOR	0110	S xor D
INVERT	1010	!D	EQUIV	1001	! (S xor D)
AND REVERSE	0010	S & !D	AND INVERTED	0100	!S & D
OR REVERSE	1011	S | !D	OR INVERTED	1101	!S | D

9.5.4 Hidden plane management (Optional function)

LIME GDC supports the Z buffer for hidden plane management.

This function compares the Z value of a new pixel to be drawn and the existing Z value in the Z buffer. Display/not display is switched according to the Z-compare mode setting. Define the Z-buffer access options in the ZWRITEMASK mode.

The Z compare operation type is determined by the Z compare mode.

Either 16 or 8 bits can be selected for the Z-value.

ZWRITEMASK	1	Compare Z values, no Z value write overwrite
	0	Compare Z values, Z value write

Z Compare mode	Code	Condition
NEVER	000	Never draw
ALWAYS	001	Always draw
LESS	010	Draw if pixel Z value < current Z buffer value
LEQUAL	011	Draw if pixel Z value ≤ current Z buffer value
EQUAL	100	Draw if pixel Z value = current Z buffer value
GEQUAL	101	Draw if pixel Z value ≥ current Z buffer value
GREATER	110	Draw if pixel Z value > current Z buffer value
NOTEQUAL	111	Draw if pixel Z value ! = current Z buffer value

9.6 Drawing Attributes

9.6.1 Line drawing attributes

In drawing lines, the following attributes apply:

Line Drawing Attributes

Drawing Attribute	Description
Line width	Line width selectable in range of 1 to 32 pixels
Broken line	Specify broken line pattern in 32-bit data
Anti-alias	Line edge smoothed when anti-aliasing enabled

9.6.2 Triangle drawing attributes

In drawing triangles, the following attributes apply (these attributes are disabled in 2DTriangle with XY setup). Texture mapping and tiling have separated texture attributes:

Triangle Drawing Attributes

Drawing Attribute	Description
Shading	Gouraud shading or flat shading selectable
Alpha blending	Set alpha blending enable/disable per polygon
Alpha blending coefficient	Set color blending ratio of alpha blending

9.6.3 Texture attributes

In texture mapping, the following attributes apply:

Texture Attributes

Drawing Attribute	Description
Texture mode	Select either texture mapping or tiling
Texture filter	Select either point sampling or bi-linear filtering
Texture coordinates correction	Select either linear or perspective correction
Texture wrap	Select either repeat or Clamp of texture pattern
Texture blend mode	Select either decal or modulate

9.6.4 BLT attributes

In BLT drawing, the following attributes apply:

BLT Attributes

Drawing Attribute	Description
Logic operation mode	Specify two source logic operation mode
Transparency mode	Set transparent copy mode and transparent color
Alpha map mode	Blend a color according to alpha map

9.6.5 Character pattern drawing attributes

Character Pattern Drawing

Drawing Attribute	Description
Character pattern enlarge/shrink	Vertical and Horizontal × 2, Horizontal × 2, Vertical and Horizontal × 1/2, Horizontal × 1/2
Character pattern color	Set character color and background color
Transparency/non-transparency	Set background color to transparency/non-transparency

10 DISPLAY LIST

10.1 Overview

Display list is a set of display list commands, parameters and pattern data. All display list commands stored in a display list are executed consequently.

The display list is transferred to the display list FIFO by the following method:

Transfer from graphics memory to display FIFO by register setting

Display list Command-1
Data 1-1
Data 1-2
Data 1-3
Display list Command-2
Data 2-1
Data 2-2
Data 2-3
...

Display List

10.1.1 Header format

The format of the display list header is shown below.

Format List

<table>
<tr><th>Format</th><th>31 ... 24</th><th>23 ... 16</th><th colspan="3">15 ... 0</th></tr>
<tr><td>Format 1</td><td>Type</td><td>Reserved</td><td colspan="3">Reserved</td></tr>
<tr><td>Format 2</td><td>Type</td><td>Count</td><td colspan="3">Address</td></tr>
<tr><td>Format 3</td><td>Type</td><td>Reserved</td><td colspan="2">Reserved</td><td>Vertex</td></tr>
<tr><td>Format 4</td><td>Type</td><td>Reserved</td><td>Reserved</td><td>Flag</td><td>Vertex</td></tr>
<tr><td>Format 5</td><td>Type</td><td>Command</td><td colspan="3">Reserved</td></tr>
<tr><td>Format 6</td><td>Type</td><td>Command</td><td colspan="3">Count</td></tr>
<tr><td>Format 7</td><td>Type</td><td>Command</td><td colspan="2">Reserved</td><td>Vertex</td></tr>
<tr><td>Format 8</td><td>Type</td><td>Command</td><td>Reserved</td><td>Flag</td><td>Vertex</td></tr>
<tr><td>Format 9</td><td>Type</td><td>Reserved</td><td>Reserved</td><td colspan="2">Flag</td></tr>
<tr><td>Format 10</td><td>Type</td><td>Reserved</td><td colspan="3">Count</td></tr>
<tr><td rowspan="2">Format 11</td><td>Type</td><td>Reserved</td><td colspan="3">Reserved</td></tr>
<tr><td colspan="5">Count</td></tr>
</table>

Description of Each Field

Type	Display list type
Command	Command
Count	Count of data excluding header
Address	Address value used at data transfer
Vertex	Vertex number
Flag	Attribute flag peculiar to display list command

Vertex Number Specified in Vertex Code

Vertex	Vertex number (Line)	Vertex number (Triangle)
00	V0	V0
01	V1	V1
10	Setting prohibited	V2
11	Setting prohibited	Setting prohibited

10.2 Rendering Command

10.2.1 Command list

The following table lists LIME GDC rendering commands and their command codes.

Type	Command	Description
Nop	—	No operation
Interrupt	—	Interrupt request to host CPU
Sync	—	Synchronization with events
SetRegister	—	Sets data to register
SetVertex2i	Normal	Sets data to 2D Triangle with XY setup vertex register
	PolygonBegin	Initializes border rectangle calculation of multiple vertices random shape
Draw	PolygonEnd	Clears polygon flag after drawing polygon
	Flush_FB/Z	Flushes drawing pipelines
DrawPixel	Pixel	Draws point
DrawPixelZ	PixelZ	Draws point with Z
DrawLine	Xvector	Draws line (principal axis X)
	Yvector	Draws line (principal axis Y)
	AntiXvector	Draws line with anti-alias option (principal axis X)
	AntiYvector	Draws line with anti-alias option (principal axis Y)
DrawLine2i DrawLine2iP	ZeroVector	Draws 2D Line with XY setup (with vertex 0 as starting point)
	OneVector	Draws 2D Line with XY setup (with vertex 1 as starting point)
DrawTrap	TrapRight	Draws right triangle
	TrapLeft	Draws left triangle
DrawVertex2i DrawVertex2iP	TriangleFan	Draws 2D Triangle with XY setup
	FlagTriangleFan	Draws 2D Triangle with XY setup for multiple vertices random shape
DrawRectP	BltFill	Draws rectangle with single color
	ClearPolyFlag	Clears polygon flag buffer
DrawBitmapP	BltDraw	Draws Blt (16-bit)
	Bitmap	Draws binary bit map (character)
DrawBitmapLargeP	BltDraw	Draws Blt (32-bit)
BltCopyP BltCopy- AlternateP	TopLeft	Blt transfer from top left coordinates
	TopRight	Blt transfer from top right coordinates
	BottomLeft	Blt transfer from bottom left coordinates
	BottomRight	Blt transfer from bottom right coordinates
LoadTextureP	LoadTexture	Loads texture pattern
	LoadTILE	Loads tile pattern
BltTextureP	LoadTexture	Loads texture pattern from local memory
	LoadTILE	Loads tile pattern from local memory
BltCopyAlt- AlphaBlendP	—	Alpha blending is supported (see the alpha map). BltCopyAlternateP

Type Code Table

Type	Code
DrawPixel	0000_0000
DrawPixelZ	0000_0001
DrawLine	0000_0010
DrawLine2i	0000_0011
DrawLine2iP	0000_0100
DrawTrap	0000_0101
DrawVertex2i	0000_0110
DrawVertex2iP	0000_0111
DrawRectP	0000_1001
DrawBitmapP	0000_1011
BitCopyP	0000_1101
BitCopyAlternateP	0000_1111
LoadTextureP	0001_0001
BltTextureP	0001_0011
BltCopyAltAlphaBlendP	0001_1111
SetVertex2i	0111_0000
SetVertex2iP	0111_0001
Draw	1111_0000
SetRegister	1111_0001
Sync	1111_1100
Interrupt	1111_1101
Nop	1111_1111

Command Code Table (1)

Command	Code
Pixel	000_00000
PixelZ	000_00001
Xvector	001_00000
Yvector	001_00001
XvectorNoEnd	001_00010
YvectorNoEnd	001_00011
XvectorBlpClear	001_00100
YvectorBlpClear	001_00101
XvectorNoEndBlpClear	001_00110
YvectorNoEndBlpClear	001_00111
AntiXvector	001_01000
AntiYvector	001_01001
AntiXvectorNoEnd	001_01010
AntiYvectorNoEnd	001_01011
AntiXvectorBlpClear	001_01100
AntiYvectorBlpClear	001_01101
AntiXvectorNoEndBlpClear	001_01110
AntiYvectorNoEndBlpClear	001_01111
ZeroVector	001_10000
Onevector	001_10001
ZeroVectorNoEnd	001_10010
OnevectorNoEnd	001_10011
ZeroVectorBlpClear	001_10100
OnevectorBlpClear	001_10101
ZeroVectorNoEndBlpClear	001_10110
OnevectorNoEndBlpClear	001_10111
AntiZeroVector	001_11000
AntiOnevector	001_11001
AntiZeroVectorNoEnd	001_11010
AntiOnevectorNoEnd	001_11011
AntiZeroVectorBlpClear	001_11100
AntiOnevectorBlpClear	001_11101
AntiZeroVectorNoEndBlpClear	001_11110
AntiOnevectorNoEndBlpClear	001_11111

Command Code Table (2)

Command	Code
BltFill	010_00001
BltDraw	010_00010
Bitmap	010_00011
TopLeft	010_00100
TopRight	010_00101
BottomLeft	010_00110
BottomRight	010_00111
LoadTexture	010_01000
LoadTILE	010_01001
TrapRight	011_00000
TrapLeft	011_00001
TriangleFan	011_00010
FlagTriangleFan	011_00011
Flush_FB	110_00001
Reserved	110_00010
PolygonBegin	111_00000
PolygonEnd	111_00001
ClearPolyFlag	111_00010
Normal	111_11111

10.2.2 Details of rendering commands

All parameters belonging to their command are stored in relevant registers. The definition of each parameter is explained in the section of each command.

Nop (Format1)

31 - 24	23 - 16	15 - 0
Nop	Reserved	Reserved

No operation

Interrupt (Format1)

31 - 24	23 - 16	15 - 0
Interrupt	Reserved	Reserved

The ***Interrupt*** command generates interrupt request to host CPU.

Sync (Format9)

31 - 24	23 - 16	15 - 5	4 - 0
Sleep	Reserved	Reserved	flag

The ***Sync*** command suspends all subsequent display list processing until event set in flag detected.

Flag:

Bit number	4	3	2	1	0
Bit field name	Reserved	Reserved	Reserved	Reserved	VBLANK

Bit 0 VBLANK

VBLANK Synchronization

0 No operation

1 Wait for VSYNC detection

SetRegister (Format2)

31 – 24	23 – 16	15 – 0
SetRegister	Count	Address
(Val 0)		
(Val 1)		
...		
(Val n)		

The ***SetRegister*** command sets data to sequential registers.

Count: Data word count (in double-word unit)

Address: Register address

Set the value of the address for ***SetRegister*** given in the register list.
When transferring two or more data, set the starting register address.

SetVertex2i (Format8)

31 – 24	23 – 16	15 – 4	3 – 2	1 – 0
SetVertex2i	Command	Reserved	flag	vertex
Xdc				
Ydc				

The ***SetVertex2i*** command sets vertices data for 2D Line with XY setup or 2D Triangle with XY setup to registers.

Commands:

Normal — Sets vertex data (X, Y).

PolygonBegin — Starts calculation of circumscribed rectangle for random shape to be drawn. Calculate vertices of rectangle including all vertices of random shape defined between ***PolygonBegin*** and ***PolygonEnd***.

Flag: Not used

SetVertex2iP (Format8)

31 – 24	23 – 16	15 – 4	3 – 2	1 – 0
SetVertex2i	Command	Reserved	flag	vertex
Ydc		Xdc		

The ***SetVertex2iP*** command sets vertices data for 2D Line with XY setup or 2D Triangle with XY setup to registers.

Only the integer (packed format) can be used to specify these vertices.

Commands:

Normal — Sets vertices data.

PolygonBegin — Starts calculation of circumscribed rectangle of random shape to be drawn. Calculate vertices of rectangle including all vertices of random shape defined between ***PolygonBegin*** and ***PolygonEnd***.

Flag: Not used

Draw (Format5)

31 ... 24	23 ... 16	15 ... 0
Draw	Command	Reserved

The ***Draw*** command executes drawing command. All parameters required for drawing command execution must be set at their appropriate registers.

Commands:

PolygonEnd	Draws polygon end. Fills random shape with color according to flags generated by ***FlagTriangleFan*** command and information of circumscribed rectangle generated by ***PolygonBegin*** command.
Flush_FB	Flushes drawing data in the drawing pipeline into the graphics memory. Place this command at the end of the display list.
Flush_Z	Flushes Z value data in the drawing pipeline into the graphics memory. When using the Z buffer, place this command together with the ***Flush_FB*** command at the end of the display list.

DrawPixel (Format5)

31 ... 24	23 ... 16	15 ... 0
DrawPixel	Command	Reserved
PXs		
PYs		

The ***DrawPixel*** command draws pixel.

Command:

Pixel	Draws pixel without Z value.

DrawPixelZ (Format5)

31 ... 24	23 ... 16	15 ... 0
DrawPixel	Command	Reserved
PXs		
PYs		
PZs		

The ***DrawPixelZ*** command draws pixel with Z value.

Command:

PixelZ	Draws pixel with Z value.

DrawLine (Format5)

31 … 24	23 … 16	15 … 0
DrawLine	Command	Reserved
LPN		
LXs		
LXde		
LYs		
LYde		

The ***DrawLine*** command draws line. It starts drawing after setting all parameters at line draw registers.

Commands:

Xvector	Draws line (principal axis X).
Yvector	Draws line (principal axis Y).
XvectorNoEnd	Draws line (principal axis X, and without end point drawing).
YvectorNoEnd	Draws line (principal axis Y, and without end point drawing).
XvectorBlpClear	Draws line (principal axis X, and prior to drawing, broken line pattern reference position cleared).
YvectorBlpClear	Draws line (principal axis Y, and prior to drawing, broken line pattern reference position cleared).
XvectorNoEndBlpClear	Draws line (principal axis X, without end point drawing and prior to drawing, broken line pattern reference position cleared).
YvectorNoEndBlpClear	Draws line (principal axis Y, without end point drawing and prior to drawing, broken line pattern reference position cleared).
AntiXvector	Draws anti-alias line (principal axis X).
AntiYvector	Draws anti-alias line (principal axis Y).
AntiXvectorNoEnd	Draws anti-alias line (principal axis X, and without end point drawing).
AntiYvectorNoEnd	Draws anti-alias line (principal axis Y, and without end point drawing).
AntiXvectorBlpClear	Draws anti-alias line (principal axis X and prior to drawing, broken line pattern reference position cleared).
AntiYvectorBlpClear	Draws anti-alias line (principal axis Y and prior to drawing, broken line pattern reference position cleared).
AntiXvectorNoEndBlpClear	Draws anti-alias line (principal axis X, without end point drawing and prior to drawing, broken line pattern reference position cleared).
AntiYvectorNoEndBlpClear	Draws anti-alias line (principal axis Y, without end point drawing and prior to drawing, broken line pattern reference position cleared).

DrawLine2i (Format7)

31–24	23–16	15–1	0
DrawLine2i	Command	Reserved	vertex
LFXs		0	
LFYs		0	

The ***DrawLine2i*** command draws 2DLine with XY setup. It starts drawing after setting parameters at the 2DLine with XY setup drawing registers. Integer data can only be used for coordinates.

Commands:

ZeroVector	Draws line from vertex 0 to vertex 1.
OneVector	Draws line from vertex 1 to vertex 0.
ZeroVectorNoEnd	Draws line from vertex 0 to vertex 1 (without drawing end point).
OneVectorNoEnd	Draws line from vertex 1 to vertex 0 (without drawing end point).
ZeroVectorBlpClear	Draws line from vertex 0 to vertex 1 (principal axis X, and prior to drawing, broken line pattern reference position cleared).
OneVectorBlpClear	Draws line from vertex 1 to vertex 0 (principal axis Y, and prior to drawing, broken line pattern reference position cleared).
ZeroVectorNoEndBlpClear	Draws line from vertex 0 to vertex 1 (principal axis X, without end point drawing and prior to drawing, broken line pattern reference position cleared).
OneVectorNoEndBlpClear	Draws line from vertex 1 to vertex 0 (principal axis Y, without end point drawing and prior to drawing, broken line pattern reference position cleared).
AntiZeroVector	Draws anti-alias line from vertex 0 to vertex 1.
AntiOneVector	Draws anti-alias line from vertex 1 to vertex 0.
AntiZeroVectorNoEnd	Draws anti-alias line from vertex 0 to vertex 1 (without end point).
AntiOneVectorNoEnd	Draws anti-alias line from vertex 1 to vertex 0 (without end point).
AntiZeroVectorBlpClear	Draws anti-alias line from vertex 0 to vertex 1 (principal axis X and prior to drawing, broken line pattern reference position cleared).
AntiOneVectorBlpClear	Draws anti-alias line from vertex 1 to vertex 0 (principal axis Y and prior to drawing, broken line pattern reference position cleared).
AntiZeroVectorNoEndBlpClear	Draws anti-alias line from vertex 0 to vertex 1 (principal axis X, without end point drawing and prior to drawing, broken line pattern reference position cleared).
AntiOneVectorNoEndBlpClear	Draws anti-alias line from vertex 1 to vertex 0 (principal axis Y, without end point drawing and prior to drawing, broken line pattern reference position cleared).

DrawLine2iP (Format7)

31 ... 24	23 ... 16	15 ...	0
DrawLine2iP	Command	Reserved	vertex
LFYs		LFXs	

The ***DrawLine2iP*** command draws high-speed 2DLine. It starts drawing after setting parameters at high-speed 2DLine drawing registers. Only packed integer data can be used for coordinates.

Commands:

ZeroVector	Draws line from vertex 0 to vertex 1.
OneVector	Draws line from vertex 1 to vertex 0.
ZeroVectorNoEnd	Draws line from vertex 0 to vertex 1 (without drawing end point).
OneVectorNoEnd	Draws line from vertex 1 to vertex 0 (without drawing end point).
ZeroVectorBlpClear	Draws line from vertex 0 to vertex 1 (principal axis X, and prior to drawing, broken line pattern reference position cleared).
OneVectorBlpClear	Draws line from vertex 1 to vertex 0 (principal axis Y, and prior to drawing, broken line pattern reference position cleared).
ZeroVectorNoEndBlpClear	Draws line from vertex 0 to vertex 1 (principal axis X, without end point drawing and prior to drawing, broken line pattern reference position cleared).
OneVectorNoEndBlpClear	Draws line from vertex 1 to vertex 0 (principal axis Y, without end point drawing and prior to drawing, broken line pattern reference position cleared).
AntiZeroVector	Draws anti-alias line from vertex 0 to vertex 1.
AntiOneVector	Draws anti-alias line from vertex 1 to vertex 0.
AntiZeroVectorNoEnd	Draws anti-alias line from vertex 0 to vertex 1 (without end point).
AntiOneVectorNoEnd	Draws anti-alias line from vertex 1 to vertex 0 (without end point).
AntiZeroVectorBlpClear	Draws anti-alias line from vertex 0 to vertex 1 (principal axis X and prior to drawing, broken line pattern reference position cleared).
AntiOneVectorBlpClear	Draws anti-alias line from vertex 1 to vertex 0 (principal axis Y and prior to drawing, broken line pattern reference position cleared).
AntiZeroVectorNoEndBlpClear	Draws anti-alias line from vertex 0 to vertex 1 (principal axis X, without end point drawing and prior to drawing, broken line pattern reference position cleared).
AntiOneVectorNoEndBlpClear	Draws anti-alias line from vertex 1 to vertex 0 (principal axis Y, without end point drawing and prior to drawing, broken line pattern reference position cleared).

DrawTrap (Format5)

31 … 24	23 … 16	15 … 0
DrawTrap	Command	Reserved
Ys		0
Xs		
DXdy		
XUs		
DXUdy		
XLs		
DXLdy		
USN		0
LSN		0

The ***DrawTrap*** command draws Triangle. It starts drawing after setting parameters at the Triangle Drawing registers (coordinates).

Commands:

TrapRight	Draws right triangle.
TrapLeft	Draws left triangle.

DrawVertex2i (Format7)

31 … 24	23 … 16	15 … 1	0
DrawVertex2i	Command	Reserved	vertex
Xdc		0	
Ydc		0	

The ***DrawVertex2i*** command draws 2D Triangle with XY setup

It starts triangle drawing after setting parameters at 2D Triangle Drawing registers.

Commands:

TriangleFan	Draws 2D Triangle with XY setup.
FlagTriangleFan	Draws 2D Triangle with XY setup for polygon drawing in the flag buffer.

DrawVertex2iP (Format7)

31 … 24	23 … 16	15 … 1	0
DrawVertex2iP	Command	Reserved	vertex
Ydc		Xdc	

The ***DrawVertex2iP*** command draws 2D Triangle with XY setup.

It starts drawing after setting parameters at 2D Triangle with XY setup Drawing registers

Only the packed integer format can be used for vertex coordinates.

Commands:

TriangleFan	Draw 2D Triangle with XY setup.
FlagTriangleFan	Draws 2D Triangle with XY setup for polygon drawing in the flag buffer.

DrawRectP (Format5)

31 — 24	23 — 16	15 — 0
DrawRectP	Command	Reserved
RYs		RXs
RsizeY		RsizeX

The ***DrawRectP*** command fills rectangle. The rectangle is filled with the current color after setting parameters at the rectangle registers. Please set XRES(X resolution) to in 8 byte units when using this command.

Only the BitBlt command allows XRES to be in 8-byte units or boundary. For all other purposes, XRES has to be in 64-byte units. Therefore, unless BitBlt is the only rendering engine function being used, XRES must be set in 64-byte units. In general, it is also recommended for XRES to be in 64-byte units.

Commands:

BltFill	Fills rectangle with current color (single).
ClearPolyFlag	Fills ***polygon drawing*** flag buffer area with 0. The size of drawing frame is defined in RsizeX,Y. Must set RXs[3:0] and RsizeX[3:0] as 0000. (16pixel aligned) Drawing clipping is not work for this command.

DrawBitmapP (Format6)

31 — 24	23 — 16	15 — 0
DrawBitmapP	Command	Count
RYs		RXs
RsizeY		RsizeX
(Pattern 0)		
(Pattern 1)		
...		
(Pattern n)		

The ***DrawBitmapP*** command draws rectangle patterns. Please set XRES(X resolution) to in 8 byte units when using this command.

Commands:

BltDraw	Draws rectangle of 8 bits/pixel or 16 bits/pixel.
DrawBitmap	Draws binary bitmap character pattern. Bit 0 is drawn in transparent or background color, and bit 1 is drawn in foreground color.

DrawBitmapLargeP (Format11)

31 — 24	23 — 16	15 — 0
DrawBitmapLargeP	Command	Reserved
Count		
Rys		Rxs
RsizeY		RsizeX
(Pattern 0)		
(Pattern 1)		
...		
(Pattern n)		

The ***DrawBitmapP*** command draws rectangle patterns.

The parameter(count field) could be used up to 32-bit(*1) unlike DrawBitmapP.

(*1: The data format of counter field is signed long. Thus actually it is possible to use up to 31-bit.)

Please set XRES(X resolution) to in 8 byte units when using this command.

Commands:

BltDraw	Draws rectangle of 8 bits/pixel or 16 bits/pixel.

BltCopyP (Format5)

31 – 24	23 – 16	15 – 0
BltCopyP	Command	Reserved
SRYs		SRXs
DRYs		DRXs
BRsizeY		BRsizeX

The ***BltCopyP*** command copies rectangle pattern within drawing frame. Please set XRES(X resolution) to in 8 byte units when using this command.

Only the BitBlt command allows XRES to be in 8-byte units or boundary. For all other purposes, XRES has to be in 64-byte units. Therefore, unless BitBlt is the only rendering engine function being used, XRES must be set in 64-byte units. In general, it is also recommended for XRES to be in 64-byte units.

Commands:

TopLeft	Starts BitBlt transfer from top left coordinates.
TopRight	Starts BitBlt transfer from top right coordinates.
BottomLeft	Starts BitBlt transfer from bottom left coordinates.
BottomRight	Starts BitBlt transfer from bottom right coordinates.

BltCopyAlternateP (Format5)

31 – 24	23 – 16	15 – 0
BltCopyAlternateP	Command	Reserved
SADDR		
SStride		
SRYs		SRXs
DADDR		
DStride		
DRYs		DRXs
BRsizeY		BRsizeX

The ***BltCopyAlternateP*** command copies rectangle between two separate drawing frames.

Please set XRES(X resolution) to in 8 byte units when using this command. And please set SStride and DStride to in 8 byte units.

Command:

TopLeft	Starts BitBlt transfer from top left coordinates. Drawing clipping is not wok for this command.

BltCopyAltAlphaBlendP (Format5)

31 24	23 16	15 0
BltCopyAlternateP	Command	Reserved
SADDR		
SStride		
SRYs		SRXs
BlendStride		
BlendRYs		BlendRXs
DRYs		DRXs
BRsizeY		BRsizeX

The **BltCopyAltAlphaBlendP** command performs alpha blending for the source (specified using SADDR, SStride, SRXs, SRXy) and the alpha map (specified using ABR (alpha base address), BlendStride, BlendRXs, BlendRYs) and then copies the result of the alpha blending to the destination (specified using FBR (frame buffer base address), XRES (X resolution), DRXs, and DRYs).

Please set XRES(X resolution) to in 8 byte units when using this command. And please set SStride and BlendStride to in 8 byte units.

Only the BitBlt command allows XRES to be in 8-byte units or boundary. For all other purposes, XRES has to be in 64-byte units. Therefore, unless BitBlt is the only rendering engine function being used, XRES must be set in 64-byte units. In general, it is also recommended for XRES to be in 64-byte units.

Command:

reserved	Set 0000_0000 to maintain future compatibility.

11 GDC Register MAP

Terms appeared in this chapter are explained below:

1. Register address
   Indicates address of register
2. Bit number
   Indicates bit number
3. Bit field name
   Indicates name of each bit field included in register
4. R/W
   Indicates access attribute (read/write) of each field
   Each symbol shown in this section denotes the following:

R0	“0” always read at read. Write access is Don’t care.
W0	Only “0” can be written.
R	Read enabled
W	Write enabled
RX	Read enabled (read values undefined)
RW	Read and write enabled
RW0	Read and write 0 enabled

5. Initial value
   Indicates initial value of immediately before the reset of each bit field.
6. Handling of reserved bits
   Reserved bits should write “0”.

11.1 Local memory register list

11.1.1 Host interface register list

Base = HostBase

Offset	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000	DTC																															
									DTC																							
004									DST								DRM								DSU							
																DST								DRM					DNA	DAM	DBM	DW
008																	LTS								DTS							
																								LTS								DTS
010	LSTA																															
																																LSTA
018	DRQ																															
																																DRQ
020	IST																															
																												IST				
024	IMASK																															
																												IMASK				
02C																									SRST							
																																SRST
038	CCF																															
															COT																	
040	LSA																															
								LSA																								
044	LCO																															
									LCO																							
048																									LREQ							
																																LREQ
05C																									RSW							
																																RSW
500	DMA_ST_ADR																															
							DMA_ST_ADR																									
504	DMA_ED_ADR																															
							DMA_ED_ADR																									
508	ERR_ADR																															
							ERR_ADR																									

Offset	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
50C	ERR_DETECT																															
510	INT_MSK																															
514	XINT_ACT																															

11.1.2 I²C interface register list

Base = I²CBase

Offset	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000	Reserved																								BSR							
004	Reserved																								BCR							
008	Reserved																								CCR							
00C	Reserved																								ADR							
010	Reserved																								DAR							
014	Access Prohibitation																															
018	Access Prohibitation																															
01C	Access Prohibitation																															

11.1.3 GPIO register list

Base = PIOBase

Offset	Register	Bits	Field
40	GPIOC1	31–16	GPIO_is_out
		15–0	GPIO_inout
44	GPIOC2	31–16	GPIO_force
		15–0	GPIO_xor
4C	PIC1	31–20	
		19	OFE
		18	WTO
		17	RTO
		16	S1
		15–0	GPIO_INT_enable
50	PIC2	31–16	
		15–0	GPIO_INT_polarity
54	PIC3	31–16	
		15–0	GPIO_INT_mode
80	PIST	31–20	
		19	OFE
		18	WTO
		17	RTO
		16	S1
		15–0	GPIO_INT_status

11.1.4 Graphics memory interface register list

Base = HostBase

Offset	Register	Bits	Field
FFFC	MMR	31	
		30	TWR
		29–27	
		26	–
		25	
		24–23	TRRD
		22–19	TRC
		18–17	TRP
		16–14	TRAS
		13–12	TRCD
		11–10	LOWD
		9–7	RTS
		6–4	SAW
		3	ASW
		2–0	CL

11.1.5 Display controller register list

Base = DisplayBase

<table>
<tr><th>Offset</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td rowspan="2">000</td><td colspan="32">DCM0 (Display Control Mode 0)</td></tr>
<tr><td>DEN</td><td colspan="11"></td><td>L45E</td><td>L23E</td><td>L1E</td><td>L0E</td><td>CKS</td><td colspan="2"></td><td colspan="5">SC</td><td>EEQ</td><td colspan="3"></td><td>SF</td><td>ESY</td><td colspan="2">SYNC</td></tr>
<tr><td rowspan="2">100</td><td colspan="32">DCM1 (Display Control Mode 1)</td></tr>
<tr><td>DEN</td><td colspan="9"></td><td>L5E</td><td>L4E</td><td>L3E</td><td>L2E</td><td>L1E</td><td>L0E</td><td>CKS</td><td></td><td colspan="6">SC</td><td>EEQ</td><td colspan="3"></td><td>SF</td><td>ESY</td><td colspan="2">SYNC</td></tr>
<tr><td rowspan="2">104</td><td colspan="32">DCM2 (Display Control Mode 2)</td></tr>
<tr><td colspan="30"></td><td>RUF</td><td>RUM0</td></tr>
<tr><td rowspan="2">108</td><td colspan="32">DCM3 (Display Control Mode 3)</td></tr>
<tr><td colspan="21"></td><td>POM</td><td>DCKed</td><td>DCKinv</td><td colspan="2"></td><td colspan="6">DCKD</td></tr>
<tr><td>004</td><td colspan="4"></td><td colspan="12">HTP (H Total Pixels)</td><td colspan="16">Reserved</td></tr>
<tr><td>008</td><td colspan="4"></td><td colspan="12">HDB (H Display Boundary)</td><td colspan="4"></td><td colspan="12">HDP (H Display Period)</td></tr>
<tr><td>00C</td><td colspan="2"></td><td colspan="6">VSW</td><td colspan="8">HSW</td><td colspan="4"></td><td colspan="12">HSP (H Sync pulse Position)</td></tr>
<tr><td>010</td><td colspan="4"></td><td colspan="12">VTR (V Total Rasters)</td><td colspan="16">Reserved</td></tr>
<tr><td>014</td><td colspan="4"></td><td colspan="12">VDP (V Display Period)</td><td colspan="4"></td><td colspan="12">VSP (V Sync pulse Position)</td></tr>
<tr><td>018</td><td colspan="4"></td><td colspan="12">WY (Window Y)</td><td colspan="4"></td><td colspan="12">WX (Window X)</td></tr>
<tr><td>01C</td><td colspan="4"></td><td colspan="12">WH (Window Height)</td><td colspan="4"></td><td colspan="12">WW (Window Width)</td></tr>
</table>

Offset	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
020	L0M (L0 Mode)																															
	L0C								L0W (L0 memory Width)												L0H (L0 Height)											
024							L0OA0 (L0 Origin Address 0)																									
028							L0DA0 (L0 Display Address 0)																									
02C					L0DY (L0 Display Y)																L0DX (L0 Display X)											
110	L0EM (L0 Extend Mode)																															
	L0EC								L0PB																							L0WP
114					L0WY (L0 Window Y)																L0WX (L0 Window X)											
118					L0WH (L0 Window Height)																L0WW (L0 Window Width)											
030	L1M (L1 Mode)																															
	L1C	L1YC	L1CS	L1IM					L1W (L1 memory Width)																							
034							L1OA0(L1 Origin Address 0) / CBDA0(Capure Buffer Display Address 0)																									
038							CBDA1 (Capture Buffer Display Address 1)																									
120	L1EM (L1 Extend Mode)																															
	L1EC						L1DM		L1PB																							
124					L1WY (L1 Window Y)																L1WX (L1 Window X)											
128					L1WH (L1 Window Height)																L1WW (L1 Window Width)											
040	L2M (L2 Mode)																															
	L2C	L2FLP							L2W(L2 memory Width)												L2H (L2 Height)											
044							L2OA0 (L2 Origin Address 0)																									
048							L2DA0 (L2 Display Address 0)																									
04C							L2OA1 (L2 Origin Address 1)																									
050							L2DA1 (L2 Display Address 1)																									
054					L2DY (L2 Display Y)																L2DX (L2 Display X)											
130	L2EM (L2 Extend Mode)																															
	L2EC								L2PB																						L2OM	L2WP
134					L2WY (L2 Window Y)																L2WX (L2 Window X)											
138					L2WH (L2 Window Height)																L2WW (L2 Window Width)											

Offset	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
058	L3M (L3 Mode)																															
	L3C	L3FLP							L3W (L3 memory Width)												L3H (L3 Height)											
05C							L3OA0 (L3 Origin Address 0)																									
060							L3DA0 (L3 Display Address 0)																									
064							L3OA1 (L3 Origin Address 1)																									
068							L3DA1 (L3 Display Address 1)																									
06C					L3DY (L3 Display Y)																L3DX (L3 Display X)											
140	L3EM (L3 Extend Mode)																															
	L3EC								L3PB																						L3OM	L3WP
144					L3WY (L3 Window Y)																L3WX (L3 Window X)											
148					L3WH (L3 Window Height)																L3WW (L3 Window Width)											
070	L4M (L4 Mode)																															
	L4C	L4FLP							L4W (L4 memory Width)												L4H (L4 Height)											
074							L4OA0 (L4 Origin Address 0)																									
078							L4DA0 (L4 Display Address 0)																									
07C							L4OA1 (L4 Origin Address 1)																									
080							L4DA1 (L4 Display Address 1)																									
084					L4DY (L4 Display Y)																L4DX (L4 Display X)											
150	L4EM (L4 Extend Mode)																															
	L4EC																														L4OM	L4WP
154					L4WY (L4 Window Y)																L4WX (L4 Window X)											
158					L4WH (L4 Window Height)																L4WW (L4 Window Width)											
088	L5M (L5 Mode)																															
	L5C	L5FLP							L5W (L5 memory Width)												L5H (L5 Height)											
08C							L5OA0 (L5 Origin Address 0)																									
090							L5DA0 (L5 Display Address 0)																									
094							L5OA1 (L5 Origin Address 1)																									
098							L5DA1 (L5 Display Address 1)																									
09C					L5DY (L5 Display Y)																L5X (L5 Display X)											
160	L5EM (L5 Extend Mode)																															
	L5EC																														L5OM	L5WP
164					L5WY (L5 Window Y)																L5WX (L5 Window X)											
168					L5WH (L5 Window Height)																L5WW (L5 Window Width)											

Offset	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0A0									CPM								CUTC (Cursor Transparent Control)															
											CEN1	CEN0			CUO1	CUO0								CUZT	CUTC							
0A4								CUOA0 (CUrsor0 Origin Address)																								
0A8					CUY0 (Cursor0 Position Y)																CUX0 (Cursor0 Position X)											
0AC								CUOA1 (CUrsor1 Origin Address)																								
0B0					CUY1 (Cursor1 Position Y)																CUX1 (Cursor1 Position X)											
170	MDC (Multi Display Control)																															
	MDen																SC1en								SC0en							
180	DLS (Display Layer Select)																															
									DLS5				DLS4				DLS3				DLS2				DLS1				DLS0			
184									DBGC (Display Back Ground Color)																							
0B4	L0BLD (L0 Blend)																															
																L0BE	L0BS	L0BI	L0BP						L0BR							
188	L1BLD (L1 Blend)																															
																L1BE	L1BS	L1BI	L1BP						L1BR							
18C	L2BLD (L2 Blend)																															
																L2BE	L2BS	L2BI	L2BP						L2BR							
190	L3BLD (L3 Blend)																															
																L3BE	L3BS	L3BI	L3BP						L3BR							
194	L4BLD (L4 Blend)																															
																L4BE	L4BS	L4BI	L4BP						L4BR							
198	L5BLD (L5 Blend)																															
																L5BE	L5BS	L5BI							L5BR							

Offset	Bits	Field
0BC	15–0	L0TC (L0 Transparent Control)
	15	L0ZT
	14–0	L0TC (L0 Transparent Color)
0C0	31–16	L2TC (L2 Transparent Control)
	15–0	L3TC (L3 Transparent Control)
	31	L2ZT
	30–16	L2TC (L2 Transparent Color)
	15	L3ZT
	14–0	L3TC(L3 Transparent Color)
1A0	31–0	L0ETC (L0 Extend Transparency Control)
	31	L0EZT
	23–0	L0ETC (L0 Extend Transparent Color)
1A4	31–0	L1ETC (L1 Transparent Extend Control)
	31	L1EZT
	23–0	L1ETC (L1 Extend Transparent Color)
1A8	31–0	L2ETC (L2 Transparent Extend Control)
	31	L2EZT
	23–0	L2ETC (L2 Extend Transparent Color)
1AC	31–0	L3ETC (L3 Transparent Extend Control)
	31	L3EZT
	23–0	L3ETC (L3 Extend Transparent Color)
1B0	31–0	L4ETC (L4 Extend Transparent Control)
	31	L4EZT
	23–0	L4ETC (L4 Extend Transparent Color)
1B4	31–0	L5ETC (L5 Extend Transparent Control)
	31	L5EZT
	23–0	L5ETC (L5 Extend Transparent Color)
1E0	31–0	L1YCR0 (L1 YC to Red Coefficient 0)
	26–16	a12
	10–0	a11
1E4	31–0	L1YCR1 (L1 YC to Red Coefficient 1)
	24–16	b1
	10–0	a13
1E8	31–0	L1YCG0 (L1 YC to Green Coefficient 0)
	26–16	a22
	10–0	a21
1EC	31–0	L1YCG1 (L1 YC to Green Coefficient 1)
	24–16	b2
	10–0	a23
1F0	31–0	L1YCB0 (L1 YC to Blue Coefficient 0)
	26–16	a32
	10–0	a31
1F4	31–0	L1YCB1 (L1 YC to Blue Coefficient 1)
	24–16	b3
	10–0	a33

Offset	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
400	L0PAL0																															
	A								R								G								B							
404	L0PAL1																															
:	:																															
7FC	L0PAL255																															
800	L1PAL0																															
	A								R								G								B							
804	L1PAL1																															
:	:																															
BFC	L1PAL255																															
1000	L2PAL0																															
	A								R								G								B							
1004	L2PAL1																															
:	:																															
13FC	L2PAL255																															
1400	L3PAL0																															
	A								R								G								B							
1404	L3PAL1																															
:	:																															
17FC	L3PAL255																															

11.1.6 Video capture register list

Base = CaptureBase

Offset	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000	VCM (Video Capture Mode)																															
	VIE	VIS		VICE			CM					VI																		NRGB	VS	
004	CSC (Capture SCale)																															
	VSCI					VSCF											HSCI					HSCF										
008	VCS (Video Capture Status)																															
																												CE				
010	CBM (Capture Buffer Mode)																															
	OO	SBUF	CRGB	PAU					CBW (stride)									C24	BED	CSW		SSS			SSM			HRV				CBST
014										CBOA (Capture Buffer Origin Address)																						
018										CBLA (Capture Buffer Limit Address)																						
01C					CIVSTR																CIHSTR											
020					CIVEND																CIHEND											
300	CVCNT																															
																					CVCNT											
028	CHP (Capture Horizontal Pixel)																															
																							CHP									
02C	CVP (Capture Vertical Pixel)																															
							CVPP																CVPN									
40	CLPF																															
					CVLPF								CHLPF																			
048	CMSS (Capture Magnify Source Size)																															
					CMSHP																CMSVL											
04C	CMDS (Capture Magnify Display Size)																															
					CMDHP																CMDVL											
080	RGBHC(RGB input HSYNC Cycle)/VIN_HSSIZE																															
																			RGBHC													
084	RGBHEN(RGB input Horizontal Enable Area)																															
							RGBHST														RGBHEN											
088	RGBVEN(RGB input Vertical Enable Area)																															
							RGBVST													RGBVEN												
090	RGBS(RGB input SYNC)																															
																RM															HP	VP
0C0	RGBCMY(RGB Color convert Matrix Y coefficient)																															
	a11											a12											a13									
0C4	RGBCMCb(RGB Color convert Matrix Cb coefficient)																															
	a21											a22											a23									
0C8	RGBCMCr(RGB Color convert Matrix Cr coefficient)																															
	a31											a32											a33									
0CC	RGBCMb(RGB Color convert Matrix b coefficient)																															
		b1											b2											b3								

Offset	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4000	CDCN(Capture Data Count for NTSC)																															
				BDCN																VDCN												
4004	CDCP(Capture Data Count for PAL)																															
				BDCP																VDCP												

11.1.7 Drawing engine register list

The parenthesized value in the Offset field denotes the absolute address used by the ***SetRegister*** command.

Base = DrawBase

Offset	31	30	29	28	27	26	25	24	23–16	15–0
000 (000)	Ys									
	s	s	s	s	Int					Frac
004 (001)	Xs									
	s	s	s	s	Int					Frac
008 (002)	dXdy									
	s	s	s	s	Int					Frac
00C (003)	XUs									
	s	s	s	s	Int					Frac
010 (004)	dXUdy									
	s	s	s	s	Int					Frac
014 (005)	XLs									
	s	s	s	s	Int					Frac
018 (006)	dXLdy									
	s	s	s	s	Int					Frac
01C (007)	USN									
	0	0	0	0	Int					0
020 (008)	LSN									
	0	0	0	0	Int					0
040 (010)	Rs									
	0	0	0	0	0	0	0	0	Int	Frac
044 (011)	dRdx									
	s	s	s	s	s	s	s	s	Int	Frac
048 (012)	dRdy									
	s	s	s	s	s	s	s	s	Int	Frac
04C (013)	Gs									
	0	0	0	0	0	0	0	0	Int	Frac
050 (014)	dGdx									
	s	s	s	s	s	s	s	s	Int	Frac
054 (015)	dGdy									
	s	s	s	s	s	s	s	s	Int	Frac
058 (016)	Bs									
	0	0	0	0	0	0	0	0	Int	Frac
05C (017)	dBdx									
	s	s	s	s	s	s	s	s	Int	Frac
060 (018)	dBdy									
	s	s	s	s	s	s	s	s	Int	Frac

<table>
<tr><th>Offset</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td rowspan="2">080
(020)</td><td colspan="32">Zs</td></tr>
<tr><td>0</td><td colspan="16">Int</td><td colspan="15">Frac</td></tr>
<tr><td rowspan="2">084
(021)</td><td colspan="32">dZdx</td></tr>
<tr><td>s</td><td colspan="16">Int</td><td colspan="15">Frac</td></tr>
<tr><td rowspan="2">088
(022)</td><td colspan="32">dZdy</td></tr>
<tr><td>s</td><td colspan="16">Int</td><td colspan="15">Frac</td></tr>
<tr><td rowspan="2">0C0
(030)</td><td colspan="32">Ss</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td colspan="13">Int</td><td colspan="16">Frac</td></tr>
<tr><td rowspan="2">0C4
(031)</td><td colspan="32">dSdx</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td colspan="13">Int</td><td colspan="16">Frac</td></tr>
<tr><td rowspan="2">0C8
(032)</td><td colspan="32">dSdy</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td colspan="13">Int</td><td colspan="16">Frac</td></tr>
<tr><td rowspan="2">0CC
(033)</td><td colspan="32">Ts</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td colspan="13">Int</td><td colspan="16">Frac</td></tr>
<tr><td rowspan="2">0D0
(034)</td><td colspan="32">dTdx</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td colspan="13">Int</td><td colspan="16">Frac</td></tr>
<tr><td rowspan="2">0D4
(035)</td><td colspan="32">dTdy</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td colspan="13">Int</td><td colspan="16">Frac</td></tr>
<tr><td rowspan="2">0D8
(036)</td><td colspan="32">Qs</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>INT</td><td colspan="24">Frac</td></tr>
<tr><td rowspan="2">0DC
(037)</td><td colspan="32">dQdx</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>INT</td><td colspan="24">Frac</td></tr>
<tr><td rowspan="2">0E0
(038)</td><td colspan="32">dQdy</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>INT</td><td colspan="24">Frac</td></tr>
<tr><td rowspan="2">140
(050)</td><td colspan="32">LPN</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td rowspan="2">144
(051)</td><td colspan="32">LXs</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td>s</td><td colspan="12">Int</td><td colspan="16">Frac</td></tr>
<tr><td rowspan="2">148
(052)</td><td colspan="32">LXde</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>Int</td><td colspan="16">Frac</td></tr>
<tr><td rowspan="2">14C
(053)</td><td colspan="32">LYs</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td>s</td><td colspan="12">Int</td><td colspan="16">Frac</td></tr>
<tr><td rowspan="2">150
(054)</td><td colspan="32">LYde</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>s</td><td>Int</td><td colspan="16">Frac</td></tr>
<tr><td rowspan="2">154
(055)</td><td colspan="32">LZs</td></tr>
<tr><td>s</td><td colspan="16">Int</td><td colspan="15">Frac</td></tr>
<tr><td rowspan="2">158
(056)</td><td colspan="32">LZde</td></tr>
<tr><td>s</td><td colspan="16">Int</td><td colspan="15">Frac</td></tr>
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<table>
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<tr><td rowspan="2">180
(060)</td><td colspan="32">PXdc</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td>s</td><td colspan="12">Int</td><td colspan="16">Frac</td></tr>
<tr><td rowspan="2">184
(061)</td><td colspan="32">PYdc</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td>s</td><td colspan="12">Int</td><td colspan="16">Frac</td></tr>
<tr><td rowspan="2">188
(062)</td><td colspan="32">PZdc</td></tr>
<tr><td>s</td><td colspan="16">Int</td><td colspan="15">Frac</td></tr>
<tr><td rowspan="2">200
(080)</td><td colspan="32">RXs</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td>s</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td rowspan="2">204
(081)</td><td colspan="32">RYs</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td>s</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td rowspan="2">208
(082)</td><td colspan="32">RsizeX</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td>s</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td rowspan="2">20C
(083)</td><td colspan="32">RsizeY</td></tr>
<tr><td>s</td><td>s</td><td>s</td><td>s</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td rowspan="2">240
(090)</td><td colspan="32">SADDR</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="25">Address</td></tr>
<tr><td rowspan="2">244
(091)</td><td colspan="32">SStride</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td rowspan="2">248
(092)</td><td colspan="32">SRXs</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td rowspan="2">24C
(093)</td><td colspan="32">SRYs</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td rowspan="2">250
(094)</td><td colspan="32">DADDR</td></tr>
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400	CTR																															
(100)								FO		CE		FCNT						NF	FF	FE			SS				DS				PS	
404	IFSR																															
(–)																														NF	FF	FE
408	IFCNT																															
(–)																											FCNT					
40C	SST																															
(–)																															SS	
410	DST																															
(–)																															DST	
414	PST																															
(–)																															PS	
418	EST																															
(–)																														FO		CE
420	MDR0																															
(108)												ZP				CF							CY	CX					BSV		BSH	
424	MDR1/MDR1S/MDR1B/MDR1TL																															
(109)				LW								BP	BL							LOG				BM		ZW	ZCL			ZC		
428	MDR2/MDR2S/MDR2TL																															
(10a)			TT																	LOG				BM		ZW	ZCL			ZC		SM
42C	MDR3																															
(10b)											TAB				TBL						TWS		TWT				TF		TC			
430	MDR4																															
(10c)																				LOG				BM							TE	

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(122)</td><td colspan="32">ALF</td></tr>
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<tr><td rowspan="2">4A0
(128)</td><td colspan="32">DFIFO</td></tr>
<tr><td colspan="32">DFIFO</td></tr>
</table>

12 Explanation of GDC Registers

Terms appeared in this chapter are explained below:

6. Register address
   Indicates address of register
7. Bit number
   Indicates bit number
8. Bit field name
   Indicates name of each bit field included in register
9. R/W
   Indicates access attribute (read/write) of each field
   Each symbol shown in this section denotes the following:

R0	"0" always read at read. Write access is Don't care.
W0	Only "0" can be written.
R	Read enabled
W	Write enabled
RX	Read enabled (read values undefined)
RW	Read and write enabled
RW0	Read and write 0 enabled

10. Initial value
    Indicates initial value of immediately before the reset of each bit field.
6. Handling of reserved bits
   "0" is recommended for the write value so that compatibility can be maintained with future products.

12.1 Host interface registers

DTC (DMA Transfer Count)

Register address	HostBaseAddress + 00_H	
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24	23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	Reserved	DTC
R/W	R0	RW
Initial value	0	Don't care

DTC is a readable/writable 32-bit register which sets the transfer count in either one long-word (32 bits) or 32 bytes units. When "1h" is set transfer is performed once. However, when "0h" is set, it indicates the maximum transfer count and 16M (16,777,216) data are transferred. During DMA transfer, the remaining transfer count is shown, therefore, the register value cannot be overwritten until DMA transfer is completed.

Note: This register need not be set in a mode in which Dual DMA ACK is not used, or the V832 mode.

DSU (DMA Set Up)

Register address	HostBaseAddress + 04_H							
Bit number	7	6	5	4	3	2	1	0
Bit field name	Reserved					DAM	DBM	DW
R/W	R0					RW	RW	RW
Initial value	0					0	0	0

Bit 0 DW (DMA Word)

Specifies DMA transfer count

0: 1-double word (32 bits) per DMA transfer

1: 8-double words (32 bytes) per DMA transfer (only SH4)

Bit 1 DBM (DMA Bus request Mode)

Selects DREQ mode used in DMA transfer in dual-address mode

0: DREQ is not negated during DMA transfer irrespective of cycle steal or burst mode.

1: DREQ is negated irrespective of cycle steal or burst mode when CORAL cannot receive data (that is, when Ready cannot be returned immediately). When CORAL is ready to receive data, DREQ is reasserted (When DMA transfer is performed in the single-address mode, DREQ is controlled automatically).

Bit 2 DAM (DMA Address Mode)

Selects DMA address mode in issuing external request

0: Dual address mode

1: Single address mode (SH4 only)

Bit 3 DNA (Dual address No Ack mode)

This bit is selected when using the dual-address-mode DMA that does not use the ACK signal.

0: Uses dual-address-mode DMA that uses ordinary ACK signal

1: Uses dual-address-mode DMA that does not use ACK signal
Detection of the DREQ edge is supported; DREQ is negated per transfer. When data cannot be received irrespective of the Bit1 setting, DREQ continues being negated.

DRM (DMA Request Mask)

Register address	HostBaseAddress + 05H							
Bit number	7	6	5	4	3	2	1	0
Bit field name	Reserved							DRM
R/W	R0							RW
Initial value	0							0

This register enables the DMA request. Setting “1” to this register to temporarily stop the DMA request from the CORAL. The external request is enabled by setting “0” to this register.

DST (DMA STatus)

Register address	HostBaseAddress + 06H							
Bit number	7	6	5	4	3	2	1	0
Bit field name	Reserved							DST
R/W	R0							R
Initial value	0							0

This register indicates the DMA transfer status. DST is set to “1” during DMA transfer. This state is cleared to “0” when the DMA transfer is completed.

DTS (DMA Transfer Stop)

Register address	HostBaseAddress + 08H							
Bit number	7	6	5	4	3	2	1	0
Bit field name	Reserved							DTS
R/W	R0							RW
Initial value	0							0

This register suspends DMA transfer.

An ongoing DMA transfer is suspended by setting DTS to “1”.

In the dual-address without ACK mode, to end the DMA transfer, write “1” to this register after CPU DMA transfer.

LTS (display Transfer Stop)

Register address	HostBaseAddress + 09H							
Bit number	7	6	5	4	3	2	1	0
Bit field name	Reserved							LTS
R/W	R0							RW
Initial value	0							0

This register suspends DisplayList transfer.

Ongoing DisplayList transfer is suspended by setting LTS to “1”.

LSTA (displayList transfer STAtus)

Register address	HostBaseAddress + 10H							
Bit number	7	6	5	4	3	2	1	0
Bit field name	Reserved							LSTA
R/W	R0							R
Initial value	0							0

This register indicates the DisplayList transfer status from Graphics Memory. LSTA is set to “1” while DisplayList transfer is in progress. This status is cleared to 0 when DisplayList transfer is completed

DRQ (DMA ReQquest)

Register address	HostBaseAddress + 18H							
Bit number	7	6	5	4	3	2	1	0
Bit field name	Reserved							DRQ
R/W	R0							RW1
Initial value	0							0

This register starts sending external DMA request.

DMA transfer using the external request handshake is triggered by setting DRQ to "1". The external DREQ signal cannot be issued when DMA is masked by the DRM register. This register cannot be written "0". When DMA transfer is completed, this status is cleared to "0".

IST (Interrupt STatus)

Register address	HostBaseAddress + 20H				
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24 : 23 : 22 : 21 : 20 : 19 : 18	17 ¦ 16	15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5	4 ¦ 3 ¦ 2	1 ¦ 0
Bit field name	Reserved	Resv	Reserved	IST	IST
R/W	R0	R0W0	R0	RW0	RW0
Initial value	0	0	0	0	0

This register indicates the current interrupt status. It shows that an interrupt request is issued when "1" is set to this register. The interrupt status is cleared by writing "0" to this register.

Bit 0 CERR (Command Error Flag)
Indicates drawing command execution error interrupt

Bit 1 CEND (Command END)
Indicates drawing command end interrupt

Bit 2 VSYNC (Vertical Sync.)
Indicates vertical interrupt synchronization

Bit 3 FSYNC (Frame Sync.)
Indicates frame synchronization interrupt

Bit 4 SYNCERR (Sync. Error)
Indicates external synchronization error interrupt

Bit 5 REGUD (Register update)
Indicates register update interrupt

Bit 17 and 16 Reserved
This field is provided for testing.
Normally, the read value is "0", but note that it may be "1" when a drawing command error (Bit 0) has occurred.

IMASK (Interrupt MASK)

Register address	HostBaseAddress + 24H				
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24 : 23 : 22 : 21 : 20 : 19 : 18	17 ¦ 16	15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5	4 ¦ 3 ¦ 2	1 ¦ 0
Bit field name	Reserved	Resv	Reserved	IMASK	IMASK
R/W	R0	R0W0	R0	RW	RW
Initial value	0	0	0	0	0

This register masks interrupt requests. Even when the interrupt request is issued for the bit to which "0" is written, interrupt signal is not asserted for CPU.

Bit 0 CERRM (Command Error Interrupt Mask)

Masks drawing command execution error interrupt

Bit 1 CENDM (Command Interrupt Mask)

Masks drawing command end interrupt

Bit 2 VSYNCM (Vertical Sync. Interrupt Mask)

Masks vertical synchronization interrupt

Bit 3 FSYNCH (Frame Sync. Interrupt Mask)

Masks frame synchronization interrupt

Bit 4 SYNCERRM (Sync Error Mask)

Masks external synchronization error interrupt

Bit 5 REGUD (Register update)

Masks register update interrupt

SRST (Software ReSeT)

Register address	HostBaseAddress + 2CH							
Bit number	7	6	5	4	3	2	1	0
Bit field name	Reserved							SRST
R/W	R0							W1
Initial value	0							0

This register controls software reset. When “1” is set to this register, a software reset is performed.

CCF (Change of Clock Frequency)

Register address	HostBaseAddress + 0038H		
Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	COT	Reserved
R/W	RW0	RW	RW0
Initial value	0	00	0

This register changes the operating frequency.

Bit 17 and 16 COT (Clock select for GDC)

Selects the clock for GDC

11 Reserved

10 Reserved

01 133 MHz

00 100 MHz

Notes:

1. Write “0” to the bit field other than the above ([31:18], [15:00]).

LSA (displayList Source Address)

Register address	HostBaseAddress + 40H		
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24	23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2	1 : 0
Bit field name	Reserved	LSA	
R/W	R0	RW	R0
Initial value	0	Don't care	0

This register sets the DisplayList transfer source address. When DisplayList is transferred from Graphics Memory, set the transfer start address of DisplayList stored in Graphics Memory. Since the lower two bits of this register are always treated as "0", DisplayList must be 4-byte aligned. The values set at this register do not change during or after transfer.

LCO (displayList Count)

Register address	HostBaseAddress + 44H	
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24	23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	Reserved	LCO
R/W	R0	RW
Initial value	0	Don't care

This register sets the DisplayList transfer count. Set the display list transfer count by the long word. When "1h" is set, 1-word data is transferred. When "0" is set, it is considered to be the maximum count and 16M (16,777,216) words of data are transferred. The values set at this register do not change during or after transfer.

LREQ (displayList transfer REQuest)

Register address	HostBaseAddress + 48H	
Bit number	7 : 6 : 5 : 4 : 3 : 2 : 1	0
Bit field name	Reserved	LREQ
R/W	R0	RW1
Initial value	0	0

This register triggers DisplayList transfer from the Graphics Memory. Transfer is started by setting LREQ to "1". The DisplayList is transferred from the Graphics Memory to the internal display list FIFO. Access to the display list FIFO by the CPU or DMA is disabled during transfer.

The reserved area in the register area in the host interface excluding the above-mentioned. Please write ALL0 when you write to the Reserved area. A read will produce undefined results.

RSW (Register location Switch)

Register address	HostBaseAddress + 5CH	
Bit number	7 : 6 : 5 : 4 : 3 : 2 : 1	0
Bit field name	Reserved	RSW
R/W	R0	RW
Initial value	0	0

In SH3 or SH4 mode, set this register when moving the register area from the center (1FC0000) to the end of the GDC area (3FC0000). This move can be performed when "1" is written to this register.

Set this register at the first access after reset. Access GDC after about 20 bus clocks after setting the register.

DMA_ST_ADR

Register address	HostBaseAddress + 500$_H$																															
Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name							DMA_ST_ADR																									
R/W							RW																									
Initial value							26'h3FFFFFF																									

DMA start address (*address width, 16-bit CPU:[23:0], 32-bit CPU[25:0])
When DMA_ST_ADR≦[input address]≦DMA_ED_ADR, it is DMA transfer.
When [input address]>DMA_ST_ADR, it is normal access.

DMA_ED_ADR

Register address	HostBaseAddress + 504$_H$																															
Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name							DMA_ED_ADR																									
R/W							RW																									
Initial value							26'h0																									

DMA end address (*address width, 16-bit CPU:[23:0], 32-bit CPU[25:0])
When DMA_ST_ADR≦[input address]≦DMA_ED_ADR, it is DMA transfer.
When [input address]>DMA_ED_ADR, it is normal access.

ERR_ADR

Register address	HostBaseAddress + 508$_H$																															
Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name							ERR_ADR																									
R/W							R																									
Initial value							26'h0																									

This register keeps the address, when the below interrupt request occurs.
It accesses the following order, upper address of 32-bit and lower address of 32-bit in 16-bit CPU mode.
It accesses the randam address in 16-bit CPU mode.

ERR_DETECT

Register address	HostBaseAddress + 50C$_H$																															
Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name																															●	●
R/W																															RW	RW
Initial value																															0	0

Bit0: 16-bit CPU interrupts status register
When “1” is set on the bit0, it shows the following interrupt request.
It accesses the following order, upper address of 32-bit and lower address of 32-bit in 16-bit CPU mode.
It clears the status by writing “0” on the bit0.

Bit1: 16-bit CPU interrupts status register
When “1” is set on the bit0, it shows the following interrupt request.
It accesses the randam address in 16-bit CPU mode. (It accesses the following order, lower address of 32-bit and upper address of 32-bit, but it is not a continuance address.)
It clears the status by writing “0” on the bit1.

INT_MSK

Register address	HostBaseAddress + 510_H																														
Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name																															●	●
R/W																															RW	RW
Initial value																															0	0

Bit0: 16-bit CPU interrupts request mask register (It accesses the following order, upper address of 32-bit and lower address of 32-bit in 16-bit CPU mode.)
It masks 16-bit CPU interrupts.
When “0” is set on the bit0, it does not assert interrupts signal even if the interrupts request occurs.

Bit1: 16-bit CPU interrupts request mask register (It accesses a randam address in 16-bit CPU mode.)
It masks 16-bit CPU interrupts.
When “0” is set on the bit1, it does not assert interrupts signal even if the interrupts request occurs.

INT_MSK

Register address	HostBaseAddress + 514_H																														
Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name																																●
R/W																																RW
Initial value																																0

XINT polarity change signal
“0” is Low Active, “1” is High Active.

12.1.1 GPIO control registers

GPIO control 1 (GPIOC1)

Register address	PIOBaseAddress+40h	
Bit number	31 - 30 - 29 - 28 - 27 - 26 - 25 - 24 - 23 - 22 - 21 - 20 - 19 - 18 - 17 - 16	15 - 14 - 13 - 12 - 11 - 10 - 9 - 8 - 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
Bit field name	GPIO_is_out	GPIO_inout
R/W	R0W	R/W
Initial value	0000_0000	XXXX_XXXX (*1)

The register controls the GPIO pins. Each bit can be set correspondingly from MSB to LSB by couple 1 in each bit.

(*1) The value of the GPIO pin is reflected longer than the fixed time.

(*2) Changes to the GPIO pin are not immediately reflected in the register. It takes time more than constancy (system clock cycle order) to mutual reflection with the GPIO pin.

Bit15-0 GPIO_inout (GPIO input/output data) (*2)

The data of the GPIO pin is read and written.

At read: The value of external pin GPIO15-0 can be read about the bit to which ‘0’ is set with GPIO_is_out.
However, the bit reversing value of external pin GPIO15-0 is read about the bit that GPIOC2.GPIO_xor is set to ‘1’.
When GPIOC2.GPIO_force is set to ‘1’, the value in which the write is compulsorily done to GPIO_inout is read as it is (*3).
The value in which the write is done to GPIO_inout is read as it is (*3) about the bit to which ‘1’ is set with GPIO_is_out. (*3 The influence of GPIO_xor is not undertaken.)
inout (at read) = (is_out || force) ? inout (at write) : (xor ^ GPIO pin)

At write: The written value is disregarded about the bit to which ‘0’ is set with GPIO_is_out.
The write value is output to external pin GPIO15-0 about the bit to which ‘1’ is set with GPIO_is_out.
However, the bit reversing value is output about the bit that GPIOC2.GPIO_xor is set to ‘1’.
GPIO pin = (is_out) ? (xor ^ inout (at write)) : Hi-Z

Bit31-16 GPIO_is_out (GPIO direction)

The direction of each bit of the terminal GPIO I/O is specified.

At read : 0 is always read.

At write : The corresponding bit of ‘1’ is an output of this.

GPIO control 2 (GPIOC2)

Register address	PIOBaseAddress +44h	
Bit number	31 - 30 - 29 - 28 - 27 - 26 - 25 - 24 - 23 - 22 - 21 - 20 - 19 - 18 - 17 - 16	15 - 14 - 13 - 12 - 11 - 10 - 9 - 8 - 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
Bit field name	GPIO_force	GPIO_xor
R/W	R/W	R/W
Initial value	0000_0000	0000_0000

The register controls the GPIO pin. Each set bit can be set corresponding from MSB to LSB by couple 1 in each bit. Refer to the paragraph of GPIOC1 for details.

Bit15-0 GPIO_xor (GPIO_inout read/write data invert)
Bit of GPIO_inout='0'
'0' : An untouched value of external pin GPIO15-0 is read from GPIO_inout.
'1' : A reversed value of external pin GPIO15-0 is read from GPIO_inout.

Bit of GPIO_inout='1'
'0' : The value in which the write is done to GPIO_inout is reflected in external pin GPIO15-0 as it is.
'1' : The reversing value in which the write is done to GPIO_inout is reflected in external pin GPIO15-0 as it is.

Bit31-16 GPIO_force (GPIO_inout force enable for input port read)
It is set whether to force the read value of GPIO_inout set to the input.
'0' : not force
'1' : The read value of a bit of GPIO_inout concerned is forced to the value in which the write is done to GPIO_inout.

12.1.2 Peripheral Interrupt related registers

Peripheral Interrupt control1 (PIC1)

Register address	PIOBaseAddress +4Ch					
Bit number	31 - 30 - 29 - 28 - 27 - 26 - 25 - 24 - 23 - 22 - 21 - 20	19	18	17	16	15 - 14 - 13 - 12 - 11 - 10 - 9 - 8 - 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
Bit field name	Reserve	OFE	WTO	RTO	S1	GPIO_INT_enable
R/W	R0W0	R/W	R/W	R/W	R/W	R/W
Initial value	0000_0000	0	0	0	0	0000_0000

The register controls the interrupt which relates to peripheral logic.

The one of GPIO reacts without regard to input and output in the situation of the setting.

Each set bit can be set corresponding from MSB to LSB by couple 1 in each bit.

Bit15-0 GPIO_INT_enable (GPIO interrupt enable)
It is set whether the generation of interrupt of each bit by the value in which external pin GPIO15-0 is sampled with the internal clock.
Interrupt is not generated for ‘0’.
Interrupt is generated for ‘1’ based on the following register setting.

Bit16 S1 (Serial1 Interrupt Enable)
Interrupt when data is abandoned is set because of word not read by input FIFO of serial 1CH.
0:Interrupt is not generated.
1:Interrupt is generated.

Bit17 RTO (Internal bus timeout interrupt Enable for read)
It is specified whether interrupt is generated when input FIFO Read Wait time of an internal bus becomes more than a set cycle. (This bit does not work if it is not TE bit = 1 of SPC2 registers.)
0:Interrupt is not generated.
1:Interrupt is generated.

Bit18 WTO (Internal bus timeout interrupt Enable for write)
It is specified whether interrupt is generated when input FIFO Read Wait time of an internal bus becomes more than a set cycle. (This bit does not work if it is not TE bit = 1 of SPC2 registers.)
0:Interrupt is not generated.
1:Interrupt is generated.

Bit19 OFE (Output FIFO empty interrupt Enable)
It is specified whether interrupt is generated when output FIFO becomes empty.
0:Interrupt is not generated.
1:Interrupt is generated.

Peripheral Interrupt control2 (PIC2)

Register address	PIOBaseAddress +50h	
Bit number	31 - 30 - 29 - 28 - 27 - 26 - 25 - 24 - 23 - 22 - 21 - 20 - 19 - 18 - 17 - 16	15 - 14 - 13 - 12 - 11 - 10 - 9 - 8 - 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
Bit field name	Reserve	GPIO_INT_polarity
R/W	R0W0	R/W
Initial value	0000_0000	0000_0000

The register controls interrupt concerning GPIO.

It reacts without regard to input and output in the situation of the setting.

Each set bit can be set corresponding from MSB to LSB by couple 1 in each bit.

Bit15-0 GPIO_INT_polarity (GPIO interrupt polarity)
Interrupt is generated for the following values.
0: When you detect Level '0' or negative edge (Depend on GPIO_INT_mode)
1: When you detect Level '1' or positive edge (Depend on GPIO_INT_mode)

Peripheral Interrupt control3 (PIC3)

Register address	PIOBaseAddress +54h	
Bit number	31 - 30 - 29 - 28 - 27 - 26 - 25 - 24 - 23 - 22 - 21 - 20 - 19 - 18 - 17 - 16	15 - 14 - 13 - 12 - 11 - 10 - 9 - 8 - 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
Bit field name	Reserve	GPIO_INT_mode
R/W	R0W0	R/W
Initial value	0000_0000	0000_0000

The register controls interrupt concerning GPIO.

It reacts without regard to input and output in the situation of the setting.

Each set bit can be set corresponding from MSB to LSB by couple 1 in each bit.

Bit15-0 GPIO_INT_mode (GPIO interrupt mode)
0: level sensitive ('0' or '1' depends on GPIO_INT_polarity)
1: edge sensitive ('pos' or 'neg' depends on GPIO_INT_polarity)

Peripheral Interrupt Status (PIST)

Register address	PIOBaseAddress +80h						
Bit number	31 - 30 - 29 - 28 - 27 - 26 - 25 - 24	23 - 22 - 21 - 20	19	18	17	16	15 - 14 - 13 - 12 - 11 - 10 - 9 - 8 - 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
Bit field name	Reserve	Reserve	OFE	WTO	RTO	S1	GPIO_INT_status
R/W	R0W0	R0W0	R/W0	R/W0	R/W0	R/W0	R/W0
Initial value	0000_0000	0000_0000	0	0	0	0	0000_0000

The register shows the state of the interrupt which relates to peripheral logic. It clears by 0 Write.
This state is consolidated and it is reflected in bit17 of host interface register IST.

Bit15-0 GPIO_INT_status (GPIO interrupt status)
Shows that interrupt is generated by the bit of the correspondence of GPIO.
0: interrupt is not generated
1: interrupt is generated

Bit16 S1 (Serial1 port interrupt status)
In Serial1communication, It is shown that interruption which notifies that input data was thrown away occurred.
0: interrupt is not generated
1: interrupt is generated

Bit17 RTO (Internal bus timeout interrupt Status for read)
It is shown that interruption when the input FIFO Read Wait time of an internal bus becomes more than a setting cycle occurred.
0: interrupt is not generated
1: interrupt is generated

Bit18 WTO (Internal bus timeout interrupt Status for write)
It is shown that interruption when the output FIFO Read Wait time of an internal bus becomes more than a setting cycle occurred.
0: interrupt is not generated
1: interrupt is generated

Bit19 OFE (Output FIFO empty interrupt Status)
It is shown that interruption when Output FIFO becomes empty occurred.
0: interrupt is not generated
1: interrupt is generated

Revision

Register address	PIOBaseAddress +84h		
Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Bit field name	YEAR	VERSION	REVISION
R/W	RO		
Initial value	0x2005	0x01	0x00

The register shows the chip version.

12.1.3 I²C Interface Registers

BSR (Bus Status Register)

Register address	I2C Base Address + 000h							
Bit No	7	6	5	4	3	2	1	0
Bit field name	BB	RSC	AL	LRB	TRX	AAS	GCA	FBT
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

All bits on this register are cleared while bit EN on CCR register is "0".

Bit7 BB (Bus Busy)
Indicate state of I2C-bus
0: STOP condition was detected.
1: START condition (The bus is in use.) was detected.

Bit6 RSC (Repeated START Condition)
Indicate repeated START condition
This bit is cleared by writing "0" to INT bit, the case of not addressed in a slave mode, the detection of START condition under bus stop, and the detection of STOP condition.
0: Repeated START condition was not detected.
1: START condition was detected again while the bus was in use.

Bit5 AL(Arbitration Lost)
Detect Arbitration lost
This bit is cleared by writing "0" to INT bit.
0: Arbitration lost was not detected.
1: Arbitration occurred during master transmission, or "1" writing was performed to MSS bit while other systems were using the bus.

Bit4 LRB (Last Received Bit)
Store Acknowledge
This bit is cleared by detection of START condition or STOP condition.

Bit3 TRX (Transmit / Receive)
Indicate data receipt and data transmission.
0: receipt
1: transmission

Bit2 AAS (Address As Slave)
Detect addressing
This bit is cleared by detection of START condition or STOP condition.
0: Addressing was not performed in a slave mode.
1: Addressing was performed in a slave mode.

Bit1 GCA (General Call Address)
Detect general call address (00h)
This bit is cleared by detection of START condition or STOP condition.
0: General call address was not received in a slave mode.
1: General call address wad received in a slave mode.

Bit0 FBT (First Byte Transfer)
Detect the 1st byte
Even if this bit is set to "1" by detection of START condition, it is cleared by writing "0" on INT bit or by not being addressed in a slave mode.
0: Received data is not the 1st byte.
1: Received data is the 1st byte (address data).

BCR (Bus Control Register)

Register address	I2C Base Address + 0004h							
Bit No	7	6	5	4	3	2	1	0
Bit field name	BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT
R/W	R/W0	R/W	R0/W1	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit7 BER (Bus Error)
Flag bit for request of bus error interruption
When this bit is set, EN bit on CCR register will be cleared, this module will be in a stop state and data transfer will be discontinued.
write case
0: A request of buss error interruption is cleared.
1: Don't care.
read case
0: A bus error was not detected.
1: Undefined START condition or STOP condition was detected while data transfer.

Bit6 BEIE (Bus Error Interruption Enable)
Permit bus error interruption
When both this bit and BER bit are "1", the interruption is generated.
0: Prohibition of bus error interruption
1: Permission of bus error interruption

Bit5 SCC (Start Condition Continue)
Generate START condition
write case
0: Don't care.
1: START condition is generated again at the time of master transmission.

Bit4 MSS (Master Slave Select)
Select master / slave mode
When arbitration lost is generated in master transmission, this bit is cleared and this module becomes a slave mode.
0: This module becomes a slave mode after generating STOP condition and completing transfer.
1: This module becomes a master mode, generates START condition and starts transfer.

Bit3 ACK (ACKnowledge)
Permit generation of acknowledge at the time of data reception
This bit becomes invalid at the time of address data reception in a slave mode.
0: Acknowledge is not generated.
1: Acknowledge is generated.

Bit2 GCAA(General Call Address Acknowledge)
Permit generation of acknowledge at the time of general call address reception
0: Acknowledge is not generated.
1: Acknowledge is generated.

Bit1 INTE (INTerrupt Enable)
Permit interruption
When this bit is "1" interruption is generated if INT bit is "1".
0: Prohibition of interrupt
1: Permission of interrupt

Bit0 INT (INTerrupt)
Flag bit for request of interruption for transfer end
When this bit is "1" SCL line is maintained at "L" level. If this bit is cleared by being written "0", SCL line is released and the following byte transfer is started. Moreover, it is reset to "0" by generating of START condition or STOP condition at the time of a master.
write case

0: The flag is cleared.
1: Don't care.
read case
0: The transfer is not ended.
1: It is set when 1 byte transfer including the acknowledge bit is completed and it corresponds to the following conditions.
- It is a bus master.
- It is an addressed slave.
- It was going to generate START condition while other systems by which arbitration lost happened used the bus.

Competition of SCC, MSS and INT bit

Competition of the following byte transfer, generation of START condition and generation of STOP condition happens by the simultaneous writing of SCC, MSS and INT bit. The priority at this case is as follows.

1) The following byte transfer and generation of STOP condition
If "0" is written to INT bit and "0" is written to MSS bit, priority will be given to "0" writing to MSS bit and STOP condition will be generated.
2) The following byte transfer and generation of START condition
If "0" is written to INT bit and "1" is written to SCC bit, priority will be given to "1" writing to SCC bit and START condition will be generated.
3) Generation of START condition and STOP condition
The simultaneous writing of "1" to SCC bit and "0" to MSS bit is prohibition.

CCR (Clock Control Register)

Register address	I2C Base Address + 0008h							
Bit No	7	6	5	4	3	2	1	0
Bit field name	-	HSM	EN	CS4	CS3	CS2	CS1	CS0
R/W	R1	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	-	-	-	-	-

Bit7 Nonuse
"1" is always read at read.

Bit6 HSM (High Speed Mode)
Select standard-mode / high-speed-mode
0: Standard-mode
1: High-speed-mode

Bit5 EN (Enable)
Permission of operation
When this bit is "0", each bit of BSR and BCR register (except BER and BEIE bit) is cleared. This bit is cleared when BER bit is set.
0: Prohibition of operation
1: Permission of operation

Bit4 CS4 - 0 (Clock Period Select4 - 0)

Set up the frequency of a serial transfer clock
Frequency fscl of a serial transfer clock is shown as the following formula.
Please set up fscl not to exceed the value shown below at the time of master operation.
standard-mode: 100KHz
high-speed-mode: 400KHz

standard-mode

$$fscl = \frac{A}{(2 \times m)+2}$$

high-speed-mode

$$fscl = \frac{A}{int(1.5 \times m)+2}$$

A: I2C system clock = 16.6MHz

<Notes>
+2 cycles are minimum overhead to confirm that the output level of SCL terminal changed. When the delay of the positive edge of SCL terminal is large or when the clock is extended by the slave device, it becomes larger than this value.

The value of m becomes like the following page to the value of CS 4-0.

CS4	CS3	CS2	CS1	CS0	m	
					standard	high-speed
0	0	0	0	0	65	inhibited
0	0	0	0	1	66	inhibited
0	0	0	1	0	67	inhibited
0	0	0	1	1	68	inhibited
0	0	1	0	0	69	inhibited
0	0	1	0	1	70	inhibited
0	0	1	1	0	71	inhibited
0	0	1	1	1	72	inhibited
0	1	0	0	0	73	9
0	1	0	0	1	74	10
0	1	0	1	0	75	11
0	1	0	1	1	76	12
0	1	1	0	0	77	13
0	1	1	0	1	78	14
0	1	1	1	0	79	15
0	1	1	1	1	80	16
1	0	0	0	0	81	17
1	0	0	0	1	82	18
1	0	0	1	0	83	19
1	0	0	1	1	84	20
1	0	1	0	0	85	21
1	0	1	0	1	86	22
1	0	1	1	0	87	23
1	0	1	1	1	88	24
1	1	0	0	0	89	25
1	1	0	0	1	90	26
1	1	0	1	0	91	27
1	1	0	1	1	92	28
1	1	1	0	0	93	29
1	1	1	0	1	94	30
1	1	1	1	0	95	31
1	1	1	1	1	96	32

Address Register(ADR)

Register address	I2C Base Address + 000Ch							
Bit No	7	6	5	4	3	2	1	0
Bit field name	-	A6	A5	A4	A3	A2	A1	A0
R/W	R1	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	-	-	-	-	-	-	-

Bit7 Nonuse
"1" is always read at read.

Bit6 - 0 A6 - 0 (Address6 - 0)
Store slave address
In a slave mode it is compared with DAR register after address data reception, and when in agreement, acknowledge is transmitted to a master.

Data Register(DAR)

Register address	I2C Base Address + 0010h							
Bit No	7	6	5	4	3	2	1	0
Bit field name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-

Bit7 - 0 D7 - 0 (Data7 - 0)
Store serial data
This is a data register for serial data transfer. The data is transferred from MSB. At the time of data reception (TRX=0) the data output is set to "1".
The writing side of this register is a double buffer. When the bus is in use (BB=1), the write data is loaded to the register for serial transfer for every transfer. At the time of read-out, the receiving data is effective only when INT bit is set because the register for serial transfer is read directly at this time.

12.2 Graphics memory interface registers

MMR (Memory I/F Mode Register)

Register address	HostBaseAddress + $FFFC_H$													
Bit number	31	30	29:28:27	26	25	24:23	22:21:20:19	18:17	16:15:14	13:12	11:10	9:8:7	6:5:4	3	2:1:0
Bit field name	*1	tWR	Reserved	*1	*1	TRRD	TRC	TRP	TRAS	TRCD	LOWD	RTS	SAW	ASW	CL
R/W	RW	RW	R	R1 W0	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Initial value	0	0	Don't care	1	0	00	0000	00	000	00	00	000	000	0	000

*1: Reserved

This register sets the mode of the graphics memory interface. A value must be written to this register after a reset. (When default setting is performed, a value must also be written to this register.) Only write once to this register; do not change the written value during operation.

This register is not initialized at a software reset.

Bit 2 to 0 CL (CAS Latency)

Sets the CAS latency. Write the same value as this field, to the mode register for SDRAM

011	CL3
010	CL2
Other than the above	Setting disabled

Bit 3 ASW (Attached SDRAM bit Width)

Sets the bit width of the data bus (memory bus width mode)

1	Reserved
0	32 bit

Bit 6 to 4 SAW (SDRAM Address Width)

Sets the bit width of the SDRAM address

001	15 bit BANK 2 bit ROW 13 bit COL 9 bit SDRAM
111	14 bit BANK 2 bit ROW 12 bit COL 9 bit SDRAM
110	14 bit BANK 2 bit ROW 12 bit COL 8 bit SDRAM
101	13 bit BANK 2 bit ROW 11 bit COL 8 bit SDRAM
100	12 bit BANK 1 bit ROW 11 bit COL 8 bit FCRAM
Other than the above	Setting disabled

Bit 9 to 7 RTS (Refresh Timing Setting)

Sets the refresh interval

000	Refresh is performed every 384 internal clocks.
111	Refresh is performed every 1552 internal clocks.
001 to 110	Refresh is performed every '64 $\times$ n' internal clocks in the 64 to 384 range.

Bit 11 and 10 LOWD

Sets the count of clocks secured for the period from the instant the ending data is output to the instant the write command is issued.

It is able to adjust the internal timing of memory interface by the setting.

11	3 clocks
10	2 clocks
01	1 clocks
Other than the above	Setting disabled

Bit 13 and 12 TRCD

Sets the wait time secured from the bank active to CAS. The clock count is used to express the wait time.

11	3 clocks
10	2 clocks
01	1 clock
00	0 clock

Bit 16 to 14 TRAS

Sets the minimum time for 1 bank active. The clock count is used to express the minimum time.

111	7 clocks
110	6 clocks
101	5 clocks
100	4 clocks
011	3 clocks
010	2 clocks
Other than the above	Setting disabled

Bit 18 and 17 TRP

Sets the wait time secured from the pre-charge to the bank active. The clock count is used to express the wait time.

11	3 clocks
10	2 clocks
01	1 clock

Bit 22 to 19 TRC

This field sets the wait time secured from the refresh to the bank active. The clock count is used to express the wait time.

1010	10 clocks
1001	9 clocks
1000	8 clocks
0111	7 clocks
0110	6 clocks
0101	5 clocks

	0100	4 clocks
	0011	3 clocks
	Other than the above	Setting disabled

Bit 24 and 23 TRRD

Sets the wait time secured from the bank active to the next bank active. The clock count is used to express the wait time.

11	3 clocks
10	2 clocks

Bit 26 Reserved

Always write "0" at write.

"1" is always read at read.

Bit 30 TWR

Sets the write recovery time (the time from the write command to the read or to the pre-charge command).

1	2 clocks
0	1 clock

12.3 Display control registers

DCM0/1 (Display Control Mode 0/1)

Register address	DisplayBaseAddress + 00_H (DCM0)															
Bit number	31	30–20	19	18	17	16	15	14	13–8	7	6	5	4	3	2	1–0
Bit field name	DEN	Reserve	L45E	L23E	L1E	L0E	CKS	Resv	SC	EEQ		Resv	Resv	SF	ESY	SYNC
R/W	RW	RX	RW	RW	RW	RW	RW	R0	RW	RW		RW	R0	RW	RW	RW
Initial value	0	X	0	0	0	0	0	0	11110	0		0	0	0	0	00

Register address	DisplayBaseAddress + 100_H (DCM1)																	
Bit number	31	30–22	21	20	19	18	17	16	15	14	13–8	7	6	5	4	3	2	1–0
Bit field name	DEN	Reserve	L5E	L4E	L3E	L2E	L1E	L0E	CKS	Resv	SC	EEQ		Resv	Resv	SF	ESY	SYNC
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	R0	RW	RW		RW	R0	RW	RW	RW
Initial value	0	X	0	0	0	0	0	0	0	0	11101	0		0	0	0	0	00

This register controls the display count mode. It is not initialized by a software reset. This register is mapped to two addresses but it is one substance. The differences between the two registers are the format of the frequency division rate setting (SC) and layer enable. The two formats exist to maintain backword compatibility with previous products.

Bit 1 to 0 SYNC (Synchronize)

Set synchronization mode

X0 Non-interlace mode

10 Interlace mode

11 Interlace video mode

Bit 2 ESY (External Synchronize)

Sets external synchronization mode

0: External synchronization disabled

1: External synchronization enabled

Bit 3 SF (Synchronize signal format)

Sets format of synchronization (VSYNC, HSYNC) signals

0: Negative logic

1: Positive logic

Bit 7 EEQ (Enable Equalizing pulse)

Sets CCYNC signal mode

0: Does not insert equalizing pulse into CCYNC signal

1: Inserts equalizing pulse into CCYNC signal

Bit 13 to 8 SC (Scaling)

Divides display reference clock by the preset ratio to generate dot clock

Offset = 0		Offset = 100_H	
x00000	Frequency not divided	000000	Frequency not divided

x00001	Frequency division rate = 1/4	000001	Frequency division rate = 1/2
x00010	Frequency division rate = 1/6	000010	Frequency division rate = 1/3
X00011	Frequency division rate = 1/8	000011	Frequency division rate = 1/4
:		:	
x11111	Frequency division rate = 1/64	111111	Frequency division rate = 1/64

When n is set, with Offset = 0, the frequency division rate is 1/(2n + 2).

When m is set, with Offset = 100h, the frequency division rate is 1/(m + 1).

Basically, these are setting parameters with the same function (2n + 2 = m + 1). Because of this, m = 2n + 1 is established. When n is set to the SC field with Offset = 0, 2n + 1 is reflected with Offset = 100h.

Also, when PLL is selected as the reference clock, frequency division rates 1/1 to 1/5 are non-functional even when set; other frequency division rates are assigned.

Bit 15 CKS (Clock Source)

Selects reference clock

0: Internal PLL output clock

1: DCLKI input

Bit 16 L0E (L0 layer Enable)

Enables display of the L0 layer. The L0 layer corresponds to the C layer for previous products.

0: Does not display L0 layer

1: Displays L0 layer

Bit 17 L1E (L1 layer Enable)

Enables display of the L1 layer. The L1 layer corresponds to the W layer for previous products.

0: Does not display L1 layer

1: Displays L1 layer

Bit 18 L23E (L2 & L3 layer Enable) ------ DCM0

Enables simultaneous display of the L2 and L3 layers. These layers correspond to the M layer for previous products.

0: Does not display L2 and L3 layer

1: Displays L2 and L3 layer

L2E (L2 layer Enable) ------ DCM1

Enables L2 layer display

0: Does not display L2 layer

1: Displays L2 layer

Bit 19 L45E (L4 & L5 layer Enable) ------ DCM0

Enables simultaneous display of the L4 and L5 layers. These layers correspond to the B layer for previous products.

0: Does not display L4 and L5 layer

1: Displays L4 and L5 layer

L3E (L3 layer Enable)) ------ DCM1

Enables L3 layer display

0: Does not display L3 layer

1: Displays L3 layer

Bit 20 L4E (L4 layer Enable)

Enables L4 layer display

0: Does not display L4 layer

1: Displays L4 layer

Bit 21 L5E (L5 layer Enable)

Enables L5 layer display

0: Does not display L5 layer

1: Displays L5 layer

Bit 31 DEN (Display Enable)

Enables display

0: Does not output display signal

1: Outputs display signal

DCM2 (Display Control Mode 2)

Register address	DisplayBaseAddress + 104_H				
Bit number	31 30 29 28 27 28 17 16 15 14 13 12 11 10 9 8 7 6 5	4	3 2	1	0
Bit field name	Reserve	Reserv	Reserv	RUF	RUM
R/W	R0	R0	R0	RW	RW
Initial value	0	0	0	0	0

Bit0 RUM (Register Update Mode)

The mode reflects the register value synchronizing with vertical synchronization is selected.

0: The register update is in real time reflected in the internal control circuit. The display falls into disorder when updating it for the display period.

1: It value of the register spreads to the internal control circuit synchronizing with vertical synchronization. The simultaneity is controlled with the following RUF flags.

Bit1 RUF (Register Update Flag)

The value is directed to be updated in the following vertical synchronization in writing 1 in this flag. If the update ends, it becomes 0.

0: Initial or update end

1: Vertical synchronous waiting

DCM3 (Display Control Mode 3)

Register address	DisplayBaseAddress + 108_H							
Bit number	31 30 29 … 17 16 15 14 13 12	11	10	9	8	7	6	5 4 3 2 1 0
Bit field name	reserve	resv	POM	DCKed	DCKinv	Reserve		DCKD
R/W	R0	R0	RW	RW	RW	RW0	R0	RW
Initial value	0	0	0	0	0	0	0	000000

Bit5-0 DCKD (Display Clock Delay)

This defines additional delay time by internal PLL clock period.

000000 No additional delay

000010 +2 PLL clock

000100 +3 PLL clock

000110 +4 PLL clock

: :

111110 +33 PLL clock

xxxxx1 reserve

Bit8 DCKinv (Display Clock inversion)

0: DCLKO output signal is not inverted

1: DCLKO output signal is inverted.

Bit9 DCKed (Display clock edge)

This defines which edge mode is used.

0: single edge mode in which positive edge is used for digital RGB output.

1: bi-edge mode in which positive edge and negative edge are used for digital RGB output to identify two data streams.

Bit10 POM (Parallel output Mode)

This defines a way to output two data streams for two display

0: multiplex output mode in which two data streams are multiplexed and goes to the digital RGB output.

1: parallel output mode in which one data stream go to the digital RGB output and another data stream goes to the analog RGB output.

HTP (Horizontal Total Pixels)

Register address	DisplayBaseAddress + 06_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				HTP											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the horizontal total pixel count. Setting value + 1 is the total pixel count.

HDP (Horizontal Display Period)

Register address	DisplayBaseAddress + 08_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				HDP											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the total horizontal display period in unit of pixel clocks. Setting value + 1 is the pixel count for the display period.

HDB (Horizontal Display Boundary)

Register address	DisplayBaseAddress + $0A_H$															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				HDB											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the display period of the left part of the window in unit of pixel clocks. Setting value + 1 is the pixel count for the display period of the left part of the window. When the window is not divided into right and left before display, set the same value as HDP.

HSP (Horizontal Synchronize pulse Position)

Register address	DisplayBaseAddress + $0C_H$															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				HSP											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the pulse position of the horizontal synchronization signal in unit of pixel clocks. When the clock count since the start of the display period reaches setting value + 1, the horizontal synchronization signal is asserted.

HSW (Horizontal Synchronize pulse Width)

Register address	DisplayBaseAddress + $0E_H$							
Bit number	7	6	5	4	3	2	1	0
Bit field name	HSW							
R/W	RW							
Initial value	Don't care							

This register controls the pulse width of the horizontal synchronization signal in unit of pixel clocks. Setting value + 1 is the pulse width clock count.

VSW (Vertical Synchronize pulse Width)

Register address	DisplayBaseAddress + $0F_H$							
Bit number	7	6	5	4	3	2	1	0
Bit field name	Reserved		VSW					
R/W	R0		RW					
Initial value	0		Don't care					

This register controls the pulse width of vertical synchronization signal in unit of raster. Setting value + 1 is the pulse width raster count.

VTR (Vertical Total Rasters)

Register address	DisplayBaseAddress + 12_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				VTR											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the vertical total raster count. Setting value + 1 is the total raster count. For the interlace display, Setting value + 1.5 is the total raster count for 1 field; 2 × setting value + 3 is the total raster count for 1 frame (see ***Section 8.3.2***).

VSP (Vertical Synchronize pulse Position)

Register address	DisplayBaseAddress + 14_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				VSP											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the pulse position of vertical synchronization signal in unit of raster. The vertical synchronization pulse is asserted starting at the setting value + 1st raster relative to the display start raster.

VDP (Vertical Display Period)

Register address	DisplayBaseAddress + 16_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				VDP											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the vertical display period in unit of raster. Setting value + 1 is the count of raster to be displayed.

L0M (L0 layer Mode)

Register address	DisplayBaseAddress + 20_H					
Bit number	31	30 29	28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	L0C	Reserved	Reserved	L0W	Reserved	L0H
R/W	RW	R0	R0	RW	R0	RW
Initial value	0	0	0	Don't care	0	Don't care

Bit 11 to 0 L0H (L0 layer Height)

Specifies the height of the logic frame of the L0 layer in pixel units. Setting value + 1 is the height

Bit 23 to 16 L0W (L0 layer memory Width)

Sets the memory width (stride) of the logic frame of the L0 layer in 64-byte units

Bit 31 L0C (L0 layer Color mode)

Sets the color mode for L0 layer

0 Indirect color (8 bits/pixel) mode

1 Direct color (16 bits/pixel) mode

L0EM (L0-layer Extended Mode)

Register address	DisplayBaseAddress + 110_H				
Bit number	31 30	29 28 27 26 25 24	23 22 21 20	19 18 17 16 15 14 13 12 11 10 ----- 4 3 2 1	0
Bit field name	L0EC	Reserved	L0PB	Reserved	L0WP
R/W	RW	R0	RW	R0	RW
Initial value		0		0	0

Bit 0 L0 WP (L0 layer Window Position enable)

Selects the display position of L0 layer

0 Compatibility mode display (C layer supported)

1 Window display

Bit 23 to 20 L0PB (L0 layer Palette Base)

Shows the value added to the index when subtracting palette of L0 layer. 16 times of setting value is added.

Bit 31 and 30 L0EC (L0 layer Extended Color mode)

Sets extended color mode for L0 layer

00 Mode determined by L0C

01 Direct color (24 bits/pixel) mode

1x Reserved

L0OA (L0 layer Origin Address)

Register address	DisplayBaseAddress + 24_H		
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
Bit field name	Reserved	L0OA	
R/W	R0	RW	R0
Initial value	0	Don't care	0000

This register sets the origin address of the logic frame of the L0 layer. Since lower 4 bits are fixed at "0", address 16-byte-aligned.

L0DA (L0-layer Display Address)

Register address	DisplayBaseAddress + 28_H		
Bit number	31 30 29 28	27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved		L0DA
R/W	R0	RW0	RW
Initial value	0		Don't care

This register sets the display origin address of the L0 layer. For the direct color mode (16 bits/pixel), the lower 1 bit is "0", and this address is treated as being aligned in 2 bytes.

L0DX (L0-layer Display position X)

Register address	DisplayBaseAddress + $2C_H$	
Bit number	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	L0DX
R/W	R0	RW
Initial value	0	Don't care

This register sets the display starting position (X coordinates) of the L0 layer on the basis of the origin of the logic frame in pixels.

L0DY (L0-layer Display position Y)

Register address	DisplayBaseAddress + $2E_H$	
Bit number	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	L0DY
R/W	R0	RW
Initial value	0	Don't care

This register sets the display starting position (Y coordinates) of the L0 layer on the basis of the origin of the logic frame in pixels.

L0WX (L0 layer Window position X)

Register address	DisplayBaseAddress + 114_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L0WX											
R/W	R0				RW											
Initial value	0															

This register sets the X coordinates of the display position of the L0 layer window.

L0WY (L0 layer Window position Y)

Register address	DisplayBaseAddress + 116_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L0WY											
R/W	R0				RW											
Initial value	0															

This register sets the Y coordinates of the display position of the L0 layer window.

L0WW (L0 layer Window Width)

Register address	DisplayBaseAddress + 118_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L0WW											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the horizontal direction display size (width) of the L0 layer window. Do not specify “0”.

L0WH (L0 layer Window Height)

Register address	DisplayBaseAddress + $11A_H$															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L0WH											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the vertical direction display size (height) of the L0 layer window. Setting value + 1 is the height.

L1M (L1-layer Mode)

Register address	DisplayBaseAddress + 30_H						
Bit number	31	30	29	28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 – – – 5 4 3 2 1 0
Bit field name	L1C	L1YC	L1CS	L1IM	Reserved	L1W	Reserved
R/W							R0
Initial value							0

Bit 23 to 16 L1W (L1 layer memory Width)

Sets the memory width (stride) of the logic frame of the W layer in unit of 64 bytes

Bit 28 L1IM (L1 layer Interlace Mode)

Sets video capture mode when L1CS in capture mode

0: Normal mode

1: For non-interlace display, displays captured video graphics in WEAVE mode
For interlace and video display, buffers are managed in frame units (pair of odd field and even field).

Bit 29 L1CS (L1 layer Capture Synchronize)

Sets whether the layer is used as normal display layer or as video capture

0: Normal mode

1: Capture mode

Bit 30 L1YC (L1 layer YC mode)

Sets color format of L1 layer
The YC mode must be set for video capture.

0: RGB mode

1: YC mode

Bit 31 L1C (L1 layer Color mode)
Sets color mode for L1 layer

0: Indirect color (8 bits/pixel) mode

1: Direct color (16 bits/pixel) mode

L1EM (L1 layer Extended Mode)

Register address	DisplayBaseAddress + 120_H				
Bit number	31 30	29 28 27 26	25 24	23 22 21 20	19 18 17 16 15 14 13 12 11 10 – – – 4 3 2 1 0
Bit field name	L1EC	Reserved	DM	L1PB	Reserved
R/W	RW	R0		RW	R0
Initial value		0			0

Bit 23 to 20 L1PB (L1 layer Palette Base)

Shows the value added to the index when subtracting palette of L1 layer. 16 times of setting value is added.

Bit 25 to 24 L1DM (L1 layer Display Magnify Mode)

- 00 Normal Mode (no scaling or shrink scaling)
- 01 Reserved
- 10 Magnify Scaling
- 11 Reserved

Bit 31 to 30 L1EC (L1 layer Extended Color mode) Sets extended color mode for L1 layer

- 00 Mode determined by L1C
- 01 Direct color (24 bits/pixel) mode
- 1x Reserved

L1DA (L1 layer Display Address)

Register address	DisplayBaseAddress + 34_H	
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	L1DA
R/W	R0	RW
Initial value	0	Don't care

This register sets the display origin address of the L1 layer. For the direct color mode (16 bits/pixel), the lower 1 bit is “0”, and this register is treated as being aligned in 2 bytes. Wraparound processing is not performed for the L1 layer, so the frame origin linear address and display position (X coordinates, and Y coordinates) are not specified.

CBDA1 (Capture Buffer Display Address 1)

Register address	DisplayBaseAddress + 0x38	
Bit No.	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserve	CBDA1
R/W	R0	R
Initial value	0	Undefined

This register is a read-only register which is only enabled when the L1CS bit is 1 and the L1IM bit is also 1. This register indicates the starting address of an even field of the capture screen.

L1WX (L1 layer Window position X)

Register address	DisplayBaseAddress + 124_H (DisplayBaseAddress + 18_H)															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L1WX											
R/W	R0				RW											
Initial value	0				Don't care											

This register sets the X coordinates of the display position of the L1 layer window. This register is placed in two address spaces. The parenthesized address is the register address to maintain compatibility with previous products. The same applies to L1WY, L1WW, and L1WH.

L1WY (L1 layer Window position Y)

Register address	DisplayBaseAddress + 126_H (DisplayBaseAddress + $1A_H$)															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L1WY											
R/W	R0				RW											
Initial value	0				Don't care											

This register sets the Y coordinates of the display position of the L1 layer window.

L1WW (L1 layer Window Width)

Register address	DisplayBaseAddress + 128_H (DisplayBaseAddress + $1C_H$)															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L1WW											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the horizontal direction display size (width) of the L1 layer window. Do not specify "0".

L1WH (L1 layer Window Height)

Register address	DisplayBaseAddress + $12A_H$ ((DisplayBaseAddress + $1E_H$)															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L1WH											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the vertical direction display size (height) of the L1 layer window. Setting value + 1 is the height.

L2M (L2 layer Mode)

Register address	DisplayBaseAddress + 40_H					
Bit number	31	30 29	28 27 – – 24	23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	L2C	L2FLP	Reserved	L2W	Reserved	L2H
R/W	RW	RW	R0	RW	R0	RW
Initial value			0	Don't care	0	Don't care

Bit 11 to 0 L2H (L2 layer Height)

Specifies the height of the logic frame of the L2 layer in pixel units. Setting value + 1 is the height

Bit 23 to 16 L2W (L2 layer memory Width)

Sets the memory width (stride) of the logic frame of the L2 layer in 64-byte units

Bit 30 and 29 L2FLP (L2 layer Flip mode)

Sets flipping mode for L2 layer

00 Displays frame 0

01 Displays frame 1

10 Switches frame 0 and 1 alternately for display

11 Reserved

Bit 31 L2C (L2 layer Color mode)

Sets the color mode for L2 layer

0 Indirect color (8 bits/pixel) mode

1 Direct color (16 bits/pixel) mode

L2EM (L2 layer Extended Mode)

Register address	DisplayBaseAddress + 130_H					
Bit number	31 : 30	29 : 28 : 27 : 26 : 25 : 24	23 : 22 : 21 : 20	19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : ----- : 4 : 3 : 2	1	0
Bit field name	L2EC	Reserved	L2PB	Reserved	L2OM	L2WP
R/W	RW	R0	RW	R0	RW	RW
Initial value	00	0	0	0	0	0

Bit 0 L2 WP (L2 layer Window Position enable)

Selects the display position of L2 layer

0 Compatibility mode display (ML layer supported)

1 Window display

Bit 1 L2OM (L2 layer Overlay Mode)

Selects the overlay mode for L2 layer

0 Compatibility mode

1 Extended mode

Bit 23 to 20 L2PB (L2 layer Palette Base)

Shows the value added to the index when subtracting palette of L2 layer. 16 times of setting value is added.

Bit 31 and 30 L2EC (L2 layer Extended Color mode)

Sets extended color mode for L2 layer

00 Mode determined by L2C

01 Direct color (24 bits/pixel) mode

1x Reserved

L2OA0 (L2 layer Origin Address 0)

Register address	DisplayBaseAddress + 44_H		
Bit number	31 : 30 : 29 : 28 : 27 : 26	25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4	3 : 2 : 1 : 0
Bit field name	Reserved	L2OA0	
R/W	R0	RW	R0
Initial value	0	Don’t care	0000

This register sets the origin address of the logic frame of the L2 layer in frame 0. Since lower 4 bits are fixed to “0”, this address is 16-byte aligned.

L2DA0 (L2 layer Display Address 0)

Register address	DisplayBaseAddress + 48_H
Bit number	31 : 30 : 29 : 28 : 27 : 26	25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	Reserved	L2DA0
R/W	R0	RW
Initial value	0	Don’t care

This register sets the origin address of the L2 layer in frame 0. For the direct color mode (16 bits/pixel), the lower 1 bit is “0” and this address is 2-byte aligned.

L2OA1 (L2 layer Origin Address 1)

Register address	DisplayBaseAddress + $4C_H$		
Bit number	31 : 30 : 29 : 28 : 27 : 26	25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4	3 : 2 : 1 : 0
Bit field name	Reserved	L2OA1	
R/W	R0	RW	R0
Initial value	0	Don’t care	0000

This register sets the origin address of the logic frame of the L2 layer in frame 1. Since lower 4-bits are fixed to “0”, this address is 16-byte aligned.

L2DA1 (L2 layer Display Address 1)

Register address	DisplayBaseAddress + 50_H	
Bit number	31 : 30 : 29 : 28 : 27 : 26	25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	Reserved	L2DA1
R/W	R0	RW
Initial value	0	Don’t care

This register sets the origin address of the L2 layer in frame 1. For the direct color mode (16 bits/pixel), the lower 1 bit is “0” and this address is 2-byte aligned.

L2DX (L2 layer Display position X)

Register address	DisplayBaseAddress + 54_H	
Bit number	15 : 14 : 13 : 12	11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	Reserved	L2DX
R/W	R0	RW
Initial value	0	Don’t care

This register sets the display starting position (X coordinates) of the L2 layer on the basis of the origin of the logic frame in pixels.

L2DY (L2 layer Display position Y)

Register address	DisplayBaseAddress + 56_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L2DY											
R/W	R0				RW											
Initial value	0				Don't care											

This register sets the display starting position (Y coordinates) of the L2 layer on the basis of the origin of the logic frame in pixels.

L2WX (L2 layer Window position X)

Register address	DisplayBaseAddress + 134_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L2WX											
R/W	R0				RW											
Initial value	0				Don't care											

This register sets the X coordinates of the display position of the L2 layer window.

L2WY (L2 layer Window position Y)

Register address	DisplayBaseAddress + 136_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L2WY											
R/W	R0				RW											
Initial value	0				Don't care											

This register sets the Y coordinates of the display position of the L2 layer window.

L2WW (L2 layer Window Width)

Register address	DisplayBaseAddress + 138_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L2WW											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the horizontal direction display size (width) of the L2 layer window. Do not specify “0”.

L2WH (L2 layer Window Height)

Register address	DisplayBaseAddress + $13A_H$															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L2WH											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the vertical direction display size (height) of the L2 layer window. Setting value + 1 is the height.

L3M (L3 layer Mode)

Register address	DisplayBaseAddress + 58_H					
Bit number	31	30 29	28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	L3C	L3FLP	Reserved	L3W	Reserved	L3H
R/W	RW	R0	R0	RW	R0	RW
Initial value	0	0	0	Don't care	0	Don't care

Bit 11 to 0 — L3H (L3 layer Height)

Specifies the height of the logic frame of the L3 layer in pixel units. Setting value + 1 is the height

Bit 23 to 16 — L3W (L3 layer memory Width)

Sets the memory width (stride) of the logic frame of the L3 layer in 64-byte units

Bit 30 and 29 — L3FLP (L3 layer Flip mode)

Sets flipping mode for L3 layer

- 00 Displays frame 0
- 01 Displays frame 1
- 10 Switches frame 0 and 1 alternately for display
- 11 Reserved

Bit 31 — L3C (L3 layer Color mode)

Sets the color mode for L3 layer

- 0 Indirect color (8 bits/pixel) mode
- 1 Direct color (16 bits/pixel) mode

L3EM (L3 layer Extended Mode)

Register address	DisplayBaseAddress + 140_H					
Bit number	31 30	29 28 27 26 25 24	23 22 21 20	19 18 17 16 15 14 13 12 11 10 – – – 4 3 2	1	0
Bit field name	L3EC	Reserved	L3PB	Reserved	L3OM	L3WP
R/W	RW	R0	RW	R0	RW	RW
Initial value	00	0	0	0		0

Bit 0 L3 WP (L3 layer Window Position enable)

Selects the display position of L3 layer

0 Compatibility mode display (MR layer supported)

1 Window display

Bit 1 L3OM (L3 layer Overlay Mode)

Selects the overlay mode for L3 layer

0 Compatibility mode

1 Extended mode

Bit 23 to 20 L3PB (L3 layer Palette Base)

Shows the value added to the index when subtracting palette of L3 layer. 16 times of setting value is added.

Bit 31 and 30 L3EC (L3 layer Extended Color mode)

Sets extended color mode for L3 layer

00 Mode determined by L3C

01 Direct color (24 bits/pixel) mode

1x Reserved

L3OA0 (L3 layer Origin Address 0)

Register address	DisplayBaseAddress + $5C_H$		
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
Bit field name	Reserved	L3OA0	
R/W	R0	RW	R0
Initial value	0	Don't care	0000

This register sets the origin address of the logic frame of the L3 layer in frame 0. Since lower 4 bits are fixed to "0", this address is 16-byte aligned.

L3DA0 (L3 layer Display Address 0)

Register address	DisplayBaseAddress + 60_H	
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	L3DA0
R/W	R0	RW
Initial value	0	Don't care

This register sets the origin address of the L3 layer in frame 0. For the direct color mode (16 bits/pixel), the lower 1 bit is "0" and this address is 2-byte aligned.

L3OA1 (L3 layer Origin Address 1)

Register address	DisplayBaseAddress + 64_H		
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
Bit field name	Reserved	L3OA1	
R/W	R0	RW	R0
Initial value	0	Don't care	0000

This register sets the origin address of the logic frame of the L3 layer in frame 1. Since lower 4-bits are fixed to "0", this address is 16-byte aligned.

L3OA1 (L3 layer Display Address 1)

Register address	DisplayBaseAddress + 68_H	
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	L3DA1
R/W	R0	RW
Initial value	0	Don't care

This register sets the origin address of the L3 layer in frame 1. For the direct color mode (16 bits/pixel), the lower 1 bit is "0" and this address is 2-byte aligned.

L3DX (L3 layer Display position X)

Register address	DisplayBaseAddress + $6C_H$	
Bit number	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	L3DX
R/W	R0	RW
Initial value	0	Don't care

This register sets the display starting position (X coordinates) of the L3 layer on the basis of the origin of the logic frame in pixels.

L3DY (L3 layer Display position Y)

Register address	DisplayBaseAddress + $6E_H$															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L3DY											
R/W	R0				RW											
Initial value	0				Don't care											

This register sets the display starting position (Y coordinates) of the L3 layer on the basis of the origin of the logic frame in pixels.

L3WX (L3 layer Window position X)

Register address	DisplayBaseAddress + 144_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L3WX											
R/W	R0				RW											
Initial value	0				Don't care											

This register sets the X coordinates of the display position of the L3 layer window.

L3WY (L3 layer Window position Y)

Register address	DisplayBaseAddress + 146_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L3WY											
R/W	R0				RW											
Initial value	0				Don't care											

This register sets the Y coordinates of the display position of the L3 layer window.

L3WW (L3 layer Window Width)

Register address	DisplayBaseAddress + 148_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L3WW											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the horizontal direction display size (width) of the L3 layer window. Do not specify “0”.

L3WH (L3-layer Window Height)

Register address	DisplayBaseAddress + $14A_H$															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L3WH											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the vertical direction display size (height) of the L3 layer window. Setting value + 1 is the height.

L4M (L4 layer Mode)

Register address	DisplayBaseAddress + 70_H						
Bit number	31	30 29	28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	L4C	L4FLP	Reserved	L4W	Reserved	L4H
R/W	RW	RW	R0	RW	R0	RW
Initial value			0	Don't care	0	Don't care

Bit 11 to 0 L4H (L4 layer Height)

Specifies the height of the logic frame of the L4 layer in pixel units. Setting value + 1 is the height

Bit 23 to 16 L4W (L4 layer memory Width)

Sets the memory width (stride) logic frame of the L4 layer in 64-byte units

Bit 30 and 29 L4FLP (L4 layer Flip mode)

Sets flipping mode for L4 layer

00 Displays frame 0

01 Displays frame 1

10 Switches frame 0 and 1 alternately for display

11 Reserved

Bit 31 L4C (L4 layer Color mode)

Sets the color mode for L4 layer

0 Indirect color (8 bits/pixel) mode

1 Direct color (16 bits/pixel) mode

L4EM (L4 layer Extended Mode)

Register address	DisplayBaseAddress + 150_H				
Bit number	31 30	29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 – – – 4 3 2	1	0
Bit field name	L4EC	Reserved	Reserved	L4OM	L4WP
R/W	RW	R0	R0	RW	RW
Initial value	00	0	0		0

Bit 0 L4 WP (L4 layer Window Position enable)

Selects the display position of L4 layer

0 Compatibility mode display (BL layer supported)

1 Window display

Bit 1 L4OM (L4 layer Overlay Mode)

Selects the overlay mode for L4 layer

0 Compatibility mode

1 Extended mode

Bit 31 and 30 L4EC (L4 layer Extended Color mode)

Sets extended color mode for L4 layer

00 Mode determined by L4C

01 Direct color (24 bits/pixel) mode

1x Reserved

L4OA0 (L4 layer Origin Address 0)

Register address	DisplayBaseAddress + 74_H																														
Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved						L4OA0																									
R/W	R0						RW																						R0			
Initial value	0						Don't care																						0000			

This register sets the origin address of the logic frame of the L4 layer in frame 0. Since lower 4 bits are fixed to "0", this address is 16-byte aligned.

L4DA0 (L4 layer Display Address 0)

Register address	DisplayBaseAddress + 78_H																														
Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved						L4DA0																									
R/W	R0						RW																									
Initial value	0						Don't care																									

This register sets the origin address of the L4 layer in frame 0. For the direct color mode (16 bits/pixel), the lower 1 bit is "0" and this address is 2-byte aligned.

L4OA1 (L4 layer Origin Address 1)

Register address	DisplayBaseAddress + $7C_H$																														
Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved						L4OA1																									
R/W	R0						RW																						R0			
Initial value	0						Don't care																						0000			

This register sets the origin address of the logic frame of the L4 layer in frame 1. Since lower 4-bits are fixed to "0", this address is 16-byte aligned.

L4DA1 (L4 layer Display Address 1)

Register address	DisplayBaseAddress + 80_H																														
Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved						L4DA1																									
R/W	R0						RW																									
Initial value	0						Don't care																									

This register sets the origin address of the L4 layer in frame 1. For the direct color mode (16 bits/pixel), the lower 1 bit is "0" and this address is 2-byte aligned.

L4DX (L4 layer Display position X)

Register address	DisplayBaseAddress + 84_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L4DX											
R/W	R0				RW											
Initial value	0				Don't care											

This register sets the display starting position (X coordinates) of the L4 layer on the basis of the origin of the logic frame in pixels.

L4DY (L4 layer Display position Y)

Register address	DisplayBaseAddress + 86_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L4DY											
R/W	R0				RW											
Initial value	0				Don't care											

This register sets the display starting position (Y coordinates) of the L4 layer on the basis of the origin of the logic frame in pixels.

L4WX (L4 layer Window position X)

Register address	DisplayBaseAddress + 154_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L4WX											
R/W	R0				RW											
Initial value	0				Don't care											

This register sets the X coordinates of the display position of the L4 layer window.

L4WY (L4 layer Window position Y)

Register address	DisplayBaseAddress + 156_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L4WY											
R/W	R0				RW											
Initial value	0				Don't care											

This register sets the Y coordinates of the display position of the L4 layer window.

L4WW (L4 layer Window Width)

Register address	DisplayBaseAddress + 158_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L4WW											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the horizontal direction display size (width) of the L4 layer window. Do not specify “0”.

L4WH (L4 layer Window Height)

Register address	DisplayBaseAddress + $15A_H$															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L4WH											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the vertical direction display size (height) of the L4 layer window. Setting value + 1 is the height.

L5M (L5 layer Mode)

Register address	DisplayBaseAddress + 88_H					
Bit number	31	30 29	28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	L5C	L5FLP	Reserved	L5W	Reserved	L5H
R/W	RW	RW	R0	RW	R0	RW
Initial value			0	Don't care	0	Don't care

Bit 11 to 0 L5H (L5 layer Height)

Specifies the height of the logic frame of the L5 layer in pixel units. Setting value + 1 is the height

Bit 23 to 16 L5W (L5 layer memory Width)

Sets the memory width (stride) logic frame of the L5 layer in 64-byte units

Bit 30 and 29 L5FLP (L5 layer Flip mode)

Sets flipping mode for L5 layer

00 Displays frame 0

01 Displays frame 1

10 Switches frame 0 and 1 alternately for display

11 Reserved

Bit 31 L5C (L5 layer Color mode)

Sets the color mode for L5 layer

0 Indirect color (8 bits/pixel) mode

1 Direct color (16 bits/pixel) mode

L5EM (L5 layer Extended Mode)

Register address	DisplayBaseAddress + 110_H				
Bit number	31 : 30	29 : 28 : 27 : 26 : 25 : 24	23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : – – – : 4 : 3 : 2	1	0
Bit field name	L5EC	Reserved	Reserved	L5OM	L5WP
R/W	RW	R0	R0	RW	RW
Initial value	00	0	0		0

Bit 0 L5 WP (L5 layer Window Position enable)

Selects the display position of L5 layer

0 Compatibility mode display (BR layer supported)

1 Window display

Bit 1 L5OM (L5 layer Overlay Mode)

Selects the overlay mode for L5 layer

0 Compatibility mode

1 Extended mode

Bit 31 to 30 L5EC (L5 layer Extended Color mode)

Sets extended color mode for L5 layer

00 Mode determined by L5C

01 Direct color (24 bits/pixel) mode

1x Reserved

L5OA0 (L5 layer Origin Address 0)

Register address	DisplayBaseAddress + $8C_H$		
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
Bit field name	Reserved	L5OA0	
R/W	R0	RW	R0
Initial value	0	Don’t care	0000

This register sets the origin address of the logic frame of the L5 layer in frame 0. Since lower 4 bits are fixed to “0”, this address is 16-byte aligned.

L5DA0 (L5 layer Display Address 0)

Register address	DisplayBaseAddress + 90_H	
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	L5DA0
R/W	R0	RW
Initial value	0	Don’t care

This register sets the origin address of the L5 layer in frame 0. For the direct color mode (16 bits/pixel), the lower 1 bit is “0” and this address is 2-byte aligned.

L5OA1 (L5 layer Origin Address 1)

Register address	DisplayBaseAddress + 94_H		
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
Bit field name	Reserved	L5OA1	
R/W	R0	RW	R0
Initial value	0	Don’t care	0000

This register sets the origin address of the logic frame of the L5 layer in frame 1. Since lower 4-bits are fixed to “0”, this address is 16-byte aligned.

L5DA1 (L5 layer Display Address 1)

Register address	DisplayBaseAddress + 98_H	
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	L5DA1
R/W	R0	RW
Initial value	0	Don’t care

This register sets the origin address of the L5 layer in frame 1. For the direct color mode (16 bits/pixel), the lower 1 bit is “0” and this address is 2-byte aligned.

L5DX (L5 layer Display position X)

Register address	DisplayBaseAddress + $9C_H$	
Bit number	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	L5DX
R/W	R0	RW
Initial value	0	Don’t care

This register sets the display starting position (X coordinates) of the L5 layer on the basis of the origin of the logic frame in pixels.

L5DY (L5 layer Display position Y)

Register address	DisplayBaseAddress + 9E$_H$															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L5DY											
R/W	R0				RW											
Initial value	0				Don't care											

This register sets the display starting position (Y coordinates) of the L5 layer on the basis of the origin of the logic frame in pixels.

L5WX (L5 layer Window position X)

Register address	DisplayBaseAddress + 164$_H$															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L5WX											
R/W	R0				RW											
Initial value	0				Don't care											

This register sets the X coordinates of the display position of the L5 layer window.

L5WY (L5 layer Window position Y)

Register address	DisplayBaseAddress + 166$_H$															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L5WY											
R/W	R0				RW											
Initial value	0				Don't care											

This register sets the Y coordinates of the display position of the L5 layer window.

L5WW (L5 layer Window Width)

Register address	DisplayBaseAddress + 168$_H$															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L5WW											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the horizontal direction display size (width) of the L5 layer window. Do not specify "0".

L5WH (L5 layer Window Height)

Register address	DisplayBaseAddress + 16A$_H$															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				L5WH											
R/W	R0				RW											
Initial value	0				Don't care											

This register controls the vertical direction display size (height) of the L5 layer window. Setting value + 1 is the height.

CUTC (Cursor Transparent Control)

Register address	DisplayBaseAddress + A0$_H$															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved							CUZT	CUTC							
R/W	R0							RW	RW							
Initial value	0							Don't care	Don't care							

Bit 7 to 0 CUTC (Cursor Transparent Code)

Sets color code handled as transparent code

Bit 8 CUZT (Cursor Zero Transparency)

Defines handling of color code 0

0 Code 0 as non-transparency color

1 Code 0 as transparency color

CPM (Cursor Priority Mode)

Register address	DisplayBaseAddress + A2$_H$							
Bit number	7	6	5	4	3	2	1	0
Bit field name	Reserved		CEN1	CEN0	Reserved		CUO1	CUO0
R/W	R0		RW	RW	R0		RW	RW
Initial value	0		0	0	0		0	0

This register controls the display priority of cursors. Cursor 0 is always preferred to cursor 1.

Bit 0 CUO0 (Cursor Overlap 0)

Sets display priority between cursor 0 and pixels of Console layer

0 Puts cursor 0 at lower than L0 layer.

1 Puts cursor 0 at higher than L0 layer.

Bit 1 CUO1 (Cursor Overlap 1)

Sets display priority between cursor 1 and C layer

0 Puts cursor 1 at lower than L0 layer.

1 Puts cursor 1 at lower than L0 layer.

Bit 4 CEN0 (Cursor Enable 0)

Sets enabling display of cursor 0

0 Disabled

1 Enabled

Bit 5 CEN1 (Cursor Enable 1)

Sets enabling display of cursor 1

0 Disabled

1 Enabled

CUOA0 (Cursor-0 Origin Address)

<table>
<tr><td>Register address</td><td colspan="32">DisplayBaseAddress + $A4_H$</td></tr>
<tr><td>Bit number</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Bit field name</td><td colspan="6">Reserved</td><td colspan="26">CUOA0</td></tr>
<tr><td>R/W</td><td colspan="6">R0</td><td colspan="22">RW</td><td colspan="4">R0</td></tr>
<tr><td>Initial value</td><td colspan="6">0</td><td colspan="22">Don’t care</td><td colspan="4">0000</td></tr>
</table>

This register sets the start address of the cursor 0 pattern. Since lower 4 bits are fixed to “0”, this address is 16-byte aligned.

CUX0 (Cursor-0 X position)

<table>
<tr><td>Register address</td><td colspan="16">DisplayBaseAddress + $A8_H$</td></tr>
<tr><td>Bit number</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Bit field name</td><td colspan="4">Reserved</td><td colspan="12">CUX0</td></tr>
<tr><td>R/W</td><td colspan="4">R0</td><td colspan="12">RW</td></tr>
<tr><td>Initial value</td><td colspan="4">0</td><td colspan="12">Don’t care</td></tr>
</table>

This register sets the display position (X coordinates) of the cursor 0 in pixels. The reference position of the coordinates is the top left of the cursor pattern.

CUY0 (Cursor-0 Y position)

<table>
<tr><td>Register address</td><td colspan="16">DisplayBaseAddress + Aa_H</td></tr>
<tr><td>Bit number</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Bit field name</td><td colspan="4">Reserved</td><td colspan="12">CUY0</td></tr>
<tr><td>R/W</td><td colspan="4">R0</td><td colspan="12">RW</td></tr>
<tr><td>Initial value</td><td colspan="4">0</td><td colspan="12">Don’t care</td></tr>
</table>

This register sets the display position (Y coordinates) of the cursor 0 in pixels. The reference position of the coordinates is the top left of the cursor pattern.

CUOA1 (Cursor-1 Origin Address)

Register address	DisplayBaseAddress + AC_H		
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
Bit field name	Reserved	CUOA1	
R/W	R0	RW	R0
Initial value	0	Don't care	0000

This register sets the start address of the cursor 1 pattern. Since lower 4 bits are fixed to "0", this address is 16-byte aligned.

CUX1 (Cursor-1 X position)

Register address	DisplayBaseAddress + $B0_H$	
Bit number	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	CUX1
R/W	R0	RW
Initial value	0	Don't care

This register sets the display position (X coordinates) of the cursor 1 in pixels. The reference position of the coordinates is the top left of the cursor pattern.

CUY1 (Cursor-1 Y position)

Register address	DisplayBaseAddress + $B2_H$	
Bit number	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	CUY1
R/W	R0	RW
Initial value	0	Don't care

This register sets the display position (Y coordinates) of the cursor 1 in pixels. The reference position of the coordinates is the top left of the cursor pattern.

MDC (Multi Display Control)

Register address	DisplayBaseAddress + 170_H			
Bit number	31	30 29 28 24 23 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Bit field name	MDen	reserve	SC1en	SC0en
R/W	RW	R0	RW	RW
Initial value	0	0	X	X

This register controls dual display mode.

Bit 0 SC0en0 (screen 0 enable 0)
- 0: L0 is not included into screen 0
- 1: L0 is included into screen 0

Bit 1 SC0en1 (screen 0 enable 1)
- 0: L1 is not included into screen 0
- 1: L1 is included into screen 0

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Bit 5 SC0en5 (screen 0 enable 5)
- 0: L5 is not included into screen 0
- 1: L5 is included into screen 0

Bit 6 SC0en6 (screen 0 enable 6)
- 0: Cursor0 is not included into screen 0
- 1: Cursor0 is included into screen 0

Bit 7 SC0en7 (screen 0 enable 7)
- 0: Cursor1 is not included into screen 0
- 1: Cursor1 is included into screen 0

Bit 8 SC1en0 (screen 1 enable 0)
- 0: L0 is not included into screen 1
- 1: L0 is included into screen 1

Bit 9 SC1en1 (screen 1 enable 1)
- 0: L1 is not included into screen 1
- 1: L1 is included into screen 1

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Bit 13 SC1en5 (screen 1 enable 5)
- 0: L5 is not included into screen 1
- 1: L5 is included into screen 1

Bit 14 SC1en6 (screen 1 enable 6)

0: Cursor 0 is not included into screen 1

1: Cursor 0 is included into screen 1

Bit 15 SC1en7 (screen 1 enable 7)

0: Cursor 1 is not included into screen 1

1: Cursor 1 is included into screen 1

Bit 31 MDen (multi display enable)

This enables multi or dual display mode

0: Single display mode

1: Dual display mode

DLS (Display Layer Select)

Register address	DisplayBaseAddress + 180_H											
Bit number	31:30:29: ----- :25:24	23	22:21:20	19	18:17:16	15	14:13:12	11	10: 9 : 8	7	6 : 5 : 4	3	2 : 1 : 0
Bit field name	Reserved	DLS5		DLS4		DLS3		DLS2		DLS1		DSL0	
R/W	R0	R0	RW	R0	RW	R0	RW	R0	RW	R0	RW	R0	RW
Initial value			101		100		011		010		001		000

This register defines the blending sequence.

Bit 3 to 0 DSL0 (Display Layer Select 0)

Selects the top layer subjected to blending.

0000 L0 layer
0001 L1 layer
: :
0101 L5 layer
0110 Reserved
: :
0110 Reserved
0111 Not selected

Bit 7 to 4 DSL1 (Display Layer Select 1)

Selects the second layer subjected to blending. The bit values are the same as DSL0.

Bit 11 to 8 DSL2 (Display Layer Select 2)

Selects the third layer subjected to blending. The bit values are the same as DSL0.

Bit 15 to 12 DSL3 (Display Layer Select 3)

Selects the fourth layer subjected to blending. The bit values are the same as DSL0.

Bit 19 to 16 DSL4 (Display Layer Select 4)

Selects the fifth layer subjected to blending. The bit values are the same as DSL0.

Bit 23 to 20 DSL5 (Display Layer Select 5)

Selects the bottom layer subjected to blending. The bit values are the same as DSL0.

DBGC (Display Background Color)

Register address	DisplayBaseAddress + 184_H			
Bit number	31 30 29 ----- 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Bit field name	Reserved	DBGR	DBGG	DBGB
R/W	R0			
Initial value				

This register specifies the color to be displayed in areas outside the display area of each layer on the window.

Bit 7 to 0 DBGB (Display Background Blue)

Specifies the blue level of the background color.

Bit 15 to 8 DBGG (Display Background Green)

Specifies the green level of the background color.

Bit 23 to 16 DBGR (Display Background Red)

Specifies the red level of the background color.

L0BLD (L0 Blend)

Register address	DisplayBaseAddress + $B4_H$						
Bit number	31 30 29 28 ----- 20 19 18 17	16	15	14	13	12 11 10 9 8	7 6 5 4 3 2 1 0
Bit field name	Reserved	L0BE	L0BS	L0BI	L0BP	Reserved	L0BR
R/W							
Initial value							

This register specifies the blend parameters for the L0 layer. This register corresponds to BRATIO or BMODE for previous products.

Bit 7 to 0 L0BR (L0 layer Blend Ratio)

Sets the blend ratio. Basically, the blend ratio is setting value/256.

Bit 13 L0BP (L0 layer Blend Plane)

Specifies that the L5 layer is the blend plane.

0 Value of L0BR used as blend ratio

1 Pixel of L5 layer used as blend ratio

Bit 14 L0BI (L0 layer Blend Increment)

Selects whether or not 1/256 is added when the blend ratio is not “0”.

0 Blend ratio calculated as is

1 1/256 added when blend ratio $\neq$ 0

Bit 15 L0BS (L0 layer Blend Select)

Selects the blend calculation expression.

0 Upper image $\times$ Blend ratio $+$ Lower image $\times$ (1 – Blend ratio)

1 Upper image $\times$ (1 – Blend ratio) $+$ Lower image $\times$ Blend ratio

Bit 16 L0BE (L0 layer Blend Enable)

This bit enables blending.

0 Overlay via transparent color

1 Overlay via blending

Before blending, the blend mode must be specified using L0BE, and alpha must also be enabled for L0 layer display data. For direct color, alpha is specified using the MSB of data; for indirect color, alpha is specified using the MSB of palette data.

L1BLD (L1 Blend)

Register address	DisplayBaseAddress + 188_H						
Bit number	31 30 29 28 ----- 20 19 18 17	16	15	14	13	12 11 10 9 8	7 6 5 4 3 2 1 0
Bit field name	Reserved	L1BE	L1BS	L1BI	L1BP	Reserved	L1BR
R/W							
Initial value							

This register specifies the blend parameters for the L1 layer.

Bit 7 to 0 L1BR (L1 layer Blend Ratio)

Sets the blend ratio. Basically, the blend ratio is setting value/256.

Bit 13 L1BP (L1 layer Blend Plane)

Specifies that the L5 layer is the blend plane.

0 Value of L1BR used as blend ratio

1 Pixel of L5 layer used as blend ratio

Bit 14 L1BI (L1 layer Blend Increment)

Selects whether or not 1/256 is added when the blend ratio is not “0”.

0 Blend ratio calculated as is

1 1/256 added when blend ratio $\neq$ 0

Bit 15 L1BS (L1 layer Blend Select)

Selects the blend calculation expression.

0 Upper image $\times$ Blend ratio $+$ Lower image $\times$ (1 – Blend ratio)

1 Upper image $\times$ (1 – Blend ratio) $+$ Lower image $\times$ Blend ratio

Bit 16 L1BE (L1 layer Blend Enable)

This bit enables blending.

0 Overlay via transparent color

1 Overlay via blending

Before blending, the blend mode must be specified using L1BE, and alpha must also be enabled for L1 layer display data. For direct color, alpha is specified using the MSB of data; for indirect color, alpha is specified using the MSB of palette data.

L2BLD (L2 Blend)

Register address	DisplayBaseAddress + $18C_H$						
Bit number	31 30 29 28 ----- 20 19 18 17	16	15	14	13	12 11 10 9 8	7 6 5 4 3 2 1 0
Bit field name	Reserved	L2BE	L2BS	L2BI	L2BP	Reserved	L2BR
R/W							
Initial value							

This register specifies the blend parameters for the L2 layer.

Bit 7 to 0 L2BR (L2 layer Blend Ratio)

Sets the blend ratio. Basically, the blend ratio is setting value/256.

Bit 13 L2BP (L2 layer Blend Plane)

Specifies that the L5 layer is the blend plane.

0 Value of L2BR used as blend ratio

1 Pixel of L5 layer used as blend ratio

Bit 14 L2BI (L2 layer Blend Increment)

Selects whether or not 1/256 is added when the blend ratio is not "0".

0 Blend ratio calculated as is

1 1/256 added when blend ratio $\neq$ 0

Bit 15 L2BS (L2 layer Blend Select)

Selects the blend calculation expression.

0 Upper image $\times$ Blend ratio $+$ Lower image $\times$ (1 – Blend ratio)

1 Upper image $\times$ (1 – Blend ratio) $+$ Lower image $\times$ Blend ratio

Bit 16 L2BE (L2 layer Blend Enable)

This bit enables blending.

0 Overlay via transparent color

1 Overlay via blending

Before blending, the blend mode must be specified using L2BE, and alpha must also be enabled for L2 layer display data. For direct color, alpha is specified using the MSB of data; for indirect color, alpha is specified using the MSB of palette data.

L3BLD (L3 Blend)

Register address	DisplayBaseAddress + 190_H						
Bit number	31 30 29 28 ----- 20 19 18 17	16	15	14	13	12 11 10 9 8	7 6 5 4 3 2 1 0
Bit field name	Reserved	L3BE	L3BS	L3BI	L3BP	Reserved	L3BR
R/W							
Initial value							

This register specifies the blend parameters for the L3 layer.

Bit 7 to 0 L3BR (L3 layer Blend Ratio)

Sets the blend ratio. Basically, the blend ratio is setting value/256.

Bit 13 L3BP (L3 layer Blend Plane)

Specifies that the L5 layer is the blend plane.

0 Value of L3BR used as blend ratio

1 Pixel of L5 layer used as blend ratio

Bit 14 L3BI (L3 layer Blend Increment)

Selects whether or not 1/256 is added when the blend ratio is not “0”.

0 Blend ratio calculated as is

1 1/256 added when blend ratio $\neq$ 0

Bit 15 L3BS (L3 layer Blend Select)

Selects the blend calculation expression.

0 Upper image $\times$ Blend ratio $+$ Lower image $\times$ (1 – Blend ratio)

1 Upper image $\times$ (1 – Blend ratio) $+$ Lower image $\times$ Blend ratio

Bit 16 L3BE (L3 layer Blend Enable)

This bit enables blending.

0 Overlay via transparent color

1 Overlay via blending

Before blending, the blend mode must be specified using L3BE, and alpha must also be enabled for L3 layer display data. For direct color, alpha is specified using the MSB of data; for indirect color, alpha is specified using the MSB of palette data.

L4BLD (L4 Blend)

Register address	DisplayBaseAddress + 194_H						
Bit number	31 : 30 : 29 : 28 : ----- : 20 : 19 : 18 : 17	16	15	14	13	12 : 11 : 10 : 9 : 8	7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	Reserved	L4BE	L4BS	L4BI	L4BP	Reserved	L4BR
R/W							
Initial value							

This register specifies the blend parameters for the L4 layer.

Bit 7 to 0 L4BR (L4 layer Blend Ratio)

Sets the blend ratio. Basically, the blend ratio is setting value/256.

Bit 13 L4BP (L4 layer Blend Plane)

Specifies that the L5 layer is the blend plane.

0 Value of L4BR used as blend ratio

1 Pixel of L5 layer used as blend ratio

Bit 14 L4BI (L4 layer Blend Increment)

Selects whether or not 1/256 is added when the blend ratio is not “0”.

0 Blend ratio calculated as is

1 1/256 added when blend ratio $\neq$ 0

Bit 15 L4BS (L4 layer Blend Select)

Selects the blend calculation expression.

0 Upper image $\times$ Blend ratio $+$ Lower image $\times$ (1 – Blend ratio)

1 Upper image $\times$ (1 – Blend ratio) $+$ Lower image $\times$ Blend ratio

Bit 16 L4BE (L4 layer Blend Enable)

This bit enables blending.

0 Overlay via transparent color

1 Overlay via blending

Before blending, the blend mode must be specified using L4BE, and alpha must also be enabled for L4 layer display data. For direct color, alpha is specified using the MSB of data; for indirect color, alpha is specified using the MSB of palette data.

L5BLD (L5 Blend)

Register address	DisplayBaseAddress + 198h					
Bit number	31 30 29 28 ----- 21 20 19 18 17	16	15	14	13 12 11 10 9 8	7 6 5 4 3 2 1 0
Bit field name	Reserved	L5BE	L5BS	L5BI	Reserved	L5BR
R/W	R0	RW	RW	RW	R0	RW
Initial value		0	0	0		

This register specifies the blend parameters for the L5 layer.

Bit 7 to 0　L5BR (L5 layer Blend Ratio)

Sets the blend ratio. Basically, the blend ratio is setting value/256.

Bit 14　L5BI (L5 layer Blend Increment)

Selects whether or not 1/256 is added when the blend ratio is not “0”.

0　Blend ratio calculated as is

1　1/256 added when blend ratio ≠ 0

Bit 15　L5BS (L5 layer Blend Select)

Selects the blend calculation expression.

0　Upper image × Blend ratio + Lower image × (1 – Blend ratio)

1　Upper image × (1 – Blend ratio) + Lower image × Blend ratio

Bit 16　L5BE (L5 layer Blend Enable)

This bit enables blending.

0　Overlay via transparent color

1　Overlay via blending

Before blending, the blend mode must be specified using L5BE, and alpha must also be enabled for L5 layer display data. For direct color, alpha is specified using the MSB of data; for indirect color, alpha is specified using the MSB of palette data.

L0TC (L0 layer Transparency Control)

Register address	DisplayBaseAddress + BC_H															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	L0ZT	L0TC														
R/W	RW	RW														
Initial value	0	Don't care														

This register sets the transparent color for the L0 layer. Color set by this register is transparent in blend mode. When L0TC = 0 and L0ZT = 0, color 0 is displayed in black (transparent).

This register corresponds to the CTC register for previous products.

Bit 14 to 0 L0TC (L0 layer Transparent Color)

Sets transparent color code for the L0 layer. In indirect color mode (8 bits/pixel) bits 7 to 0 are used.

Bit 15 L0ZT (L0 layer Zero Transparency)

Sets handling of color code 0 in L0 layer

0: Code 0 as transparency color

1: Code 0 as non-transparency color

L2TC (L2 layer Transparency Control)

Register address	DisplayBaseAddress + $C2_H$															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	L2ZT	L2TC														
R/W	RW	RW														
Initial value	0	Don't care														

This register sets the transparent color for the L2 layer.

When L2TC = 0 and L2ZT = 0, color 0 is displayed in black (transparent).

This register corresponds to the MLTC register for previous products.

Bit 14 to 0 L2TC (L2 layer Transparent Color)

Sets transparent color code for the L2 layer. In indirect color mode (8 bits/pixel) bits 7 to 0 are used.

Bit 15 L2ZT (L2 layer Zero Transparency)

Sets handling of color code 0 in L2 layer

0 Code 0 as transparency color

1 Code 0 as non-transparency color

L3TC (L3 layer Transparency Control)

Register address	DisplayBaseAddress + C0$_{H}$	
Bit number	15	14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	L3ZT	L3TC
R/W	RW	RW
Initial value	0	Don't care

This register sets the transparent color for the L3 layer. When L3TC = 0 and L3ZT = 0, color 0 is displayed in black (transparent).

This register corresponds to the MLTC register for previous products.

Bit 14 to 0 L3TC (L3 layer Transparent Color)

Sets transparent color code for the L3 layer. In indirect color mode (8 bits/pixel) bits 7 to 0 are used.

Bit 15 L3ZT (L3 layer Zero Transparency)

Sets handling of color code 0 in L3 layer

0 Code 0 as transparency color

1 Code 0 as non-transparency color

L0ETC (L0 layer Extend Transparency Control)

Register address	DisplayBaseAddress + 1A0$_{H}$		
Bit number	31	30 : 29 : 28 : --- : 24	23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	L0EZT	Reserved	L0ETC
R/W	RW	R0	RW
Initial value	0	0	

This register sets the transparent color for the L0 layer. The 24 bits/pixel transparent color is set using this register. The lower 15 bits of this register are physically the same as L0TC. Also, L0ETZ is physically the same as L0TZ.

When L0ETC = 0 and L0EZT = 0, color 0 is displayed in black (transparent).

Bit 23 to 0 L0ETC (L0 layer Extend Transparent Color)

Sets transparent color code for the L0 layer. In indirect color mode (8 bits/pixel) bits 7 to 0 are used.

Bit 31 L0EZT (L0 layer Extend Zero Transparency)

Sets handling of color code 0 in L0 layer

0 Code 0 as transparency color

1 Code 0 as non-transparency color

L1ETC (L1 layer Extend Transparency Control)

Register address	DisplayBaseAddress + $1A4_H$		
Bit number	31	30 : 29 : 28 : --- : 24	23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	L1EZT	Reserved	L1ETC
R/W	RW	R0	RW
Initial value			

This register sets the transparent color for the L1 layer. When L1ETC = 0 and L1EZT = 0, color 0 is displayed in black (transparent).

For YCbCr display, transparent color checking is not performed; processing is always performed assuming that transparent color is not used.

Bit 23 to 0 L1ETC (L1 layer Extend Transparent Color)

Sets transparent color code for the L1 layer. In indirect color mode (8 bits/pixel) bits 7 to 0 are used.

Bit 31 L1EZT (L1 layer Extend Zero Transparency)

Sets handling of color code 0 in L1 layer

0 Code 0 as transparency color

1 Code 0 as non-transparency color

L2ETC (L2 layer Extend Transparency Control)

Register address	DisplayBaseAddress + $1A8_H$		
Bit number	31	30 : 29 : 28 : --- : 24	23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	L2EZT	Reserved	L2ETC
R/W	RW	R0	RW
Initial value			

This register sets the transparent color for the L2 layer. The 24 bits/pixel transparent color is set using this register. The lower 15 bits of this register are physically the same as L2TC. Also, L2ETZ is physically the same as L2TZ.

When L2ETC = 0 and L2EZT = 0, color 0 is displayed in black (transparent).

Bit 23 to 0 L2ETC (L2 layer Extend Transparent Color)

Sets transparent color code for the L2 layer. In indirect color mode (8 bits/pixel) bits 7 to 0 are used.

Bit 31 L2EZT (L2 layer Extend Zero Transparency)

Sets handling of color code 0 in L2 layer

0 Code 0 as transparency color

1 Code 0 as non-transparency color

L3ETC (L3 layer Extend Transparency Control)

Register address	DisplayBaseAddress + $1AC_H$		
Bit number	31	30 : 29 : 28 : --- : 24	23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	L3EZT	Reserved	L3ETC
R/W	RW	R0	RW
Initial value	0	0	

This register sets the transparent color for the L3 layer. The 24 bits/pixel transparent color is set using this register. The lower 15 bits of this register are physically the same as L3TC. Also, L3ETZ is physically the same as L3TZ.

When L3ETC = 0 and L3EZT = 0, color 0 is displayed in black (transparent).

Bit 23 to 0 L3ETC (L3 layer Extend Transparent Color)

Sets transparent color code for the L3 layer. In indirect color mode (8 bits/pixel) bits 7 to 0 are used.

Bit 31 L3EZT (L3 layer Extend Zero Transparency)

Sets handling of color code 0 in L3 layer

0 Code 0 as transparency color

1 Code 0 as non-transparency color

L4ETC (L4 layer Extend Transparency Control)

Register address	DisplayBaseAddress + $1B0_H$		
Bit number	31	30 : 29 : 28 : --- : 24	23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	L4EZT	Reserved	L4ETC
R/W	RW	R0	RW
Initial value	0	0	

This register sets the transparent color for the L4 layer. This register sets the transparent color for the L4 layer. When L4ETC = 0 and L4EZT = 0, color 0 is displayed in black (transparent).

Bit 23 to 0 L4ETC (L4 layer Extend Transparent Color)

Sets transparent color code for the L4 layer. In indirect color mode (8 bits/pixel) bits 7 to 0 are used.

Bit 31 L4EZT (L4 layer Extend Zero Transparency)

Sets handling of color code 0 in L4 layer

0 Code 0 as transparency color

1 Code 0 as non-transparency color

L5ETC (L5 layer Extend Transparency Control)

Register address	DisplayBaseAddress + $1B4_H$		
Bit number	31	30 : 29 : 28 : --- : 24	23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	L5EZT	Reserved	L5ETC
R/W	RW	R0	RW
Initial value	0	0	

This register sets the transparent color for the L5 layer. This register sets the transparent color for the L5 layer. When L5ETC = 0 and L5EZT = 0, color 0 is displayed in black (transparent).

Bit 23 to 0 L5ETC (L5 layer Extend Transparent Color)

Sets transparent color code for the L5 layer. In indirect color mode (8 bits/pixel) bits 7 to 0 are used.

Bit 31 L5EZT (L5 layer Extend Zero Transparency)

Sets handling of color code 0 in L5 layer

0 Code 0 as transparency color

1 Code 0 as non-transparency color

L1YCR0 (L1 layer YC to Red coefficient 0)

Register address	DisplayBaseAddress + 0x1E0			
Bit No.	31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	a12	Reserved	a11
R/W	R0	RW	R0	RW
Initial value	0	000 0000 0000	0	001 0010 1011

This register defines the parameter for the red component at YCbCr/RGB conversion.

Bit 10-0 a11
11-bit signed fixed-point value. The lower 8 bits of the value are placed after the decimal point.
The value is complement representation for 2.

Bit 26-16 a12
11-bit signed fixed-point value. The lower 8 bits of the value are placed after the decimal point.
The value is complement representation for 2.

L1YCR1 (L1 layer YC to Red coefficient 1)

Register address	DisplayBaseAddress + 0x1E4			
Bit No.	31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	b1	Reserved	a13
R/W	R0	RW	R0	RW
Initial value	0	1 1111 0000	0	001 1001 1000

This register defines the parameter for the red component at YCbCr/RGB conversion time.

Bit 10-0 a13
11-bit signed fixed-point value. The lower 8 bits of the value are placed after the decimal point.
The value is complement representation for 2.

Bit 24-16 b1
9-bit signed integer. The value is complement representation for 2.

L1YCG0 (L1 layer YC to Green coefficient 0)

<table>
<tr><td>Register address</td><td colspan="32">DisplayBaseAddress + 0x1E8</td></tr>
<tr><td>Bit No.</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Bit field name</td><td colspan="5">Reserved</td><td colspan="11">a22</td><td colspan="5">Reserved</td><td colspan="11">a21</td></tr>
<tr><td>R/W</td><td colspan="5">R0</td><td colspan="11">RW</td><td colspan="5">R0</td><td colspan="11">RW</td></tr>
<tr><td>Initial value</td><td colspan="5">0</td><td colspan="11">111 1001 1100</td><td colspan="5">0</td><td colspan="11">001 0010 1011</td></tr>
</table>

This register defines the parameter for the green component at YCbCr/RGB conversion time.

Bit 10-0 a21
11-bit signed fixed-point value. The lower 8 bits of the value are placed after the decimal point. The value is complement representation for 2.

Bit 26-16 a22
11-bit signed fixed-point value. The lower 8 bits of the value are placed after the decimal point. The value is complement representation for 2.

L1YCG1 (L1 layer YC to Green coefficient 1)

<table>
<tr><td>Register address</td><td colspan="32">DisplayBaseAddress + 0x1EC</td></tr>
<tr><td>Bit No.</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Bit field name</td><td colspan="7">Reserved</td><td colspan="9">b2</td><td colspan="5">Reserved</td><td colspan="11">a23</td></tr>
<tr><td>R/W</td><td colspan="7">R0</td><td colspan="9">RW</td><td colspan="5">R0</td><td colspan="11">RW</td></tr>
<tr><td>Initial value</td><td colspan="7">0</td><td colspan="9">1 1111 0000</td><td colspan="5">0</td><td colspan="11">111 0010 1111</td></tr>
</table>

This register defines the parameter for the green component at YCbCr/RGB conversion time.

Bit 10-0 a23
11-bit signed fixed-point value. The lower 8 bits of the value are placed after the decimal point. The value is complement representation for 2.

Bit 24-16 b2
9-bit signed integer. The value is complement representation for 2.

L1YCB0 (L1 layer YC to Blue coefficient 0)

Register address	DisplayBaseAddress + 0x1F0			
Bit No.	31	30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	a32	Reserved	a31
R/W	R0	RW	R0	RW
Initial value	0	010 0000 0100	0	001 0010 1011

This register defines the parameter for the blue component at YCbCr/RGB conversion.

Bit 10-0 a31
11-bit signed fixed-point value. The lower 8 bits of the value are placed after the decimal point. The value is complement representation for 2.

Bit 26-16 a32
11-bit signed fixed-point value. The lower 8 bits of the value are placed after the decimal point. The value is complement representation for 2.

L1YCB1 (L1 layer YC to Green coefficient 1)

Register address	DisplayBaseAddress + 0x1F4			
Bit No.	31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8 7 6 5 4 3 2 1 0
Bit field name	Reserved	b3	Reserved	a33
R/W	R0	RW	R0	RW
Initial value	0	1 1111 0000	0	000 0000 0000

This register defines the parameter for the blue component at YCbCr/RGB conversion.

Bit 10-0 a33
11-bit signed fixed-point value. The lower 8 bits of the value are placed after the decimal point. The value is complement representation for 2.

Bit 24-16 b3
The value is a 9-bit signed integer. The value is complement representation for 2.

L0PAL0-255 (L0 layer Palette 0-255)

Register address	DisplayBaseAddress + 400_H -- DisplayBaseAddress + $7FC_H$							
Bit number	31	30 29 28 27 26 25 24	23 22 21 20 19 18	17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2	1 0
Bit field name	A		R		G		B	
R/W	RW	R0	RW	R0	RW	R0	RW	R0
Initial value	Don't care	0000000	Don't care	00	Don't care	00	Don't care	00

These are color palette registers for L0 layer and cursors. In the indirect color mode, a color code in the display frame indicates the palette register number, and the color information set in that register is applied as the display color of that pixel. This register corresponds to the CPALn register for previous products.

Bit 7 to 2 B (Blue)

Sets blue color component

Bit 15 to 10 G (Green)

Sets green color component

Bit 23 to 18 R (Red)

Sets red color component

Bit 31 A (Alpha)

Specifies whether or not to perform blending with lower layers when the blending mode is enabled.

0 Blending not performed even when blending mode enabled
Overlay is performed via transparent color.

1 Blending performed

L1PAL0-255 (L1 layer Palette 0-255)

Register address	DisplayBaseAddress + 800_H -- DisplayBaseAddress + BFC_H							
Bit number	31	30:29:28:27:26:25:24	23:22:21:20:19:18	17:16	15:14:13:12:11:10	9:8	7:6:5:4:3:2	1:0
Bit field name	A		R		G		B	
R/W	RW	R0	RW	R0	RW	R0	RW	R0
Initial value	Don't care	0000000	Don't care	00	Don't care	00	Don't care	00

These are color palette registers for L1 layer and cursors. In the indirect color mode, a color code in the display frame indicates the palette register number, and the color information set in that register is applied as the display color of that pixel. This register corresponds to the MBPALn register for previous products.

Bit 7 to 2 B (Blue)

Sets blue color component

Bit 15 to 10 G (Green)

Sets green color component

Bit 23 to 18 R (Red)

Sets red color component

Bit 31 A (Alpha)

Specifies whether or not to perform blending with lower layers when the blending mode is enabled.

0 Blending not performed even when blending mode enabled
Overlay is performed via transparent color.

1 Blending performed

L2PAL0-255 (L2 layer Palette 0-255)

Register address	DisplayBaseAddress + 1000_H -- DisplayBaseAddress + $13FC_H$							
Bit number	31	30 29 28 27 26 25 24	23 22 21 20 19 18	17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2	1 0
Bit field name	A		R		G		B	
R/W	RW	R0	RW	R0	RW	R0	RW	R0
Initial value	Don't care	0000000	Don't care	00	Don't care	00	Don't care	00

These are color palette registers for L2 layer and cursors. In the indirect color mode, a color code in the display frame indicates the palette register number, and the color information set in that register is applied as the display color of that pixel.

Bit 7 to 2 B (Blue)

Sets blue color component

Bit 15 to 10 G (Green)

Sets green color component

Bit 23 to 18 R (Red)

Sets red color component

Bit 31 A (Alpha)

Specifies whether or not to perform blending with lower layers when the blending mode is enabled.

0 Blending not performed even when blending mode enabled
Overlay is performed via transparent color.

1 Blending performed

L3PAL0-255 (L3 layer Palette 0-255)

Register address	DisplayBaseAddress + 1400_H -- DisplayBaseAddress + $17FC_H$							
Bit number	31	30:29:28:27:26:25:24	23:22:21:20:19:18	17:16	15:14:13:12:11:10	9:8	7:6:5:4:3:2	1:0
Bit field name	A		R		G		B	
R/W	RW	R0	RW	R0	RW	R0	RW	R0
Initial value	Don't care	0000000	Don't care	00	Don't care	00	Don't care	00

These are color palette registers for L3 layer and cursors. In the indirect color mode, a color code in the display frame indicates the palette register number, and the color information set in that register is applied as the display color of that pixel.

Bit 7 to 2 B (Blue)

Sets blue color component

Bit 15 to 10 G (Green)

Sets green color component

Bit 23 to 18 R (Red)

Sets red color component

Bit 31 A (Alpha)

Specifies whether or not to perform blending with lower layers when the blending mode is enabled.

0 Blending not performed even when blending mode enabled
Overlay is performed via transparent color.

1 Blending performed

12.4 Video capture registers

VCM (Video Capture Mode)

Register address	CaptureBaseAddress + 00h											
Bit number	31	30	29	28	27 : 26	25 : 24	23 : 22 : 21	20	19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3	2	1	0
Bit field name	VIE	VIS	Reserve	VICE	Reserve	CM	Reserve	VI	Reserve	NRGB	VS	Rsv
R/W	R/W	R/W	RX	R/W	RX	R/W	RX	R/W	RX	R/W	R/W	RX
Initial value	0	0	X	0	X	00	X	0	X	0	0	X

This register sets the video capture mode. This register is not initialized by software reset.

Bit1 VS (Video Select)
NTSC or PAL is selected for the code error detection (only RBT656 is input)
- 0 NTSC
- 1 PAL

Bit2 NRGB (Native RGB input on)
Native RGB mode is set up.
- 0 RGB video data is accepted via an internal RGB preprocessor which converts RGB to YUV422
- 1 Native RGB

Bit20 VI (Vertical Interpolation)
Sets whether to perform vertical interpolation
- 0 Performs vertical interpolation. The graphics are enlarged vertically by two times
- 1 Does not perform vertical interpolation

Bit25-24 CM (Capture Mode)
Sets video capture mode. To capture vides, set these bits to “11”.
- 00 Initial value
- 01 Reserved
- 10 Reserved
- 11 Capture

Bit28 VICE (Video Input Clock Enable)
Capture clock enable
- 0 Enable
- 1 Disable

Bit30 VIS (Video Input Select)
- 0 RBT656/601
- 1 RGB

Bit31 VIE (Video Input Enable)
Enables video capture function
- 0 Does not capture video
- 1 Captures video

- Procedure of video capture clock Stop

1) 0 is written in bit31 (VIE) of the VCM register, and the video capture function is invalidated.

2) 1 is written in bit28 (VICE) of the VCM register, and Stop does video capture clock.

- Procedure of video capture clock beginning

1) 0 is written in bit28 (VICE) of the VCM register, and video capture clock is made effective.

2) 1 is written in bit31 (VIE) of the VCM register, and the video capture function is made effective.

CSC (Capture SCale)

Register address	CaptureBaseAddress + 04h			
Bit number	31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8 7 6 5 4 3 2 1 0
Bit field name	VSCI	VSCF	HSCI	HSCF
R/W	R/W	R/W	R/W	R/W
Initial value	00001	00000000000	00001	00000000000

This register sets the video capture upscaling/downscaling ratio.

Bit10-0 HSCF (Vertical SCale Fraction)
The decimal part of a horizontal upscaling/downscaling ratio is set.

Bit15-11 HSCI (Horizontal Scale Integer)
The integer part of a horizontal upscaling/downscaling ratio is set.

Bit26-16 VSCF (Vertical SCale Fraction)
The decimal part of a vertical upscaling/downscaling ratio is set.

Bit31-27 VSCI (Vertical SCale Integer)
The integer part of a vertical upscaling/downscaling ratio is set.

Note:
It is not possible to smoothly transition from downscaling mode to upscaling mode. Picture artefacts will occur at transition time. The reason for this hardware limitation is that the downscaling and upscaling modules share the same interpolation unit.

CBM (video Capture Buffer Mode)

Register address	CaptureBaseAddress + 10h														
Bit number	31	30	29	28	27 … 24	23 22 … 17 16	15	14	13	12	11	10 9 8	7 6 5	4	3 2 1	0
Bit field name	OO	S-BUF	C-RGB	PAU	Reserve	CBW	resv	C24	BED	CSW	resv	SSS	SSM	HRV	reserve	C-BST
R/W	R/W	R/W	R/W	R/W	RX	R/W	RX	R/W	R/W	R/W	RX	R/W	R/W	R/W	RX	R/W
Initial value	0	X	X	0	X	X	X	0	0	0	X	000	000	0	X	0

Bit0 CBST (Capture Burst)
The burst-length at the capture Write is specified. Because long burst-length is good the access efficiency, 1 is recommended to be set.
0 Normal burst write (4word)
1 Long burst write (8word)

Bit4 HRV (H-reverse)
The horizontal reversing mode specification
0 Normal operation mode
1 Horizontal reversing mode

Bit7-5 SSM (Single Shot Mode)
Single shot mode
000 Normal operation mode
001 Single shot/odd field mode
010 Single shot/even field mode
011 Single shot/both field mode (with field distinction)
111 Single shot/both field mode2 (without field distinction)

Bit10-8 SSS (Single Shot Status)
The state of single shot operation is shown.
000 Initial state
001 Odd field mode / under capture
010 Even field mode / under capture
100 Both field mode / under first field capture
101 Both field mode / under second field capture

Bit12 CSW (Color Swap)
The byte position of a color ingredient is replaced.
0 Without exchange
1 With exchange

Bit13 BED (Big EnDian)
Endian is reversed
0 Little endian (enable display)
1 Big endian (disable display)

Bit14 C24 (Color 24bit/pixel)
It specifies wherther 24bit/pixel or 16bit/pixel is used in RGB capture.
It is effective in native RGB capture (NRGB=1) or converted RGB capture(CRGB=1).
0 16bit/pixel
1 24bit/pixel

Bit23-16 CBW (Capture Buffer memory Width)
Sets memory width (stride) of capture buffer in 64 bytes

Bit28 PAU (PAUse)
It is shown that capture operation is Stop temporarily. 0 can be written and it can cancel.
0 Under operation
1 Stop temporarily

Bit29 CRGB (Capture RGB write)
It specifies whether YCbCr to RGB conversion is applied or not before writing into the capture buffer. There are two formats of RGB or RGB=5:5:5 (16 bits/pixel) and RGB = 8:8:8 (24 bit/pixel) format, depending to C24-bit value described above.
0 YCbCr (without conversion)
1 RGB

Bit30 SBUF (Single Buffer)
It specifies managing a capture buffer by the single buffer system.
0 Normal mode (ring buffer)
1 Single buffer mode

Bit31 OO (Odd Only mode)
Specifies whether to capture odd fields only

0 Normal mode
1 Odd only mode

Note: This register is not initialized by software reset.

CBOA (video Capture Buffer Origin Address)

Register address	CaptureBaseAddress + 14h		
Bit number	31 - 30 - 29 - 28 - 27 - 26 - 25 - 24	23 - 22 - 21 - 20 - 19 - 18 - 17 - 16 - 15 - 14 - 13 - 12 - 11 - 10 - 9 - 8 - 7 - 6 - 5 - 4	3 - 2 - 1 - 0
Bit field name	Reserved	CBOA	
R/W	RX	R/W	R0
Initial value	Don't care	Don't care	0

This register specifies the starting (origin) address of the video capture buffer.

CBLA (video Capture Buffer Limit Address)

Register address	CaptureBaseAddress + 18h		
Bit number	31 - 30 - 29 - 28 - 27 - 26 - 25 - 24	23 - 22 - 21 - 20 - 19 - 18 - 17 - 16 - 15 - 14 - 13 - 12 - 11 - 10 - 9 - 8 - 7 - 6 - 5 - 4	3 - 2 - 1 - 0
Bit field name	Reserved	CBLA	
R/W	RX	R/W	R0
Initial value	Don't care	Don't care	0

This register specifies the end (limit) address of the video capture buffer.

CBLA must be larger than CBOA.

CIHSTR (Capture Image Horizontal STaRt)

Register address	CaptureBaseAddress + 1Ch															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				CIHSTR											
R/W	RX				R/W											
Initial value	Don't care				Don't care											

This register sets the range of the images to be written (captured) to the video capture buffer. Specify the X coordinates located in the top left of the image range as the count of pixels from the top left of the image. For downscaling, apply this setting to the post-reduction image coordinates.

CIVSTR (Capture Image Vertical STaRt)

Register address	CaptureBaseAddress + 1Eh															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				CIVSTR											
R/W	RX				R/W											
Initial value	Don't care				Don't care											

This register sets the range of the images to be written (captured) to the video capture buffer. Specify the Y coordinates located in the top left of the image range as the count of pixels from the top left of the image. For downscaling, apply this setting to the post-reduction image coordinates.

CIHEND (Capture Image Horizontal END)

Register address	CaptureBaseAddress + 20h															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				CIHEND											
R/W	RX				R/W											
Initial value	X				X											

This register sets the range of the images to be written (captured) to the video capture buffer. Specify the X coordinates located in the bottom right of the image range as the count of pixels from the top left of the image. For downscaling, apply this setting to the post-reduction image coordinates.

If the pixel at the right end of the image is not aligned on 64 bits/word boundary, extra data is written before 64 bits/word boundary.

If the width of the input image is less than the range set by this command, data is written only at the size of input image.

CIVEND (Capture Image Vertical END)

Register address	CaptureBaseAddress + 22h															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				CIVEND											
R/W	RX				R/W											
Initial value	X				X											

This register sets the range of the images to be written (captured) to the video capture buffer. Specify the Y coordinates located in the bottom right of the image range as the count of pixels from the top left of the original image to be input. For downscaling, apply this setting to the post-reduction image coordinates.

If the count of rasters of the input image is less than the range set by this command, data is written only at the size of the input image.

CVCNT (Capture Vertical Count)

Register address	CaptureBaseAddress + 300h															
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	Reserved				CVCNT											
R/W	R0				R											
Initial value	0				Don't care											

Y coordinates of the raster which is carrying out the capture are shown. The register is read-only.

CHP (Capture Horizontal Pixel)

Register address	CaptureBaseAddress + 28h	
Bit number	31 - 30 - 29 - 28 - 27 - 26 - 25 - 24 : 23 - 22 - 21 - 20 - 19 - 18 - 17 - 16 - 15 - 14 - 13 - 12 - 11 - 10	9 - 8 - 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
Bit field name	Reserved	CHP
R/W	RX	R/W
Initial value	X	0x168 (360)

This register sets the count of horizontal pixels of the image output after scaling. Specify the count of horizontal pixels in 2 pixels. Maximum is 840 pixels (setting value is 0x1A4)

CVP (Capture Vertical Pixel)

Register address	CaptureBaseAddress + $2c_H$			
Bit number	31 : 30 : 29 : 28 : 27 : 26	25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16	15 : 14 : 13 : 12 : 11 : 10	9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	Reserved	CVPP	Reserved	CVPN
R/W	RX	RW	RX	RW
Initial value	X	271_H (625_D)	X	$20D_H$ (525_D)

This register sets the count of vertical pixels of the image output after scaling. The fields to be used depend on the video format to be used.

Bit 25 to 16 CVPP (Capture Vertical Pixel for PAL)

Set count of vertical pixels of output image in PAL format used

Bit 9 to 0 CVPN (Capture Vertical Pixel for NTSC)

Set count of vertical pixels of output image in NTSC format used

CLPF (Capture Low Pass Filter)

Register address	CaptureBaseAddress + 40h				
Bit number	31 - 30 - 29 - 28	27 - 26	25 - 24 - 23 - 22 - 21 - 20	19 - 18 - 17 - 16	15 - 14 - 13 - 12 - 11 - 10 - 9 - 8 - 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
Bit field name	Reserved	CVLPF	Reserved	CHLPF	Reserved
R/W	RX	R/W	RX	R/W	RX
Initial value	0	0	0	0	X

This register sets the Low Pass Filter Coefficient. The vertical low pass filter consists of FIR filters of three taps. The horizontal low pass filter consists of FIR filters of five taps. It specifies independently in 2-bit coefficient code with a luminance signal (Y) and a chrominance signal (Cb and Cr) . A low pass filter is OFF (through) in a setup of each coefficient code “00”.

Bit 17 to 16 CHLPF_C (Capture Horizontal LPF coefficient C)

CHLPF_C	K0	K1	K2	K3	K4
00	0	0	1	0	0
01	0	1/4	2/4	1/4	0
10	0	3/16	10/16	3/16	0
11	3/32	8/32	10/32	10/32	3/32

Bit 19 to 18 CHLPF_Y (Capture Horizontal LPF coefficient Y)

CHLPF_Y	K0	K1	K2	K3	K4
00	0	0	1	0	0
01	0	1/4	2/4	1/4	0
10	0	3/16	10/16	3/16	0
11	3/32	8/32	10/32	10/32	3/32

Bit 25 to 24 CVLPF_C (Capture Vertical LPF coefficient C)

CVLPF_C	K0	K1	K2
00	0	1	0
01	1/4	2/4	1/4
10	3/16	10/16	3/16
11	Reserved		

Bit 27 to 26 CVLPF_Y (Capture Vertical LPF coefficient Y)

CVLPF_Y	K0	K1	K2
00	0	1	0
01	1/4	2/4	1/4
10	3/16	10/16	3/16
11	Reserved		

Note:

- In the case of Native RGB mode (NRGB=1), only a setup of CVLPF_Y code becomes effective.

CMSS (Capture Magnify Source Size)

Register address	CaptureBaseAddress + 48h			
Bit number	31 - 28	27 - 16	15 - 12	11 - 0
Bit field name	Reserved	CMSHP	Reserved	CMSVL
R/W	RX	R/W	RX	R/W
Initial value	X	X	X	X

Bit11-0 CMSVL (Capture Magnify Source Vertical Line)
This register sets the number of vertical lines of the image input before Magnify scaling.

Bit27-16 CMSHP (Capture Magnify Source Horizontal Pixel)
This register sets the number of horizontal pixels of the image input before Magnify scaling. Specify the number of horizontal pixels in 2-pixel units.

CMDS (Capture Magnify Display Size)

Register address	CaptureBaseAddress + 4Ch			
Bit number	31 - 28	27 - 16	15 - 12	11 - 0
Bit field name	Reserved	CMDHP	Reserved	CMDVL
R/W	RX	R/W	RX	R/W
Initial value	X	X	X	X

Bit11-0 CMDVL (Capture Magnify Display Vertical Line)
This register sets the number of vertical lines of the image output after Magnify scaling.

Bit27-16 CMDHP (Capture Magnify Display Horizontal Pixel)
This register sets the number of horizontal pixels of the image output after Magnify scaling. Specify the number of horizontal pixels in 2-pixel units.

RGBHC (RGB input Hsync Cycle)

Register address	CaptureBaseAddress + 80h	
Bit number	31 - 30 - 29 - 28 - 27 - 26 - 25 - 24 - 23 - 22 - 21 - 20 - 19 - 18 - 17 - 16 - 15 - 14	13 - 12 - 11 - 10 - 9 - 8 - 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
Bit field name	Reserved	RGBHC
R/W	RX	R/W
Initial value	X	X

Bit13-0 RGBHC
This register sets number of HSYNC cycles of the RGB input. . It is used when it is made a setup which samples VSYNC. The setting value +1 is a level cycle.

RGBHEN (RGB input Horizontal Enable area)

Register address	CaptureBaseAddress + 84h			
Bit number	31 - 30 - 29 - 28 - 27 - 26	25 - 24 - 23 - 22 - 21 - 20 - 19 - 18 - 17 - 16	15 - 14 - 13	12 - 11 - 10 - 9 - 8 - 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
Bit field name	Reserved	RGBHST	Reserved	RGBHEN
R/W	RX	R/W	RX	R/W
Initial value	X	X	X	X

It is a parameter for determining effective pixel data.

Bit12-0 RGBHEN(RGB input Horizontal Enable area Size)
Effective pixel data size is set up per pixel. Specify the number of horizontal pixels in 2-pixel units

Bit25-16 RGBHST(RGB input Horizontal Enable area Start position)
The start position of effective pixel data is set up. The setting value -4 is a start position.

Note:

- The maximum horizontal enable area size (RGBHEN) which can be captured is 840 pixels. This restriction is due to the line buffer size in the video capture module.

RGBVEN (RGB input Vertical Enable area)

Register address	CaptureBaseAddress + 88h					
Bit number	31 - 30	29 - 28	27 - 26	25 - 24 - 23 - 22 - 21 - 20 - 19 - 18 - 17 - 16	15 - 14 - 13	12 - 11 - 10 - 9 - 8 - 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
Bit field name	Reserved		Reserved	RGBVST	Reserved	RGBVEN
R/W	RX		R/W	R/W	RX	R/W
Initial value	X		X	X	X	X

This parameter determines the effective pixel data.

Bit12-0 RGBVEN(RGB input Vertical Enable area Size)
Set effective line size

Bit25-16 RGBVST(RGB input Vertical Enable area Start position)
The start position of effective line is set up. The setting value -1 is a start position.

RGBS (RGB input Sync)

Register address	CaptureBaseAddress + 90h				
Bit number	31 - 17	16	15 - 2	1	0
Bit field name	Reserved	RM	Reserved	HP	VP
R/W	RX	R/W	RX	R/W	R/W
Initial value	X	1	X	0	0

Edge detection of a synchronized signal is set up. It is used at the time of RGB input format.

Bit0 VP (VSYNCI Polarity)
- 0 Negative edge of VINVSYNC is set to VSYNC.
- 1 Positive edge of VINVSYNC is set to VSYNC.

Bit1 HP (HSYNCI Polarity)
- 0 Negative edge of VINHSYNC is set to HSYNC.
- 1 Positive edge of VINHSYNC is set to HSYNC.

Bit16 RM (RGB Input Mode select)
Sets Direct RGB input mode
- 0 reserved
- 1 RGB666 Direct input Mode

Conversion Operation

RGB data is converted to YUV by the following matrix expression :

Y = a11*R + a12*G + a13*B + b1
Cb= a21*R + a22*G + a23*B + b2 $\quad a_{ij}$ 10bit signed real (lower 8bit is fraction)
Cr= a31*R + a32*G + a33*B + b3 $\quad b_i$ 8bit unsigned integer

Each coefficients can be defined by following registers.
Cb and Cr components are reduced half after this operation to form the 4:2:2 format.

RGBCMY (RGB Color convert Matrix Y coefficient)

Register address	CaptureBaseAddress + $C0_H$				
Bit number	31 30 29 28 27 26 25 24 23 22	21	20 19 18 17 16 15 14 13 12 11	10	9 8 7 6 5 4 3 2 1 0
Bit field name	a11	Re	a12	Re	a13
R/W	RW	R	RW	R	RW
Initial value	0001000010_b	0	0010000000_b	0	0000011001_b

This register sets the RGB color convert matrix coefficient.

Bit 31 to 22 a11
10bit signed real (the lower 8bit are the fraction part)

Bit 20 to 11 a12
10bit signed real (the lower 8bit are the fraction part)

Bit 9 to 0 a13
10bit signed real (the lower 8bit are the fraction part)

RGBCMCb (RGB Color convert Matrix Cb coefficient)

Register address	CaptureBaseAddress + $C4_H$				
Bit number	31 30 29 28 27 26 25 24 23 22	21	20 19 18 17 16 15 14 13 12 11	10	9 8 7 6 5 4 3 2 1 0
Bit field name	a21	Re	a22	Re	a23
R/W	RW	R	RW	R	RW
Initial value	1111011010_b	0	1110110110_b	0	0001110000_b

This register sets the RGB color convert matrix coefficient.

Bit 31 to 22 A21
10bit signed real (the lower 8bit are the fraction part)

Bit 20 to 11 A22
10bit signed real (the lower 8bit are the fraction part)

Bit 9 to 0 A23
10bit signed real (the lower 8bit are the fraction part)

RGBCMCr (RGB Color convert Matrix Cr coefficient)

Register address	CaptureBaseAddress + $C8_H$

Bit number	31 30 29 28 27 26 25 24 23 22	21	20 19 18 17 16 15 14 13 12 11	10	9 8 7 6 5 4 3 2 1 0
Bit field name	A31	Re	A32	Re	A33
R/W	RW	R	RW	R	RW
Initial value	0001110000 b	0	1110100010 b	0	1111101110 b

This register sets the RGB color convert matrix coefficient.

Bit 31 to 22 A31

10bit signed real (the lower 8bit are the fraction part)

Bit 20 to 11 A32

10bit signed real (the lower 8bit are the fraction part)

Bit 9 to 0 A33

10bit signed real (the lower 8bit are the fraction part)

RGBCMb (RGB Color convert Matrix b coefficient)

Register address	CaptureBaseAddress + CC_H					
Bit number	31	30 29 28 27 26 25 24 23 22	21 20	19 18 17 16 15 14 13 12 11	10 9	8 7 6 5 4 3 2 1 0
Bit field name	R	B1	Res	b2	Res	b3
R/W	R	RW	R	RW	R	RW
Initial value	0	000010000 b	0	010000000 b	0	010000000 b

This register sets the RGB color convert matrix coefficient.

Bit 30 to 22 B1

9bit unsigned integer

Bit 19 to 11 B2

9bit unsigned integer

Bit 8 to 0 B3

9bit unsigned integer

CINT (Capture Interrupt)

Register address	CaputureBaseAddress + 178_H		
Bit No.	31 30 29 28 27 26 .. .. .. 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
Bit field name	Reserved	VS	
R/W	R	RW0	
Initial value	0	0	

This register is the video synchronization signal interrupt status register. This register is cleared by writing “0” to it.

Bit 1 VS (VSYNC)

1: VSYNC 0: No VSYNC

CINTMASK (Capture Interrupt Mask)

Register address	CaputureBaseAddress + $17C_H$		
Bit No.	31 30 29 28 27 26 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0

Bit field name	Reserved	VS	
R/W	R	RW	
Initial value	0	0	

This register masks the video synchronization signal interrupt

Bit 1 VS (VSYNC)

1: Does not mask interrupt. 0: Masks interrupt.

【656 Code error detect】

< RBT656 format input only>

CDCN (Capture Data Count for NTSC)

Register address	CaptureBaseAddress + 4000h			
Bit number	31 - 30 - 29	28 - 27 - 26 - 25 - 24 - 23 - 22 - 21 - 20 - 19 - 18 - 17 - 16	15 - 14 - 13	12 - 11 - 10 - 9 - 8 - 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
Bit field name	Reserved	BDCN	Reserved	VDCN
R/W	RX	RW	RX	RW
Initial value	X	0x10f(271)	X	0x5A3(1443)

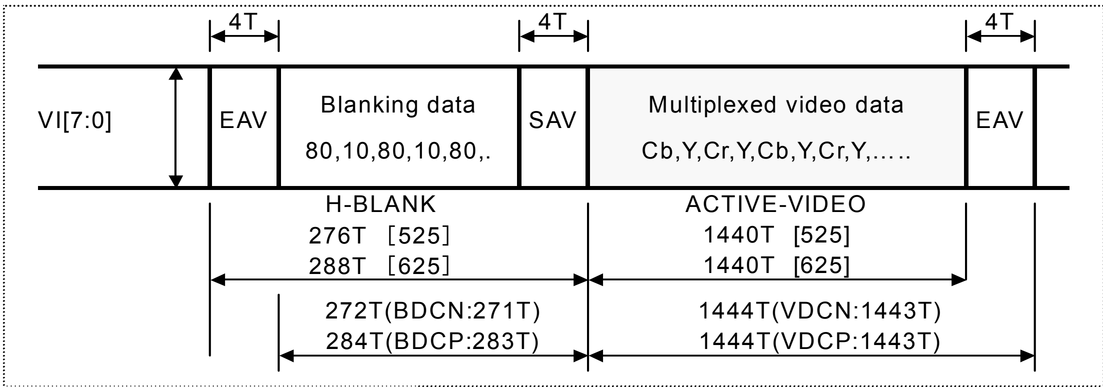
This register sets the count of data of the input video stream in NTSC format.

Bit12-0 VDCN (Valid Data Count for NTSC)

Sets count of data processed during valid period in NTSC format. The setting value +1 is a data number

Bit28-16 BDCN (Blanking Data Count for NTSC)

Sets count of data processed during blanking period in NTSC format. The setting value +1 is a data number



The range of VDCN and BDCN is shown in the following figure.

SAV: start of active video timing reference code

EAV: end of active video timing reference code

T: clock period 37 ns nom.

CDCP (Capture Data Count for PAL)

Register address	CaptureBaseAddress + 4004h			
Bit number	31 - 30 - 29	28 - 27 - 26 - 25 - 24 - 23 - 22 - 21 - 20 - 19 - 18 - 17 - 16	15 - 14 - 13	12 - 11 - 10 - 9 - 8 - 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
Bit field name	Reserved	BDCP	Reserved	VDCP
R/W	RX	RW	RX	RW
Initial value	X	0x11B(283)	X	0x5A3(1443)

This register sets the count of data of the input video stream in PAL format.

Bit12-0 VDCP (Valid Data Count for PAL)
Sets count of data processed during valid period in PAL format. The setting value +1 is a data number

Bit28-16 BDCP (Blanking Data Count for PAL)
Sets count of data processed during blanking period in PAL format. The setting value +1 is a data number

VCS (Video Capture Status)

Register address	CaptureBaseAddress + 08h	
Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5	4 3 2 1 0
Bit field name	Reserve	CE
R/W	RX	RW0
Initial value	X	00000

This register indicates the ITU-RBT656 SAV and EAV status.

To detect error codes, set NTSC/PAL in the VS bit of VCM. If NTSC is set, reference the number of data in the capture data count register (CDCN). If PAL is set, reference the number of data in the capture data counter register (CDCP). If the reference data does not match the stream data , or undefined Fourth word of SAV/EAV codes are detected, bits 4 to 0 of the video capture status register (VCS) will be values as follows.

Bits 6-0 CE0 (Capture Error 0)

Bit0	1 : RBT.656 undefined error (Code Bit7)	0 : true
Bit1	1 : RBT.656 undefined error (Code Bit7-4)	0 : true
Bit2	1 : RBT.656 undefined error (Code Bit7-0)	0 : true
Bit3	1 : RBT.656 long term H code error (SAV)	0 : true
Bit4	1 : RBT.656 long term H code error (EAV)	0 : true

12.5 Drawing registers

12.5.1 Drawing control registers

CTR (Control Register)

Register address	DrawBaseAddress + 400_H														
Bit number	31 30 29 28 27 26 25	24	23	22	21	20 19 18 17 16 15	14	13	12	11 10	9 8	7 6	5 4	3 2	1 0
Bit field name		FO		CE		FCNT	NF	FF	FE		SS		DS		PS
R/W		RW		RW		R	R	R	R		R		R		R
Initial value		0		0		011101	0	0	1		00		00		00

This register indicates drawing flags and status information. Bits 24 to 22 are not cleared until 0 is set.

Bit 1 and 0 PS (Pixel engine Status)

Indicate status of pixel engine unit

00 Idle

01 Busy

10 Reserved

11 Reserved

Bit 5 and 4 DS (DDA Status)

Indicate status of DDA

00 Idle

01 Busy

10 Busy

11 Reserved

Bit 9 and 8 SS (Setup Status)

Indicate status of Setup unit

00 Idle

01 Busy

10 Reserved

11 Reserved

Bit 12 FE (FIFO Empty)

Indicates whether data contained or not in display list FIFO

0 Valid data

1 No valid data

Bit 13 FF (FIFO Full)

Indicates whether display list FIFO is full or not

0 Not full

1 Full

Bit 14 NF (FIFO Near Full)

Indicates how empty the display list FIFO is

0 Empty entries equal to or more than half

1 Empty entries less than half

Bit 20 to 15 FCNT (FIFO Counter)

Indicates count of empty entries of display list FIFO (0 to 100000_b) 32 entries deep

Bit 22-23 CE (Display List Command Error)

Indicates command error occurrence (Not all error can detect. Need software reset or hardware reset for recovery)

00 Normal

11 Command error detected

Bit 24 FO (FIFO Overflow)

Indicates FIFO overflow occurrence

0 Normal

1 FIFO overflow detected

IFSR (Input FIFO Status Register)

Register address	DrawBaseAddress + 404_H			
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3	2	1	0
Bit field name		NF	FF	FE
R/W		R	R	R
Initial value		0	0	1

This is a mirror register for bits 14 to 12 of the CTR register.

IFCNT (Input FIFO Counter)

Register address	DrawBaseAddress + 408_H	
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6	5 : 4 : 3 : 2 : 1 : 0
Bit field name		FCNT
R/W		R
Initial value		011101

This is a mirror register for bits 20 to 15 of the CTR register.

SST (Setup engine Status)

Register address	DrawBaseAddress + $40C_H$	
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2	1 : 0
Bit field name		SS
R/W		R
Initial value		00

This is a mirror register for bits 9 to 8 of the CTR register.

DST (DDA Status)

Register address	DrawBaseAddress + 410_H	
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2	1 : 0
Bit field name		DS
R/W		RW
Initial value		00

This is a mirror register for bits 5 to 4 of the CTR register.

PST (Pixel engine Status)

Register address	DrawBaseAddress + 414_H	
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2	1 : 0
Bit field name		PS
R/W		R
Initial value		00

This is a mirror register for bits 1 to 0 of the CTR register.

EST (Error Status)

Register address	DrawBaseAddress + 418_H		
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3	2	1 | 0
Bit field name		FO	CE
R/W		RW	RW
Initial value		0	0

This is a mirror register for bits 24 to 22 of the CTR register.

12.5.2 Drawing mode registers

When write to the registers, use the ***SetRegister*** command. The registers cannot be accessed from the CPU.

MDR0 (Mode Register for miscellaneous)

Register address	DrawBaseAddress + 420_H									
Bit number	31 30 29 28 27 26 25 24 23 22 21	20	19 18 17	16 15	14 13 12 11 10	9	8	7 6 5 4	3 2	1 0
Bit field name		ZP		CF		CY	CX		BSV	BSH
R/W	W0	RW	W0	RW	W0	RW	RW	W0	RW	RW
Initial value		0		00		0	0		00	00

Bit 1 to 0 BSH (Bitmap Scale Horizontal)

Sets horizontal zoom ratio of bitmap draw

00 x1

01 x2

10 x1/2

01 Reserved

Bit 3 to 2 BSV (Bitmap Scale Vertical)

Sets vertical zoom ratio of bitmap draw

00 x1

01 x2

10 x1/2

01 Reserved

Bit 8 CX (Clip X enable)

Sets X coordinates clipping mode

0 Disabled

1 Enabled

Bit 9 CY (Clip Y enable)

Sets Y coordinates clipping mode

0 Disabled

1 Enabled

Bit 16 and 15 CF (Color Format)

Sets drawing color format

00 Indirect color mode (8 bits/pixel)

01 Direct color mode (16 bits/pixel)

Bit 20 ZP (Z Precision)

Sets the precision of the Z value used for erasing hidden planes

16 bits/pixel

8 bits/pixel

MDR1 (Mode Register for LINE)

Register address	DrawBaseAddress + 424_H												
Bit number	31 30 29	28 27 26 25 24	23 22 21	20	19	18 17 16 15 14 13	12 11 10 9	8 7	6	5 4 3	2	1	0
Bit field name		LW		BP	BL		LOG	BM	ZW	ZCL	ZC		
R/W		RW		RW	RW		RW	RW	RW	RW	RW		
Initial value		00000		0	0		0011	0	0	0000	0		

This register sets the mode of line and pixel drawing.

Please set ZC bit (bit 2) to 0 when draw BltCopyAltAlphaBlendP command.

Bit 2 ZC (Z Compare mode)

Sets Z comparison mode

0 Disabled

1 Enabled

Bit 5 to 3 ZCL (Z Compare Logic)

Selects type of Z comparison

000 NEVER

001 ALWAYS

010 LESS

011 LEQUAL

100 EQUAL

101 GEQUAL

110 GREATER

111 NOTEQUAL

Bit 6 ZW (Z Write mode)

Sets Z write mode

0 Writes Z values.

1 Not write Z values.

Bit 8 to 7 BM (Blend Mode)

Sets blend mode

00 Normal (source copy)

01 Alpha blending

10 Drawing with logic operation

11 Reserved

Bit 12 to 9 LOG (Logical operation)

Sets type of logic operation

0000 CLEAR

0001 AND

0010 AND REVERSE

0011 COPY

0100 AND INVERTED

0101	NOP
0110	XOR
0111	OR
1000	NOR
1001	EQUIV
1010	INVERT
1011	OR REVERSE
1100	COPY INVERTED
1101	OR INVERTED
1110	NAND
1111	SET

Bit 19 BL (Broken Line)

Selects line type

0	Solid line
1	Broken line

Bit 20 BP (Broken line Period)

Selects broken line cycle

0:	32 bits
1:	24 bits

Bit 28 to 24 LW (Line Width)

Sets line width for drawing line

00000	1 pixel
00001	2 pixels
:	:
11111	32 pixels

MDR2 (Mode Register for Polygon)

Register address	DrawBaseAddress + 428_H									
Bit number	31 30	29 28	27 26 25 24 23 22 21 20 19 18 17 16 15 14 13	12 11 10 9	8 7	6	5 4 3	2	1	0
Bit field name		TT		LOG	BM	ZW	ZCL	ZC		SM
R/W	W0	RW		RW	RW	RW	RW	RW		RW
Initial value		00		0011	0	0	0000	0		0

This register sets the polygon drawing mode.

Bit 0 SM (Shading Mode)

Sets shading mode

0 Flat shading

1 Gouraud shading

Bit 2 ZC (Z Compare mode)

Sets Z comparison mode

0 Disabled

1 Enabled

Bit 5 to 3 ZCL (Z Compare Logic)

Selects type of Z comparison

000 NEVER

001 ALWAYS

010 LESS

011 LEQUAL

100 EQUAL

101 GEQUAL

110 GREATER

111 NOTEQUAL

Bit 6 ZW (Z Write mask)

Sets Z write mode

0 Writes Z values

1 Not write Z values

Bit 8 to 7 BM (Blend Mode)

Sets blend mode

00 Normal (source copy)

01 Alpha blending

10 Drawing with logic operation

11 Reserved

Bit 12 to 9 LOG (Logical operation)

Sets type of logic operation

0000	CLEAR
0001	AND
0010	AND REVERSE
0011	COPY
0100	AND INVERTED
0101	NOP
0110	XOR
0111	OR
1000	NOR
1001	EQUIV
1010	INVERT
1011	OR REVERSE
1100	COPY INVERTED
1101	OR INVERTED
1110	NAND
1111	SET

Bit 29 to 28 TT (Texture-Tile Select)

Selects texture or tile pattern

00	Neither used
01	Enabled tiling
10	Enabled texture
11	Reserved

MDR3 (Mode Register for Texture)

Register address	DrawBaseAddress + $42C_H$											
Bit number	31 30 29 28 27 26 25 24 23 22	21 20	19 18	17 16	15 14 13 12	11 10	9 8	7 6	5	4	3	2 1 0
Bit field name		TAB		TBL		TWS	TWT		TF		TC	
R/W		RW		RW		RW	RW		RW		RW	
Initial value		00		00		00	00		0		0	

This register sets the texture mapping mode.

Bit 3 TC (Texture coordinates Correct)

Sets texture coordinates correction mode

0 Disabled

1 Reserved

Bit 5 TF (Texture Filtering)

Sets type of texture interpolation (filtering)

0 Point sampling

1 Bi-linear filtering

Bit 9 and 8 TWT (Texture Wrap T)

Sets type of texture coordinates T direction wrapping

00 Clamp

01 Repeat

10 Border

11 Reserved

Bit 11 and 10 TWS (Texture Wrap S)

Sets type of texture coordinates S direction wrapping

00 Clamp

01 Repeat

10 Border

11 Reserved

Bit 17 and 16 TBL (Texture Blend mode)

Sets texture blending mode

00 De-curl

01 Modulate

10 Stencil

11 Reserved

Bit 21 and 20 TAB (Texture Alpha Blend mode)

Sets texture blending mode

The stencil mode and the stencil alpha mode are enabled only when the MDR2 register blend mode (BM) is set to the alpha blending mode. If it is not set to the alpha blending mode, the stencil mode and stencil alpha mode perform the same function as the normal mode.

00	Normal
01	Stencil
10	Stencil alpha
11	Reserved

MDR4 (Mode Register for BLT)

Register address	DrawBaseAddress + 430_H					
Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13	12 11 10 9	8 7	6 5 4 3 2	1	0
Bit field name		LOG	BM		TE	
R/W		RW	RW		RW	
Initial value		0011	00		0	

This register controls the BLT mode.

Bit 1 TE (Transparent Enable)

Sets transparent mode

0: Not perform transparent processing

1: Not draw pixels that corresponds to set transparent color in BLT (transparancy copy)
Note: Set the blend mode (BM) to normal.

Bit 8 to 7 BM (Blend Mode)

Sets blend mode

00	Normal (source copy)
01	Reserved
10	Drawing with logic operation
11	Reserved

Bit 12 to 9 LOG (Logical operation)

Sets logic operation

0000	CLEAR
0001	AND
0010	AND REVERSE
0011	COPY
0100	AND INVERTED
0101	NOP
0110	XOR
0111	OR
1000	NOR
1001	EQUIV
1010	INVERT
1011	OR REVERSE
1100	COPY INVERTED
1101	OR INVERTED
1110	NAND
1111	SET

FBR (Frame buffer Base)

Register address	DrawBaseAddress + 440_H		
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Bit field name		FBASE	
R/W		RW	R0
Initial value		Don't care	0

This register stores the base address of the drawing frame.

XRES (X Resolution)

Register address	DrawBaseAddress + 444_H	
Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Bit field name		XRES
R/W		RW
Initial value		Don't care

This register sets the drawing frame horizontal resolution.

ZBR (Z buffer Base)

Register address	DrawBaseAddress + 448_H		
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Bit field name		ZBASE	
R/W		RW	R0
Initial value		Don't care	0

This register sets the Z buffer base address.

TBR (Texture memory Base)

Register address	DrawBaseAddress + $44C_H$		
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Bit field name		TBASE	
R/W		RW	R0
Initial value		Don't care	0

This register sets the texture memory base address.

PFBR (2D Polygon Flag-Buffer Base)

Register address	DrawBaseAddress + 450_H		
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Bit field name		PFBASE	
R/W		RW	R0
Initial value		Don't care	0

This register sets the polygon flag buffer base address.

CXMIN (Clip X minimum)

Register address	DrawBaseAddress + 454_H	
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12	11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name		CLIPXMIN
R/W		RW
Initial value		Don't care

This register sets the clip frame minimum X position.

CXMAX (Clip X maximum)

Register address	DrawBaseAddress + 458_H	
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12	11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name		CLIPXMAX
R/W		RW
Initial value		Don't care

This register sets the clip frame maximum X position.

CYMIN (Clip Y minimum)

Register address	DrawBaseAddress + $45C_H$	
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12	11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name		CLIPYMIN
R/W		RW
Initial value		Don't care

This register sets the clip frame minimum Y position.

CYMAX (Clip Y maximum)

Register address	DrawBaseAddress + 460_H	
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12	11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name		CLIPYMAX
R/W		RW
Initial value		Don't care

This register sets the clip frame maximum Y position.

TXS (Texture Size)

Register address	DrawBaseAddress + 464_H			
Bit number	31 30 29	28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
Bit field name		TXSN		TXSM
R/W		RW		RW
Initial value		000010000000		000010000000

This register specifies the texture size (m, n).

Bit 12 to 0 TXSM (Texture Size M)

Sets horizontal texture size. Any power of 2 between 4 and 4096 can be used. Values that are not a power of 2 cannot be used.

0_0000_0000_0100	M=4	0_0010_0000_0000	M=512
0_0000_0000_1000	M=8	0_0100_0000_0000	M=1024
0_0000_0001_0000	M=16	0_1000_0000_0000	M=2048
0_0000_0010_0000	M=32	1_0000_0000_0000	M=4096
0_0000_0100_0000	M=64		
0_0000_1000_0000	M=128		
0_0001_0000_0000	M=256	Other than the above	Setting disabled

Bit 28 to 16 TXSN (Texture Size N)

Sets vertical texture size. Any power of 2 between 4 and 4096 can be used. Values that are not a power of 2 cannot be used.

0_0000_0000_0100	N=4	0_0010_0000_0000	N=512
0_0000_0000_1000	N=8	0_0100_0000_0000	N=1024
0_0000_0001_0000	N=16	0_1000_0000_0000	N=2048
0_0000_0010_0000	N=32	1_0000_0000_0000	N=4096
0_0000_0100_0000	N=64		
0_0000_1000_0000	N=128		
0_0001_0000_0000	N=256	Other than the above	Setting disabled

TIS (Tile Size)

Register address	DrawBaseAddress + 468_H			
Bit number	31 30 29 28 27 26 25 24 23	22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7	6 5 4 3 2 1 0
Bit field name		TISN		TISM
R/W		RW		RW
Initial value		1000000		1000000

This register specifies the tile size (m, n).

Bit 6 to 0 TISM (Title Size M)

Sets horizontal tile size. Any power of 2 between 4 and 64 can be used. Values that are not a power of 2 cannot be used.

0.000100	M=4
0001000	M=8
0010000	M=16
0100000	M=32
1000000	M=64
Other than the above	Setting disabled

Bit 22 to 16 TISN (Title Size N)

Sets vertical tile size. Any power of 2 between 4 and 64 can be used. Values that are not a power of 2 cannot be used.

0000100	N=4
0001000	N=8
0010000	N=16
0100000	N=32
1000000	N=64
Other than the above	Setting disabled

TOA (Texture Buffer Offset address)

Register address	DrawBaseAddress + $46C_H$	
Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
Bit field name		XBO
R/W		RW
Initial value		Don't care

This register sets the texture buffer offset address. Using this offset value, texture patterns can be referred to the texture buffer memory.

Specify the word-aligned byte address (16 bits). (Bit 0 is always “0”.)

ABR (Alpha map Base)

Register address	DrawBaseAddress + 474_H		
Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5 4 3 2 1 0
Bit field name		ABASE	
R/W		RW	R0
Initial value		Don't care	0

This register sets the base address of the alpha map.

FC (Foreground Color)

Register address	DrawBaseAddress + 480_H	
Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Bit field name		FGC
R/W		RW
Initial value		0

This register sets the drawing foreground color. This color is for the object color for flat shading and foreground color for bitmap drawing and broken line drawing. All bits set to "1" are drawn in the color set at this register.

8 bit color mode:

Bit 7 to 0 FGC8 (Foreground 8 bit Color)

Sets the indirect color for the foreground (color index code).

Bit 31 to 8 These bits are not used.

16 bit color mode:

Bit 15 to 0 FGC16 (Foreground 16 bit Color)

This field sets the 16-bit direct color for the foreground.
Note that the handling of bit 15 is different from that in ORCHID.
Up to ORCHID, bit 15 is "0" for other than bit map and rectangular drawing, but starting with LIME GDC, the setting value is reflected in memory as is. This bit is also reflected in bit 15 of the 16-bit color at Gouraud shading.

Bit 31 to 16 These bits are not used.

BC (Background Color)

Register address	DrawBaseAddress + 484_H
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 | 15 | 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	BGC8/16
R/W	RW
Initial value	0

This register sets the drawing frame background color. This color is used for the background color of bitmap drawing and broken line drawing. At bitmap drawing, all bits set to "0" are drawn in the color set at this register.

BT bit of this register allows the background color of be transparent (no drawing).

8 bit color mode:

- Bit 7 to 0 BGC8 (Background 8 bit Color)
  Sets the indirect color for the background (color index code)
- Bit 14 to 8 Not used
- Bit 15 BT (Background Transparency)
  Sets the transparent mode for the background color
  - 0 Background drawn using color set for BGC field
  - 1 Background not drawn (transparent)
- Bit 31 to 16 Not used

16 bit color mode:

- Bit 14 to 0 BGC16 (Background 16 bit Color)
  Sets 16-bit direct color (RGB) for the background
- Bit 15 BT (Background Transparency)
  Sets the transparent mode for the background color
  - 0 Background drawn using color set for BGC field
  - 1 Background not drawn (transparent)
- Bit 31 to 16 Not used

ALF (Alpha Factor)

Register address	DrawBaseAddress + 488_H	
Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Bit field name		A
R/W		RW
Initial value		0

This register sets the alpha blending coefficient.

BLP (Broken Line Pattern)

Register address	DrawBaseAddress + $48C_H$
Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	BLP
R/W	RW
Initial value	0

This register sets the broken-line pattern. The bit 1 set in the broken-line pattern is drawn in the foreground color and bit 0 is drawn in the background color. The line pattern for 1 pixel line is laid out in the direction of MSB to LSB and when it reaches LSB, it goes back to MSB. The BLPO register manages the bit numbers of the broken-line pattern. 32 or 24 bits can be selected as the repetition of the broken-line pattern by the BP bit of the MDR1 register. When 24 bits are selected, bits 23 to 0 of the BLP register are used.

TBC (Texture Border Color)

Register address	DrawBaseAddress + 494_H		
Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Bit field name	BC8/16		
R/W	RW		
Initial value	0		

This register sets the border color for texture mapping.

8 bit color mode:

Bit 7 to 0 BC8 (Border Color)
Sets the 8-bit direct color for the texture border color

16 bit color mode:

Bit 15 to 0 BC16 (Border Color)
Sets the 16-bit direct color for the texture border color
Bit15 is used for controlling a stencil and stencil alpha

BLPO (Broken Line Pattern Offset)

Register address	DrawBaseAddress + $3E0_H$	
Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5	4 3 2 1 0
Bit field name		BCR
R/W		RW
Initial value		11111

This register stores the bit number of the broken-line pattern set to BLP registers, for broken line drawing. This value is decremented at each pixel drawing. Broken line can be drawn starting from any starting position of the specified broken-line pattern by setting any value at this register.

When no write is performed, the position of broken-line pattern is sustained.

12.5.3 Triangle drawing registers

Each register is used by the drawing commands. The registers cannot be accessed from the CPU or using the ***SetRegister*** command.

(XY coordinates register)

Register	Address	31	30	29	28	27:26:25:24:23:22:21:20:19:18:17:16	15:14:13:12:11:10:9:8:7:6:5:4:3:2:1:0
Ys	0000_H	S	S	S	S	Int	Frac
Xs	0004_H	S	S	S	S	Int	Frac
dXdy	0008_H	S	S	S	S	Int	Frac
XUs	$000c_H$	S	S	S	S	Int	Frac
dXUdy	0010_H	S	S	S	S	Int	Frac
XLs	0014_H	S	S	S	S	Int	Frac
dXLdy	0018_H	S	S	S	S	Int	Frac
USN	$001b_H$	0	0	0	0	Int	0
LSN	0020_H	0	0	0	0	Int	0

Address Offset value from DrawBaseAddress
S Sign bit or sign extension
0 Not used or 0 extension
Int Integer or integer part of fixed point data
Frac Fraction part of fixed point data

Sets (X, Y) coordinates for triangle drawing

Ys	Y coordinates start position of long edge
Xs	X coordinates start position of long edge corresponding to Ys
dXdy	X DDA value of long edge direction
XUs	X coordinates start position of upper edge
dXUdy	X DDA value of upper edge direction
XLs	X coordinates start position of lower edge
dXLdy	X DDA value of lower edge direction
USN	Count of spans of upper triangle. If this value is “0”, the upper triangle is not drawn.
LSN	Count of spans of lower triangle. If this value is “0”, the lower triangle is not drawn.

(Color setting register)

Register	Address	31	30	29	28	27	26	25	24	23–16	15–0
Rs	0040_H	0	0	0	0	0	0	0	0	Int	Frac
dRdx	0044_H	S	S	S	S	S	S	S	S	Int	Frac
dRdy	0048_H	S	S	S	S	S	S	S	S	Int	Frac
Gs	$004C_H$	0	0	0	0	0	0	0	0	Int	Frac
dGdx	0050_H	S	S	S	S	S	S	S	S	Int	Frac
dGdy	0054_H	S	S	S	S	S	S	S	S	Int	Frac
Bs	0058_H	0	0	0	0	0	0	0	0	Int	Frac
dBdx	$005c_H$	S	S	S	S	S	S	S	S	Int	Frac
dBdy	0060_H	S	S	S	S	S	S	S	S	Int	Frac
As	0064_H	0	0	0	0	0	0	0	0	Int	Frac
dAdx	0068_H	S	S	S	S	S	S	S	S	Int	Frac
dAdy	$006c_H$	S	S	S	S	S	S	S	S	Int	Frac

Address Offset from DrawBaseAddress
S Sign bit or sign extension
0 Not used or 0 extension
Int Integer or integer part of fixed point data
Frac Fraction part of fixed point data

Sets color parameters for triangle drawing. These parameters are enabled in the Gouraud shading mode.

Rs	R value at (Xs, Ys, Zs) of long edge corresponding to Ys
dRdx	R DDA value of horizontal direction
dRdy	R DDA value of long edge
Gs	G value at (Xs, Ys, Zs) of long edge corresponding to Ys
dGdx	G DDA value of horizontal direction
dGdy	G DDA value of long edge
Bs	B value at (Xs, Ys, Zs) of long edge corresponding to Ys
dBdx	B DDA value of horizontal direction
dBdy	B DDA value of long edge
As	Alpha value at (Xs, Ys, Zs) of long edge corresponding to Ys
dAdx	Alpha DDA value of horizontal direction
dAdy	Alpha DDA value of long edge

(Z coordinates register)

Register	Address	31	30–15	14–0
Zs	0080h	0	Int	Frac
dZdx	0084h	S	Int	Frac
dZdy	008ch	S	Int	Frac

Address Offset from DrawBaseAddress
S Sign bit or sign extension
0 Not used or 0 extension
Int Integer or integer part of fixed point data
Frac Fraction part of fixed point data

Sets Z coordinates for 3D triangle drawing

Zs	Z coordinate start position of long edge
dZdx	Z DDA value of horizontal direction
dZdy	Z DDA value of long edge

(Texture coordinates-setting register)

Register	Address	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ss	00c0$_H$	S	S	S	Int													Frac															
dSdx	00c4$_H$	S	S	S	Int													Frac															
dSdy	00c8$_H$	S	S	S	Int													Frac															
Ts	00cc$_H$	S	S	S	Int													Frac															
dTdx	00d0$_H$	S	S	S	Int													Frac															
dTdy	00d4$_H$	S	S	S	Int													Frac															
Qs	00d8$_H$	0	0	0	0	0	0	0	Int	Frac																							
dQdx	00dc$_H$	S	S	S	S	S	S	S	Int	Frac																							
dQdy	00e0$_H$	S	S	S	S	S	S	S	Int	Frac																							

Address	Offset from DrawBaseAddress
S	Sign bit or sign extension
0	Not used or 0 extension
Int	Integer or integer part of fixed point data
Frac	Fraction part of fixed point data

Sets texture coordinates parameters for triangle drawing

Ss	S texture coordinates (Xs, Ys, Zs) of long edge corresponding to Ys
dSdx	S DDA value of horizontal direction
dSdy	S DDA value of long edge direction
Ts	T texture coordinates (Xs, Ys, Zs) of long edge corresponding to Ys
dTdx	T DDA value of horizontal direction
dTdy	T DDA value of long edge direction
Qs	Q (Perspective correction value) of texture at (Xs, Ys, Zs) of long edge corresponding to Ys
dQdx	Q DDA value of horizontal direction
dQdy	Q DDA value of long edge direction

12.5.4 Line drawing registers

Each register is used by the drawing commands. The registers cannot be accessed from the CPU or by using the ***SetRegister*** command.

(Coordinates setting register)

<table>
<tr><th>Register</th><th>Address</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>LPN</td><td>0140_H</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td>LXs</td><td>0144_H</td><td>S</td><td>S</td><td>S</td><td>S</td><td colspan="12">Int</td><td colspan="16">Frac</td></tr>
<tr><td>LXde</td><td>0148_H</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>Int</td><td colspan="16">Frac</td></tr>
<tr><td>LYs</td><td>014c_H</td><td>S</td><td>S</td><td>S</td><td>S</td><td colspan="12">Int</td><td colspan="16">Frac</td></tr>
<tr><td>LYde</td><td>0150_H</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>Int</td><td colspan="16">Frac</td></tr>
<tr><td>LZs</td><td>0154_H</td><td>S</td><td colspan="16">Int</td><td colspan="15">Frac</td></tr>
<tr><td>LZde</td><td>0158_H</td><td>S</td><td colspan="16">Int</td><td colspan="15">Frac</td></tr>
</table>

Address	Offset from DrawBaseAddress
S	Sign bit or sign extension
0	Not used or 0 extension
Int	Integer or integer part of fixed point data
Frac	Fraction part of fixed point data

Sets coordinates parameters for line drawing

LPN	Pixel count of principal axis direction
LXs	X coordinates start position of draw line (In principal axis X) Integer value of X coordinates rounded off (In principal axis Y) X coordinates in form of fixed point data
LXde	Inclination data for X coordinates (In principal axis X) Increment or decrement according to drawing direction (In principal axis Y) Fraction part of DX/DY
LYs	Y coordinates start position of draw line (In principal axis X) Y coordinates in form of fixed point data (In principal axis Y) Integer value of Y coordinates rounded off
LYde	Inclination data for Y coordinates (In principal axis X) Fraction part of DY/DX (In principal axis Y) Increment or decrement according to drawing direction
LZs	Z coordinates start position of line drawing line
LZde	Z Inclination

12.5.5 Pixel drawing registers

Each register is used by the drawing commands. The registers cannot be accessed from the CPU or using the ***SetRegister*** command.

<table>
<tr><th>Register</th><th>Address</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>PXdc</td><td>0180_H</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td>PYdc</td><td>0184_H</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td>PZdc</td><td>0188_H</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
</table>

Address Offset from DrawBaseAddress
S Sign bit or sign extension
0 Not used or 0 extension
Int Integer or integer part of fixed point data
Frac Fraction part of fixed point data

Sets coordinates parameter for drawing pixel. The foreground color is used.

PXdc	Sets X coordinates position
PYdc	Sets Y coordinates position
PZdc	Sets Z coordinates position

12.5.6 Rectangle drawing registers

Each register is used by the drawing commands. The registers cannot be accessed from the CPU or using the ***SetRegister*** command.

<table>
<tr><th>Register</th><th>Address</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>RXs</td><td>0200_H</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td>Rys</td><td>0204_H</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td>RsizeX</td><td>0208_H</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td>RsizeY</td><td>$020c_H$</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
</table>

Address Offset from DrawBaseAddress
S Sign bit or sign extension
0 Not used or 0 extension
Int Integer or integer part of fixed point data
Frac Fraction part of fixed point data

Sets coordinates parameters for rectangle drawing. The foreground color is used.

RXs	Sets the X coordinates of top left vertex
Rys	Sets the Y coordinates of top left vertex
RsizeX	Sets horizontal size
RsizeY	Sets vertical size

12.5.7 Blt registers

Sets the parameters of each register as described below:

Set the Tcolor register with the ***SetRegister*** command.

Note that the Tcolor register cannot be set at access from the CPU and by drawing commands.

Each register except the Tcolor register is set by executing a drawing command.

Note that access from the CPU and the ***SetRegister*** command cannot be used.

Register	Address	31	30	29	28	27	26	25	24	23–16	15–0
SADDR	0240_H	0	0	0	0	0	0	0	0	Address	
SStride	0244_H	0	0	0	0	Int					0
SRXs	0248_H	0	0	0	0	Int					0
SRYs	$024c_H$	0	0	0	0	Int					0
DADDR	0250_H	0	0	0	0	0	0	0	0	Address	
DStride	0254_H	0	0	0	0	Int					0
DRXs	0258_H	0	0	0	0	Int					0
DRYs	$025c_H$	0	0	0	0	Int					0
BRsizeX	0260_H	0	0	0	0	Int					0
BRsizeY	0264_H	0	0	0	0	Int					0
TColor	0280_H	0									Color

Address	Offset from DrawBaseAddress
S	Sign bit or sign extension
0	Not used or 0 extension
Int	Integer or integer part of fixed point data
Frac	Fraction part of fixed point data

Sets parameters for Blt operations

SADDR	Sets start address of source rectangle area in byte address
SStride	Sets stride of source
SRXs	Sets X coordinates start position of source rectangle area
SRYs	Sets Y coordinates start position of source rectangle area
DADDR	Sets start address of destination rectangle area in byte address
DStride	Sets stride of destination
DRXs	Sets X coordinates start position of destination rectangle area
DRYs	Sets Y coordinates start position of destination rectangle area
BRsizeX	Sets horizontal size of rectangle
BRsizeY	Sets vertical size of rectangle
Tcolor	Sets transparent color For indirect color, set a palette code in the lower 8 bits.

12.5.8 2D line with XY setup drawing registers

Each register is used by the drawing commands. The registers cannot be accessed from the CPU.

Register	Address	31	30	29	28	27 … 16	15 … 0
LX0dc	0540_H	0	0	0	0	Int	0
LY0dc	0544_H	0	0	0	0	Int	0
LX1dc	0548_H	0	0	0	0	Int	0
LY1dc	$054c_H$	0	0	0	0	Int	0

Address Offset from DrawBaseAddress
S Sign bit or sign extension
0 Not used or 0 extension
Int Integer or integer part of fixed point data
Frac Fraction part of fixed point data

Sets coordinates of line end points for 2D Line with XY setup drawing

LX0dc	Sets X coordinates of vertex V0
LY0dc	Sets Y coordinates of vertex V0
LX1dc	Sets X coordinates of vertex V1
LY1dc	Sets Y coordinates of vertex V1

12.5.9 2D triangle with XY setup drawing registers

Each register is used by the drawing commands. The registers cannot be accessed from the CPU or using the ***SetRegister*** command.

<table>
<tr><th>Register</th><th>Address</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>X0dc</td><td>0580h</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td>Y0dc</td><td>0584h</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td>X1dc</td><td>0588h</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td>Y1dc</td><td>058ch</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td>X2dc</td><td>0590h</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
<tr><td>Y2dc</td><td>0594h</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="12">Int</td><td colspan="16">0</td></tr>
</table>

Address	Offset from DrawBaseAddress
S	Sign bit or sign extension
0	Not used or 0 extension
Int	Integer or integer part of fixed point data
Frac	Fraction part of fixed point data

Sets coordinates of three vertices for 2D Triangle with XY setup drawing

X0dc	Sets X coordinates of vertex V0
Y0dc	Sets Y coordinates of vertex V0
X1dc	Sets X coordinates of vertex V1
Y1dc	Sets Y coordinates of vertex V1
X2dc	Sets X coordinates of vertex V2
Y2dc	Sets Y coordinates of vertex V2

12.5.10 Display list FIFO registers

DFIFO (Displaylist FIFO)

Register address	DrawBaseAddress+ $4A0_H$
Bit number	31 : 30 : 29 : 28 : 27 : 26 : 25 : 24 : 23 : 22 : 21 : 20 : 19 : 18 : 17 : 16 : 15 : 14 : 13 : 12 : 11 : 10 : 9 : 8 : 7 : 6 : 5 : 4 : 3 : 2 : 1 : 0
Bit field name	DFIFO
R/W	W
Initial value	Don't care

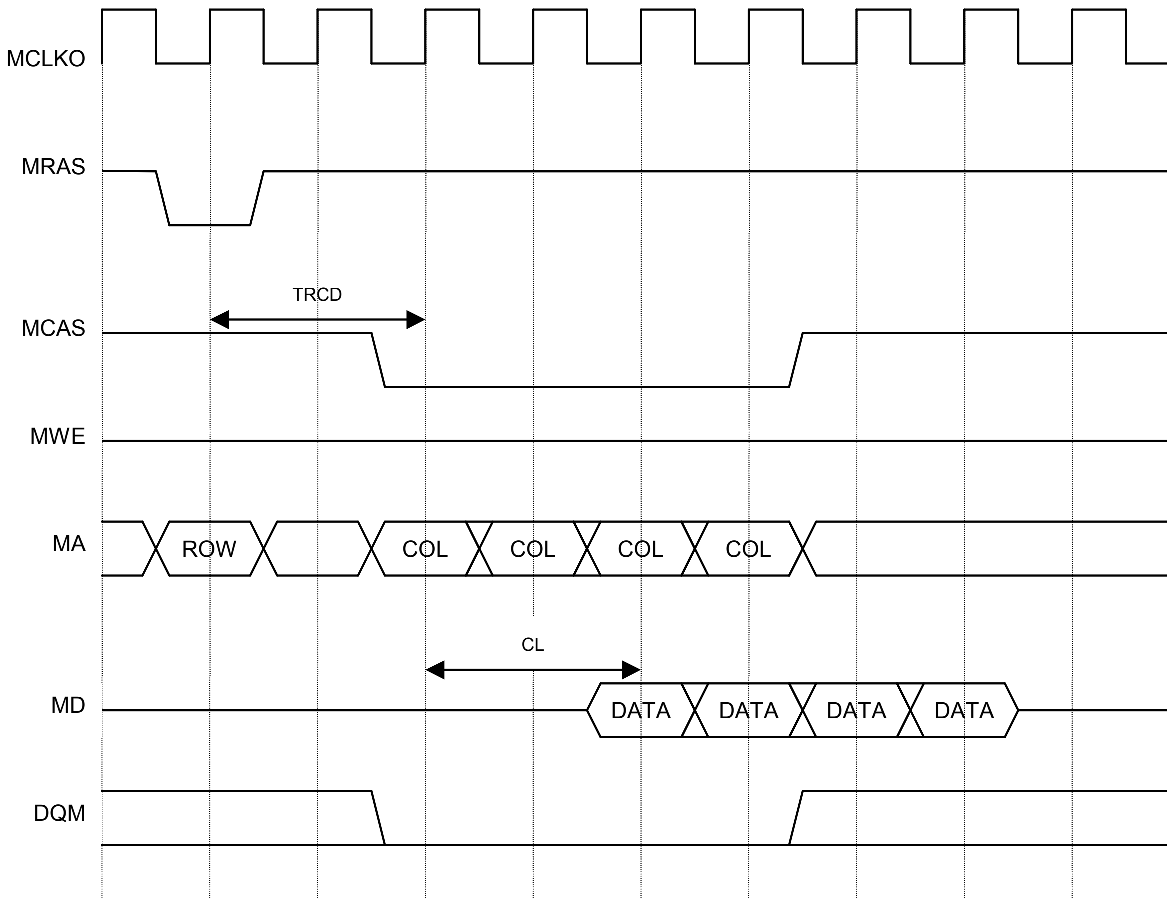
FIFO registers for Display List transfer. The Display List FIFO is 32 entries deep.

13 TIMING DIAGRAM

13.1 Graphics Memory Interface

The LIME GDC access timing and graphics memory access timing are explained here.

13.1.1 Timing of read access to same row address



ROW: Row Address
COL: Column Address
DATA: READ DATA

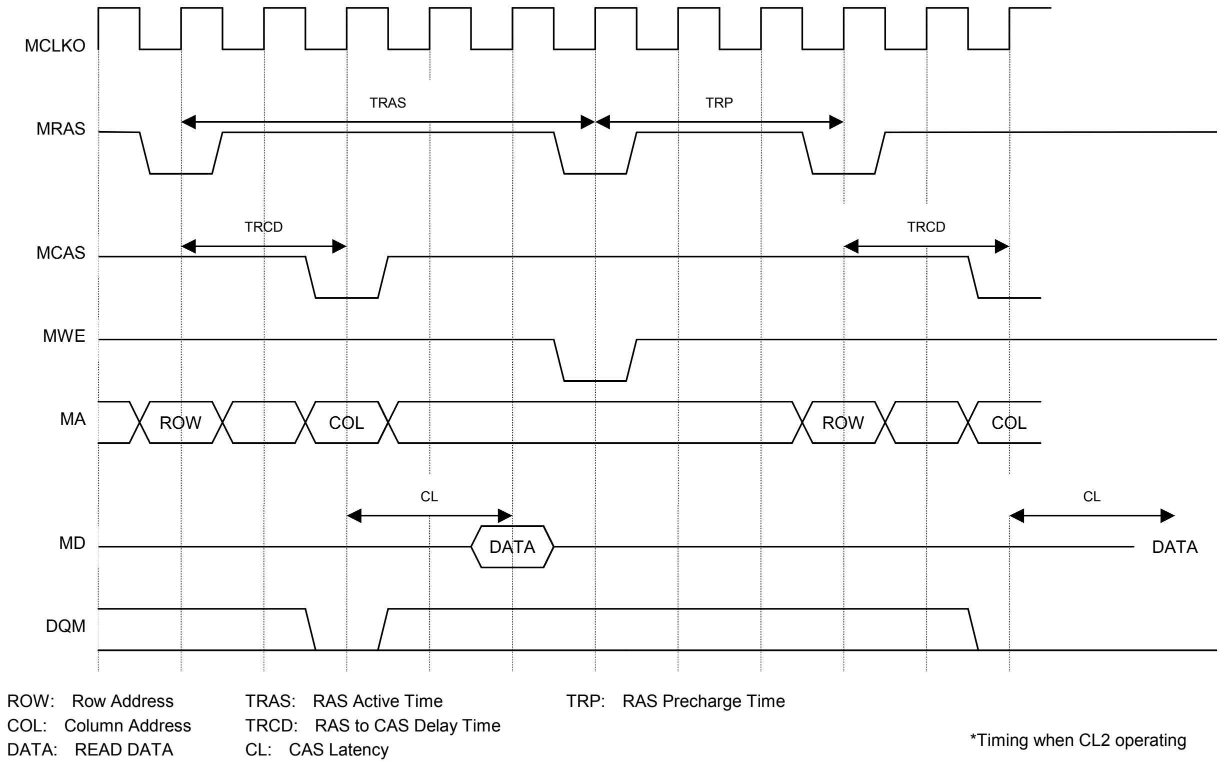
TRCD: RAS to CAS Delay Time
CL: CAS Latency

*Timing when CL2 operating

Timing of Read Access to Same Row Address

The above timing diagram shows that read access is made four times from LIME to the same row address of SDRAM. The ***ACTV*** command is issued and then the ***READ*** command is issued after TRCD elapses. Then data that is output after the elapse of CL after the ***READ*** command is issued is captured into LIME.

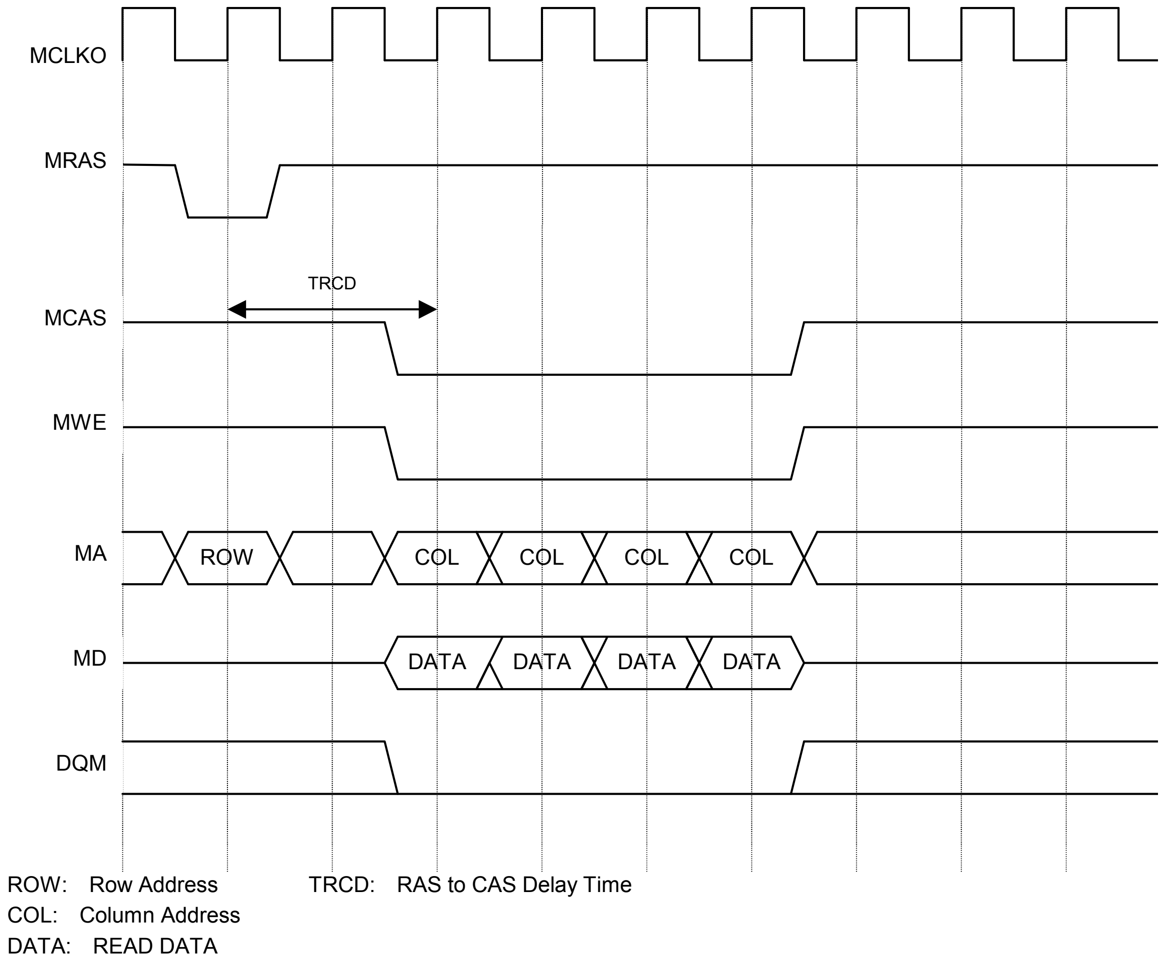
13.1.2 Timing of read access to different row addresses



Timing of Read Access to Different Row Addresses

The above timing diagram shows that read access is made from LIME to different row addresses of SDRAM. The first and next address to be read fall across an SDRAM page boundary, so the ***Pre-charge*** command is issued at the timing satisfying TRAS, and then after the elapse of TRP, the ***ACTV*** command is reissued, and then the ***READ*** command is issued.

13.1.3 Timing of write access to same row address

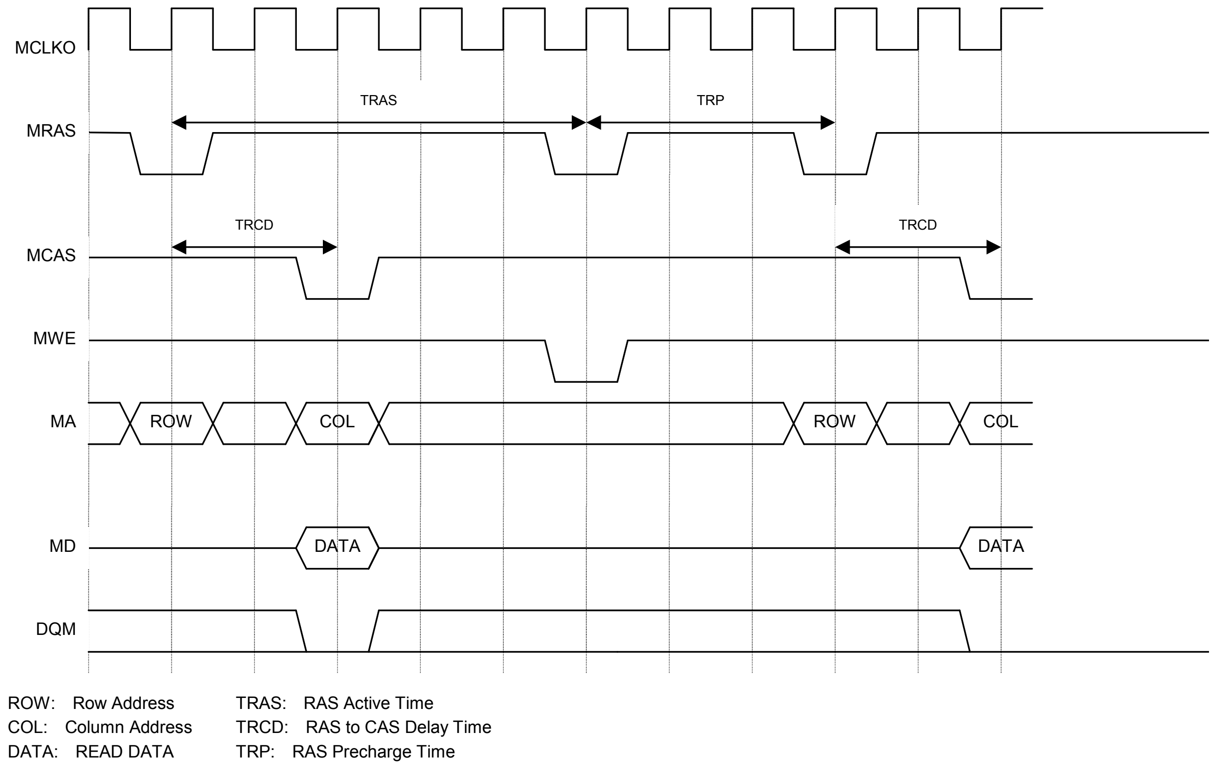


Timing of Write Access to Same Row Address

The above timing diagram shows that write access is made form times form LIME to the same row address of SDRAM.

The ***ACTV*** command is issued, and then after the elapse of TRCD, the ***WRITE*** command is issued to write to SDRAM.

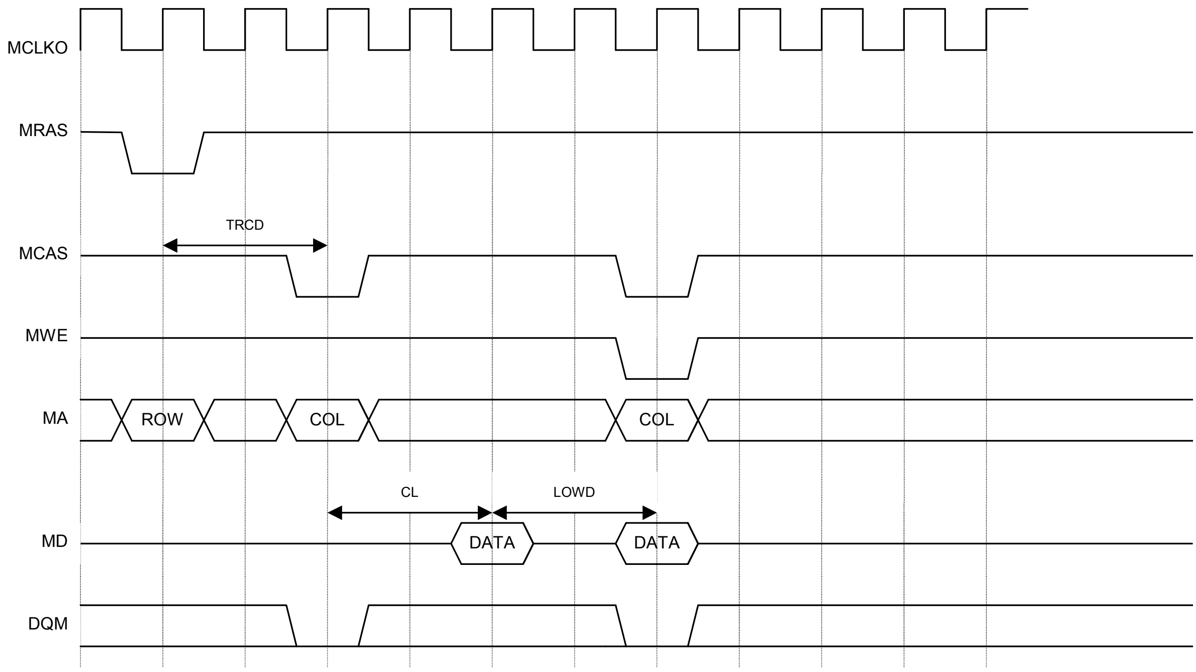
13.1.4 Timing of write access to different row addresses



Timing of Write Access to Different Row Addresses

The above timing diagram shows that write access is made from LIME to different row addresses of SDRAM. The first and next address to be write fall across an SDRAM page boundary, so the ***Pre-charge*** command is issued at the timing satisfying TRAS, and then after the elapse of TRP, the ***ACTV*** command is reissued, and then the ***WRITE*** command is issued.

13.1.5 Timing of read/write access to same row address



ROW: Row Address
COL: Column Address
DATA: READ DATA
TRAS: RAS Active Time
TRCD: RAS to CAS Delay Time
CL: CAS Latency
TRP: RAS Precharge Time
LOWD: Last Output to Write Command Delay

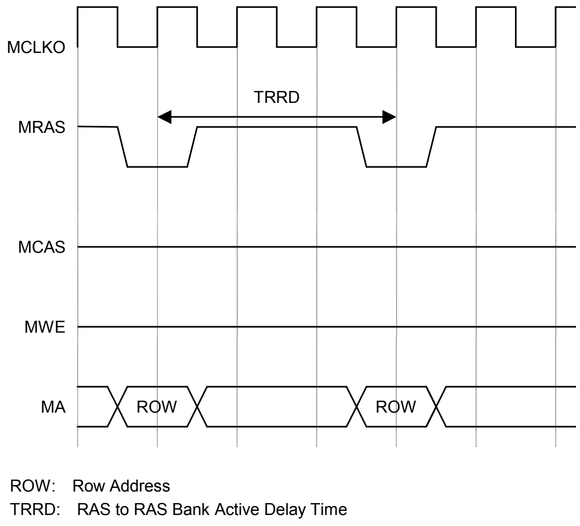
Timing when CL2 operating

Timing of Read/Write Access to Same Row Address

The above timing diagram shows that write access is made immediately after read access is made from LIME to the same row address of SDRAM.

Read data is output from SDRAM, LOWD elapses, and then the ***WRITE*** command is issued.

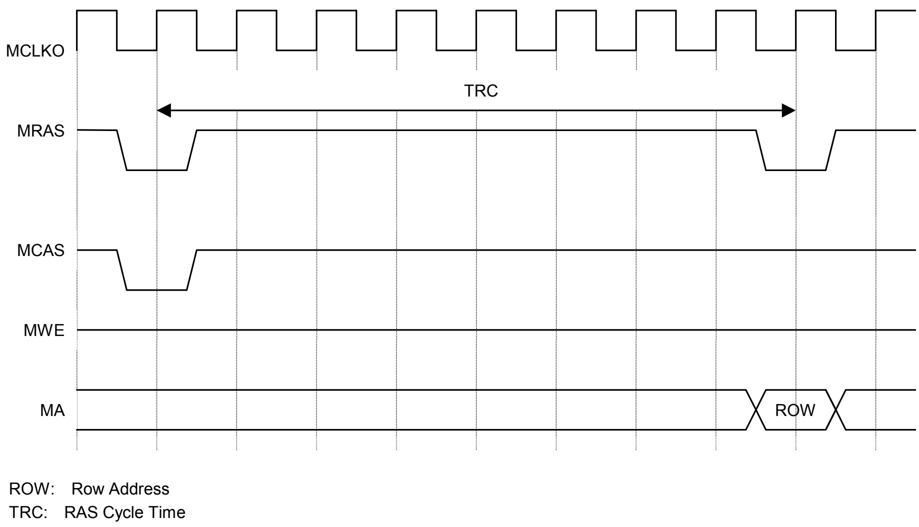
13.1.6 Delay between ACTV commands



Delay between ACTV Commands

The ACTV command is issued from LIME GDC to the row address of SDRAM after the elapse of ***TRRD*** after issuance of the previous ***ACTV*** command.

13.1.7 Delay between Refresh command and next ACTV command

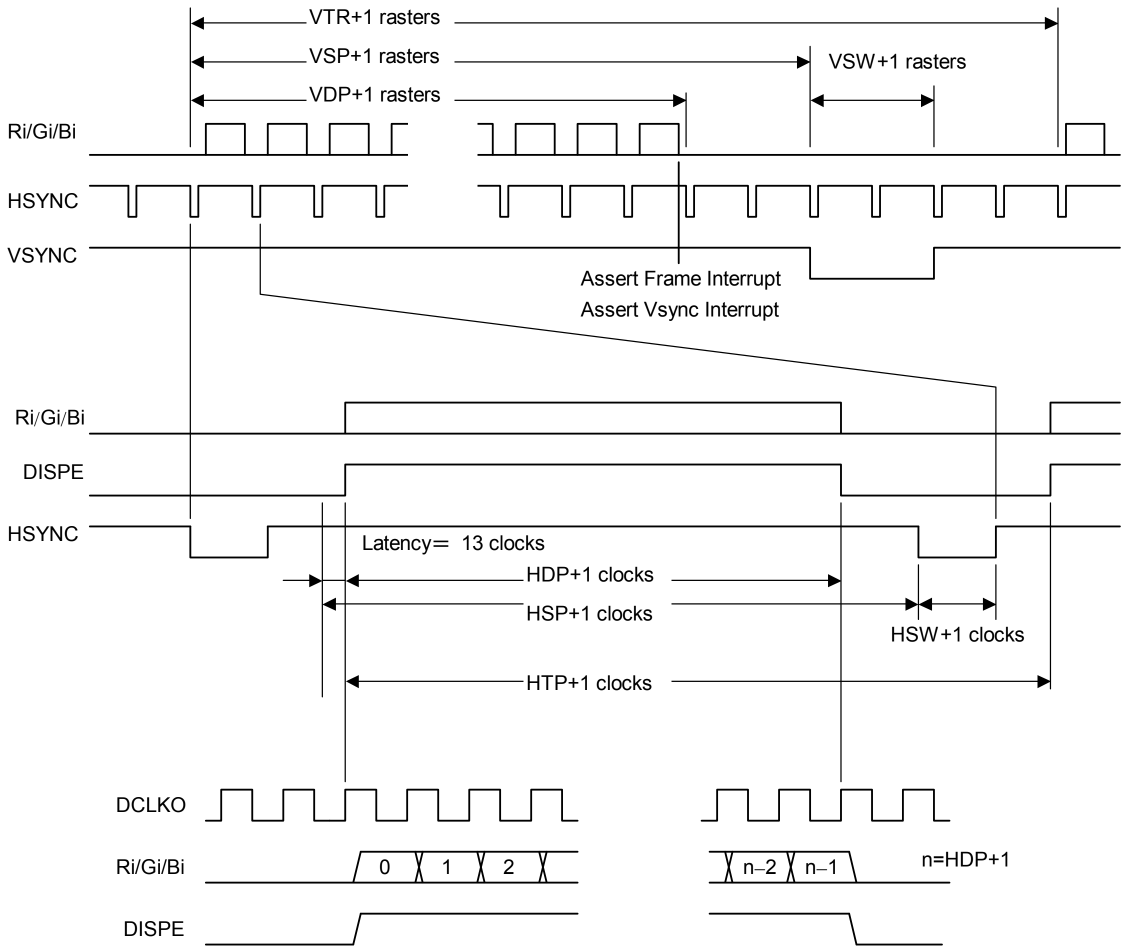


Delay between Refresh Command and Next ACTV Command

The ***ACTV*** command is issued after the elapse of TRC after issuance of the ***Refresh*** command.

13.2 Display Timing

13.2.1 Non-interlace mode



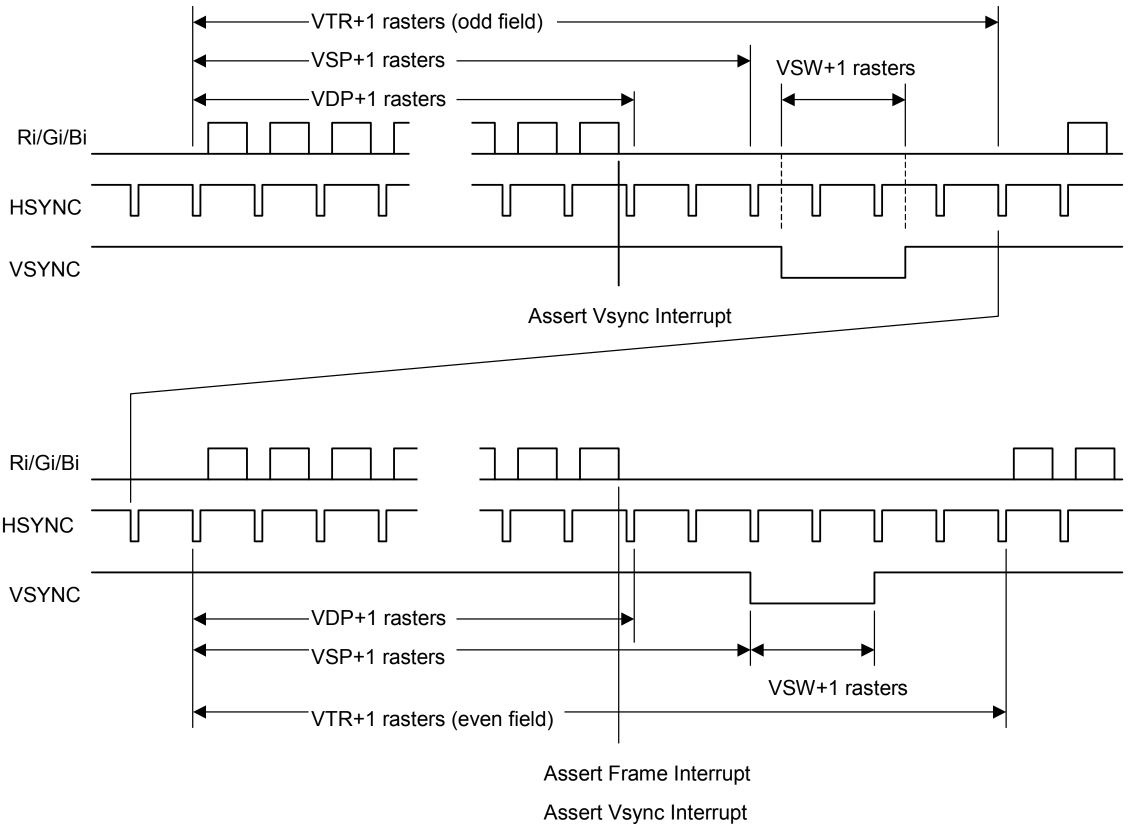
Non-interlace Timing

In the above diagram, VTR, HDP, etc., are the setting values of their associated registers.

The VSYNC/frame interrupt is asserted when display of the last raster ends. When updating display parameters, synchronize with the frame interrupt so no display disturbance occurs. Calculation for the next frame is started immediately after the vertical synchronization pulse is asserted, so the parameters must be updated by the time that calculation is started.

VSYNC is output 1 dot clock faster than HSYNC.

13.2.2 Interlace video mode



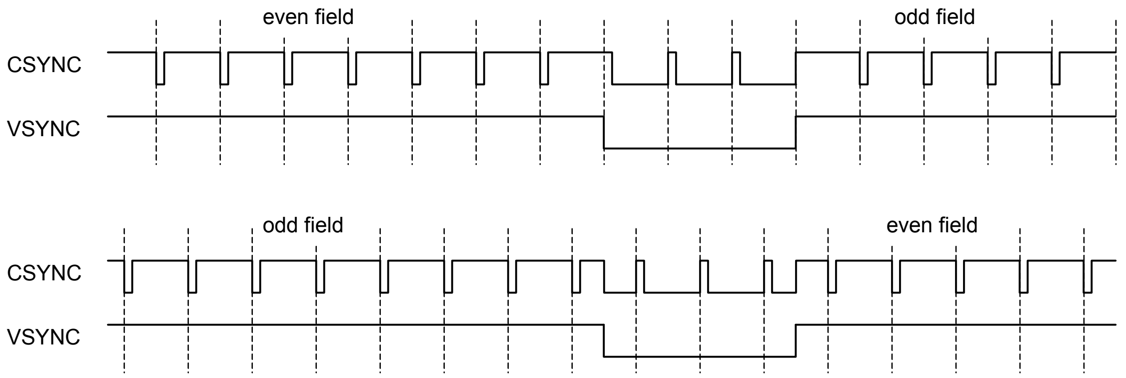
Interlace Video Timing

In the above diagram, VTR, HDP, etc., are the setting values of their associated registers.

The interlace mode also operates at the same timing as the interlace video mode. The only difference between the two modes is the output image data.

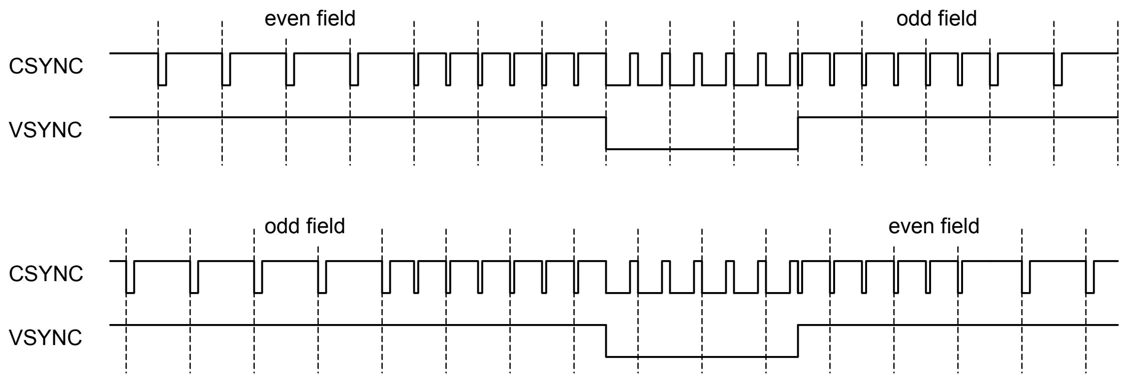
13.2.3 Composite synchronous signal

When the EEQ bit of the DCM register is “0”, the CSYNC signal output waveform is as shown below.



Composite Synchronous Signal without Equalizing Pulse

When the EEQ bit of the DCM register is “1”, the equalizing pulse is inserted into the CSYNC signal, producing the waveform shown below.

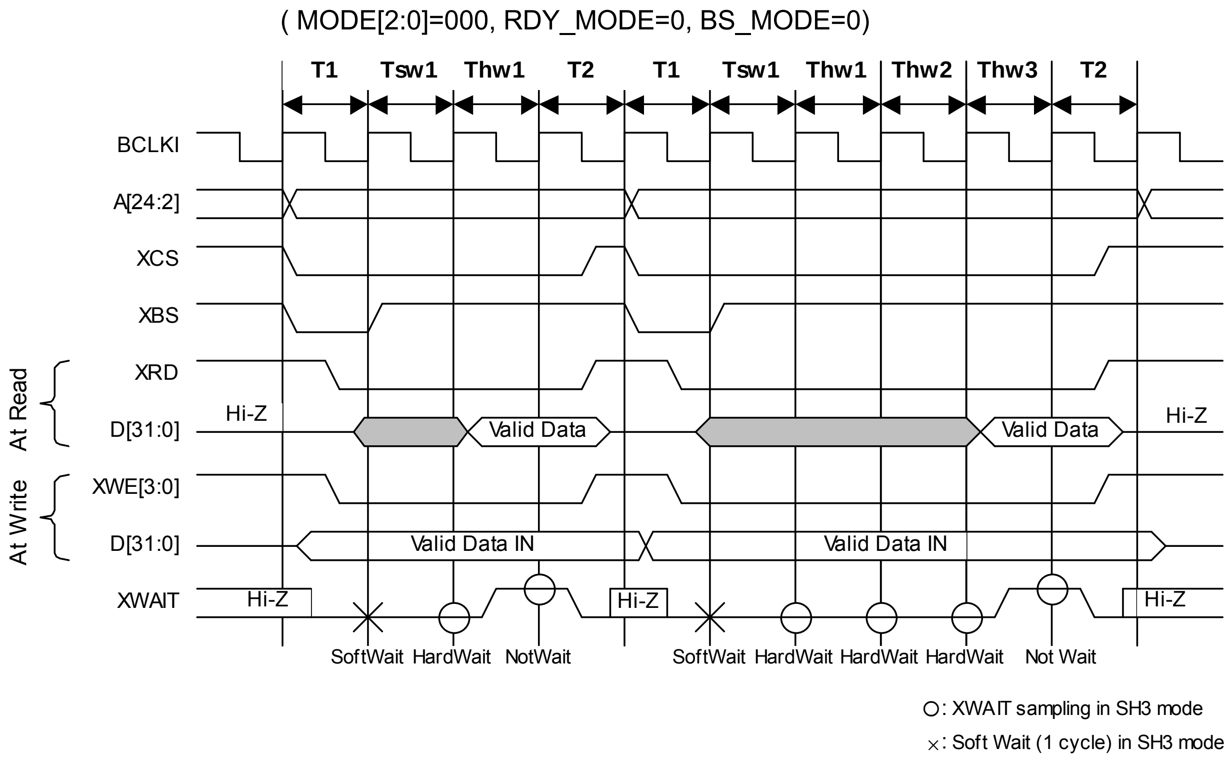


Composite Synchronous Signal with Equalizing Pulse

The equalizing pulse is inserted when the vertical blanking time period starts. It is also inserted three times after the vertical synchronization time period has elapsed.

13.3 Host interface Timing

13.3.1 CPU read/write timing diagram in SH3 mode (Normally Not Ready Mode)



T1: Read/write start cycle (XRDY in wait state)

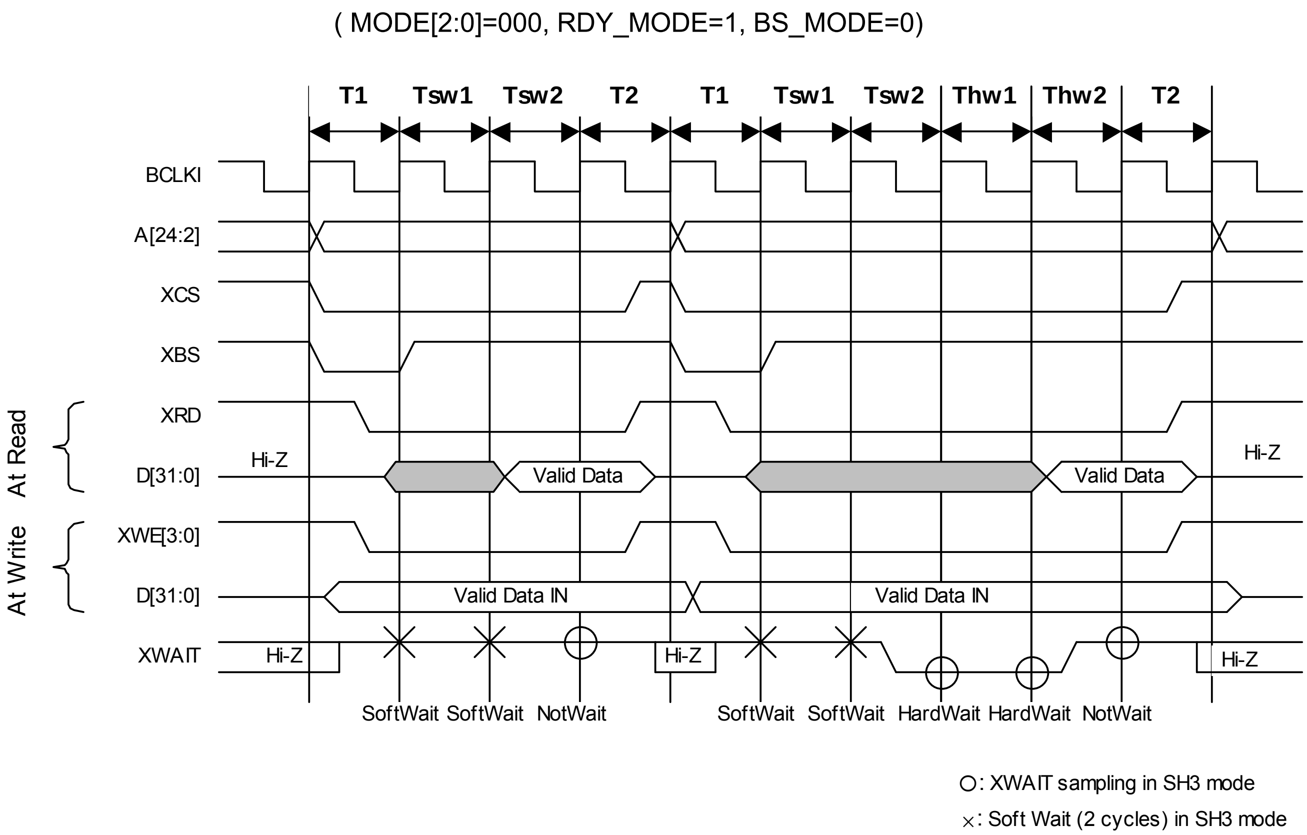
Tsw*: Software wait insertion cycle (1 cycle setting)

Thw*: Hardware wait insertion cycle (XRDY cancels the wait state after the preparations)

T2: Read/write end cycle (XRDY ends in wait state)

Fig. Read/Write Timing Diagram for SH3 (Normally Not Ready Mode)

13.3.2 CPU read/write timing diagram in SH3 mode (Normally Ready Mode)



T1: Read/write start cycle (XRDY in not wait state)

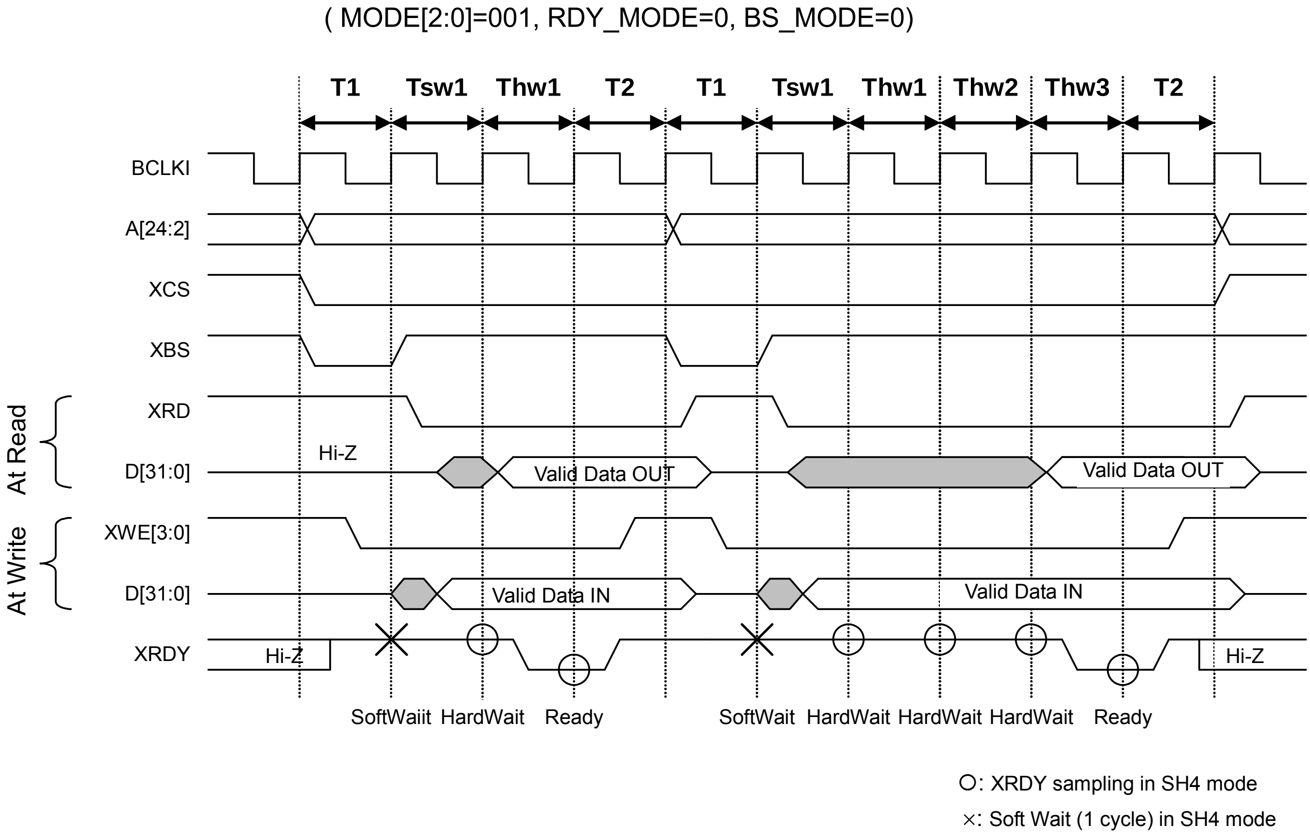
Tsw*: Software wait insertion cycle (2-cycle setting required)

Thw*: Hardware wait insertion cycle (In hardware state when the immediate accessing is disabled)

T2: Read/write end cycle (XRDY ends in not wait state)

Fig. Read/Write Timing Diagram for SH3 (Normally Ready Mode)

13.3.3 CPU read/write timing diagram in SH4 mode (Normally Not Ready Mode)



T1: Read/write start cycle (XRDY in the not ready state)

Tsw*: Software wait insertion cycle (1 cycle)

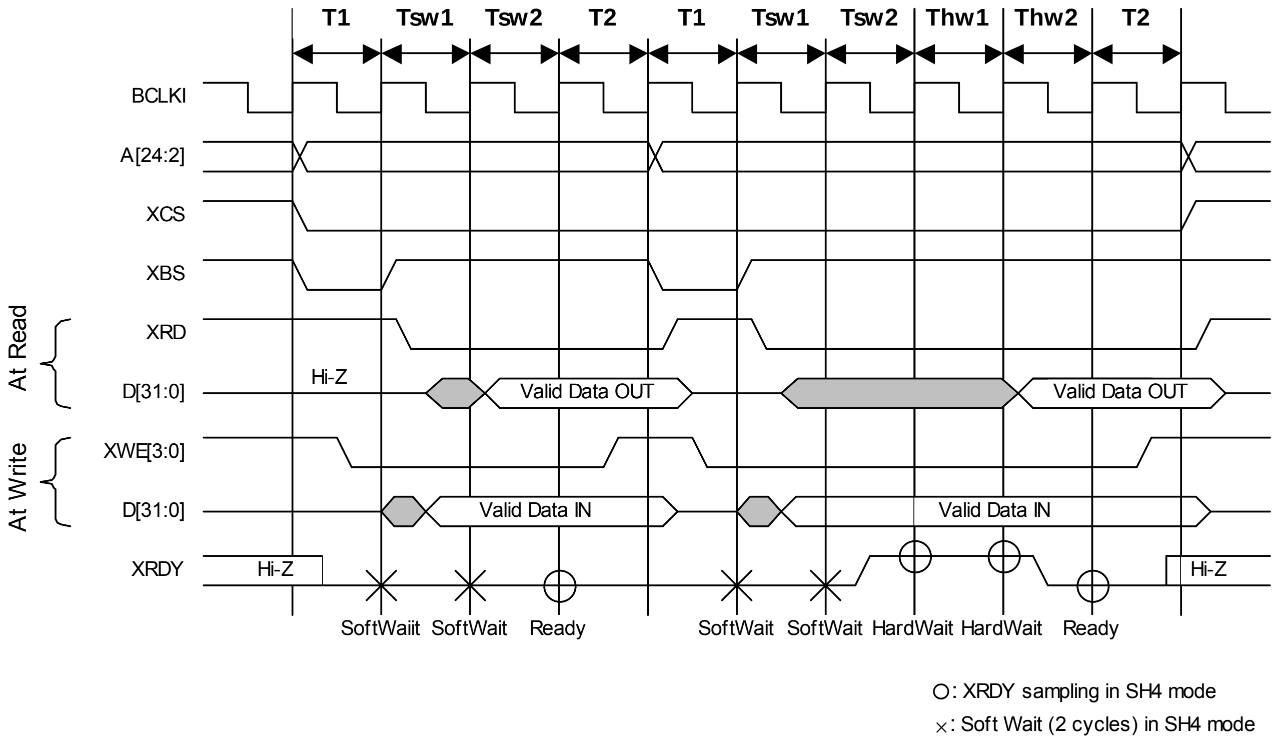
Twh*: Hardware wait insertion cycle (XRDY asserts Ready after the preparations)

T2: Read/write end cycle (XRDY ends in not ready state)

Fig. Read/Write Timing Diagram for SH4 Mode (Normally Not Ready Mode)

13.3.4 CPU read/write timing diagram in SH4 mode (Normally Ready Mode)

(MODE[2:0]=001, RDY_MODE=1, BS_MODE=0)



T1: Read/write start cycle (XRDY in ready state)

Tsw*: Software wait insertion cycle (2-cycle setting required)

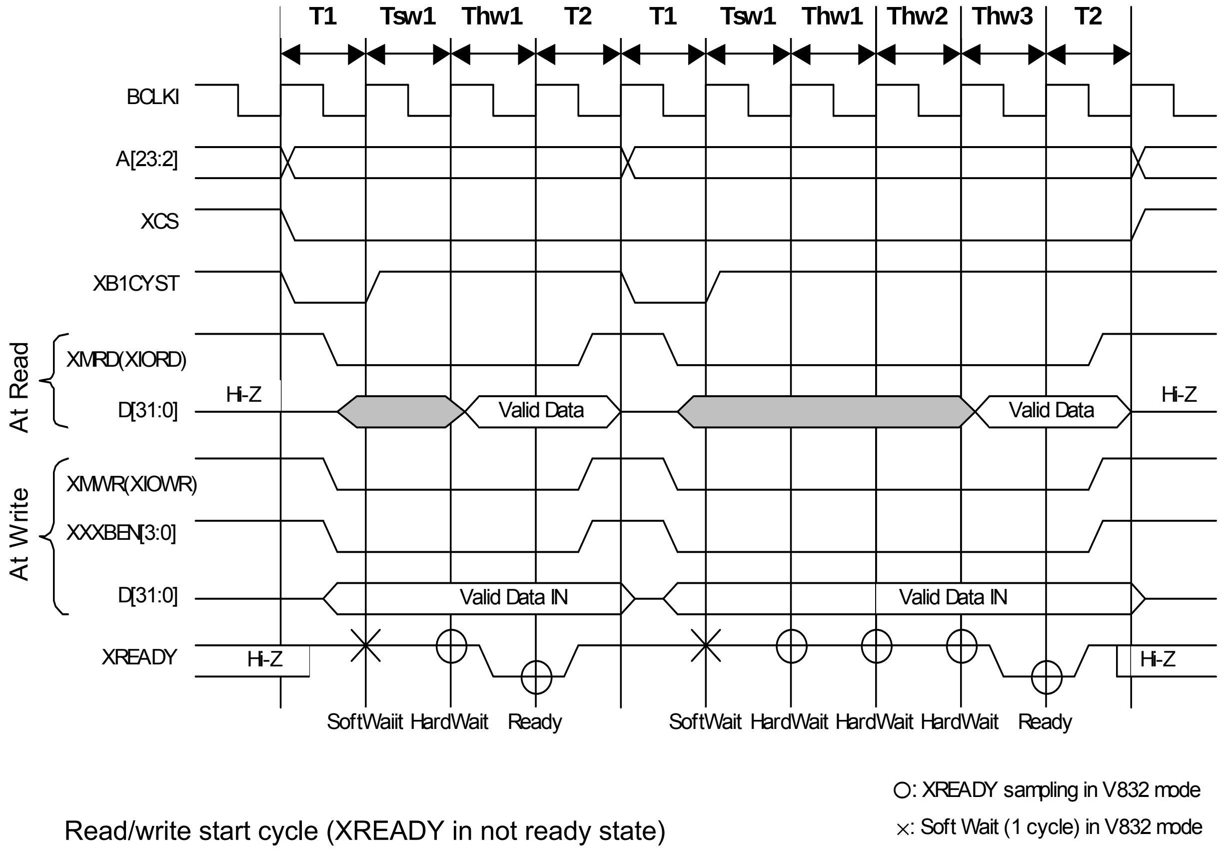
Twh*: Hardware wait insertion cycle (XRDY asserts Ready after the preparations)

T2: Read/write end cycle (XRDY ends in ready state.)

Fig. CPU Read/Write Timing Diagram for SH4 Mode (Normally Ready Mode)

13.3.5 CPU read/write timing diagram in V832 mode (Normally Not Ready Mode)

(MODE[2:0]=010, RDY_MODE=0, BS_MODE=0)



T1: Read/write start cycle (XREADY in not ready state)

Tsw*: Software wait insertion cycle

Twh*: Hardware wait insertion cycle (XREADY asserts Ready after the preparations)

T2: Read/write end cycle (XREADY ends in not ready state)

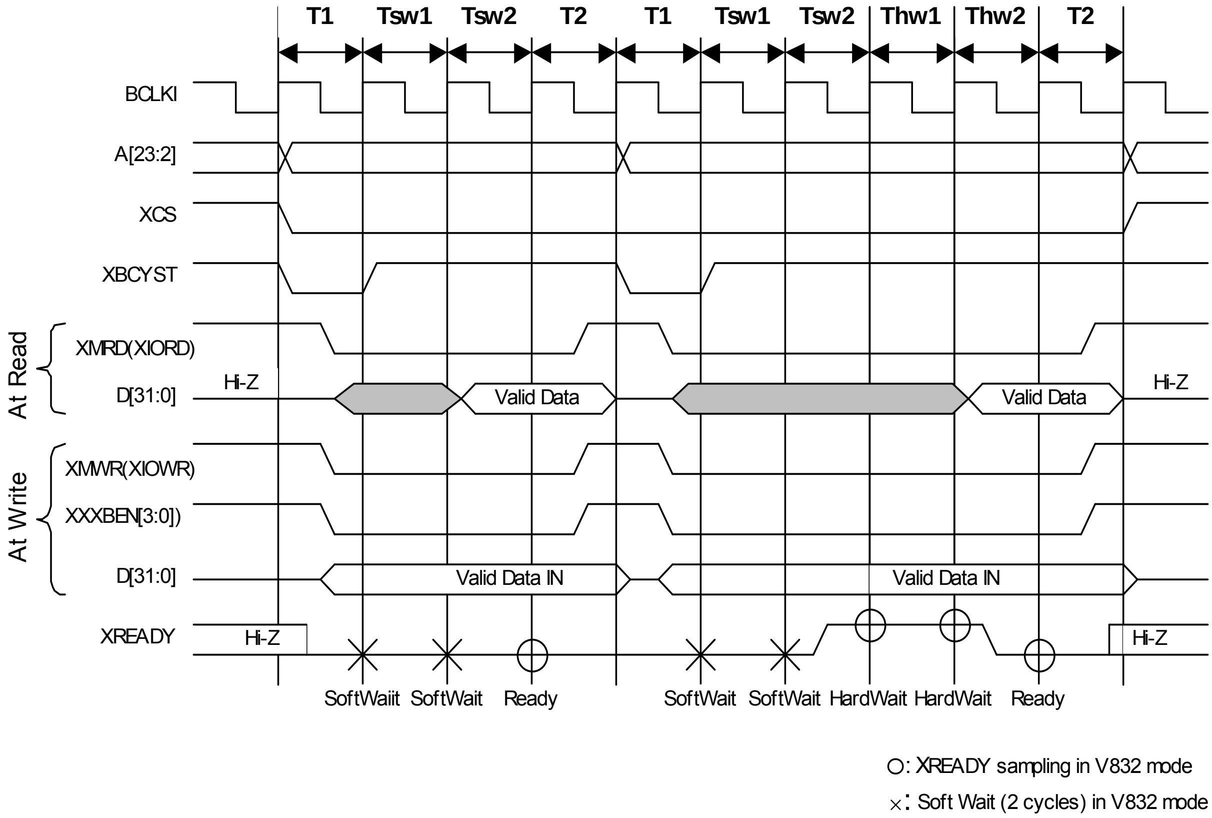
Notes: 1.The XxxBEN signal is used only for a write from the CPU; it is not used for a read from the CPU.

2.The CPU always inserts one cycle wait after read access.

Fig. Read/Write Timing Diagram in V832 Mode (Normally Not Ready Mode)

13.3.6 CPU read/write timing diagram in V832 mode (Normally Ready Mode)

(MODE[2:0]=010, RDY_MODE=1, BS_MODE=0)



T1: Read/write start cycle (XREADY in ready state)

Tsw*: Software wait insertion cycle (2-cycle setting required)

Twh*: Hardware wait insertion cycle (XREADY asserts Ready after the preparations)

T2: Read/write end cycle (XREADY ends in ready state)

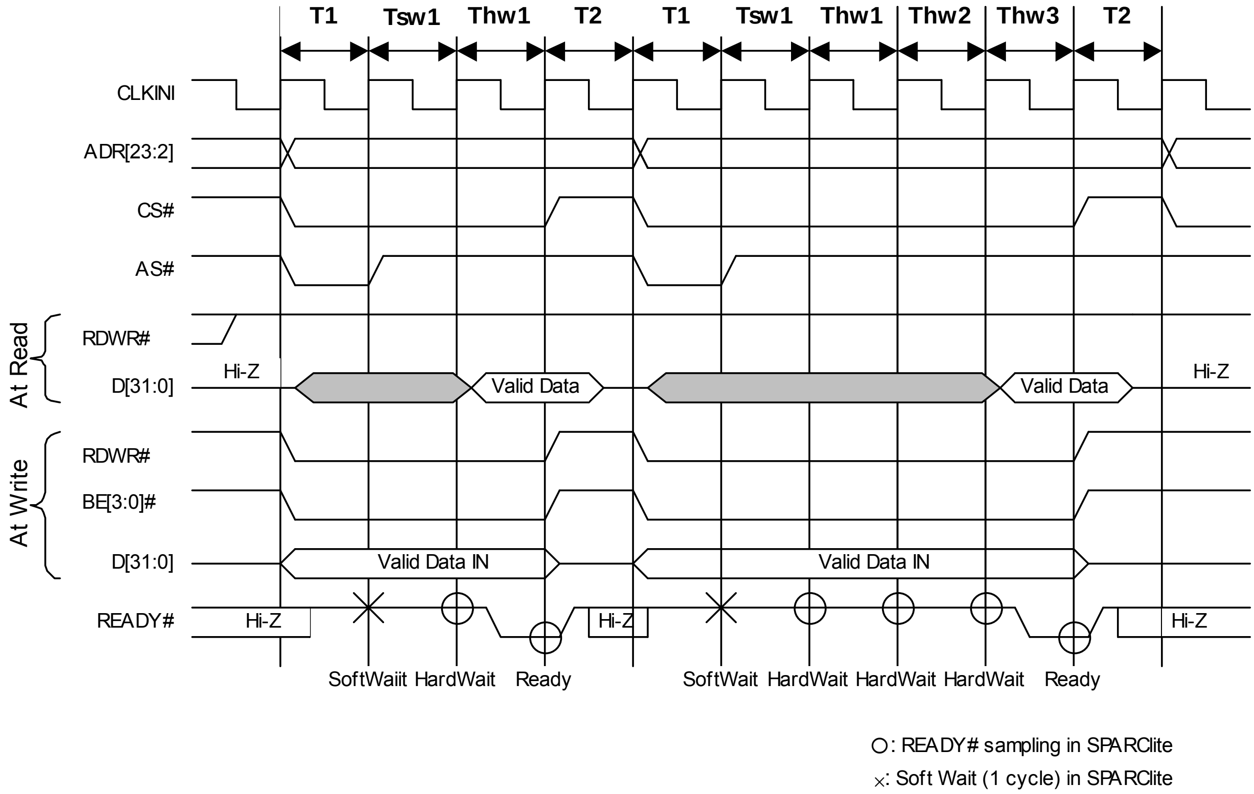
Notes: 1.The XxxBEN signal is used only for a write from the CPU; it is not used for a read from the CPU.

2.The CPU always inserts one cycle wait after read access.

Fig. Read/Write Timing Diagram in V832 Mode (Normally Ready Mode)

13.3.7 CPU read/write timing diagram in SPARClite (Normally Not Ready Mode)

(MODE[2:0]=011, RDY_MODE=0, BS_MODE=0)



T1: Read/write start cycle (READY# in not ready state)

Tsw*: Software wait insertion cycle

Twh*: Hardware wait insertion cycle (READY# asserts Ready after the preparations)

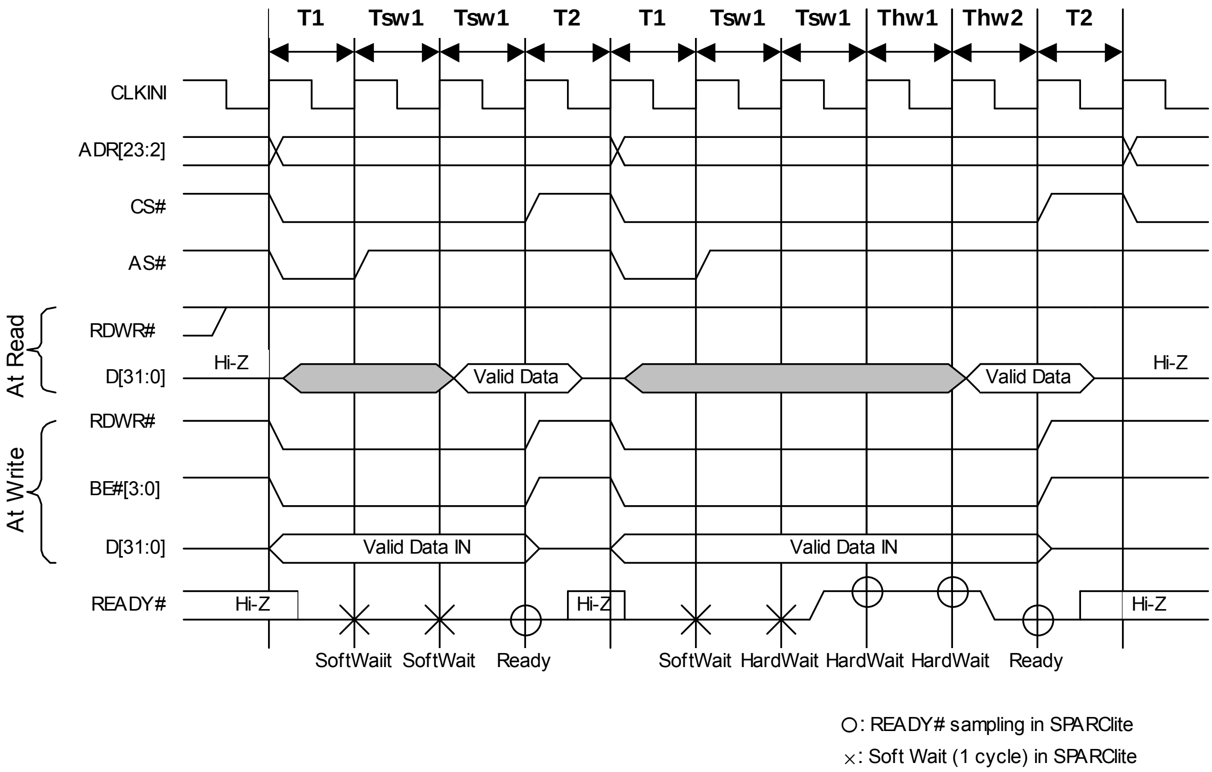
T2: Read/write end cycle (READY# ends in not ready state)

Note: BE# signal is used only for a write from the CPU; it is not used for a read from the CPU.

Fig. Read/Write Timing Diagram in SPARClite (Normally Not Ready Mode)

13.3.8 CPU read/write timing diagram in SPARClite (Normally Ready Mode)

(MODE[2:0]=011, RDY_MODE=1, BS_MODE=0)



T1: Read/write start cycle (READY# in ready state)

Tsw*: Software wait insertion cycle (2-cycle setting required)

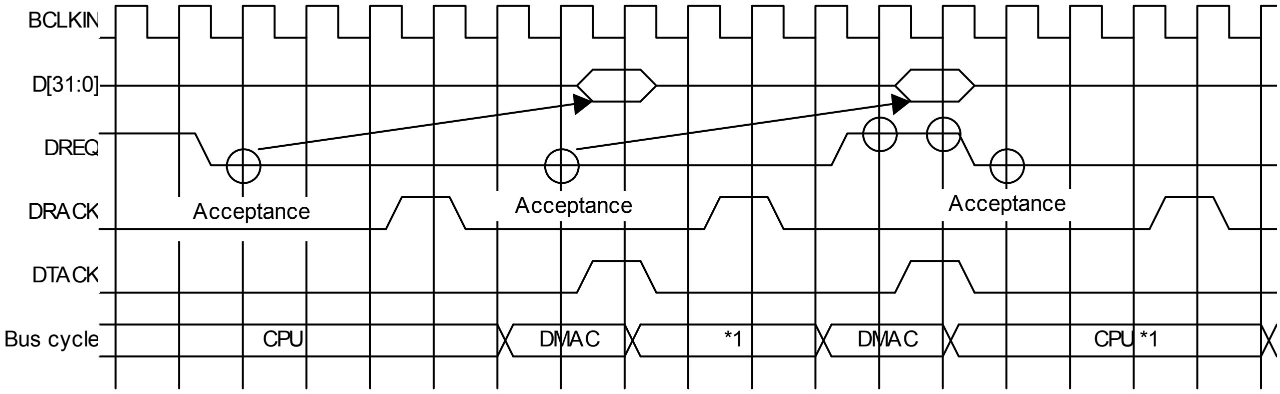
Twh*: Hardware wait insertion cycle (READY# asserts Ready after the preparations)

T2: Read/write end cycle (READY# ends in ready state)

Note: BE# signal is used only for a write from the CPU; it is not used for a read from the CPU.

Fig. Read/Write Timing Diagram in SPARClite (Normally Ready Mode)

13.3.9 SH4 single-address DMA write (transfer of 1 long word)



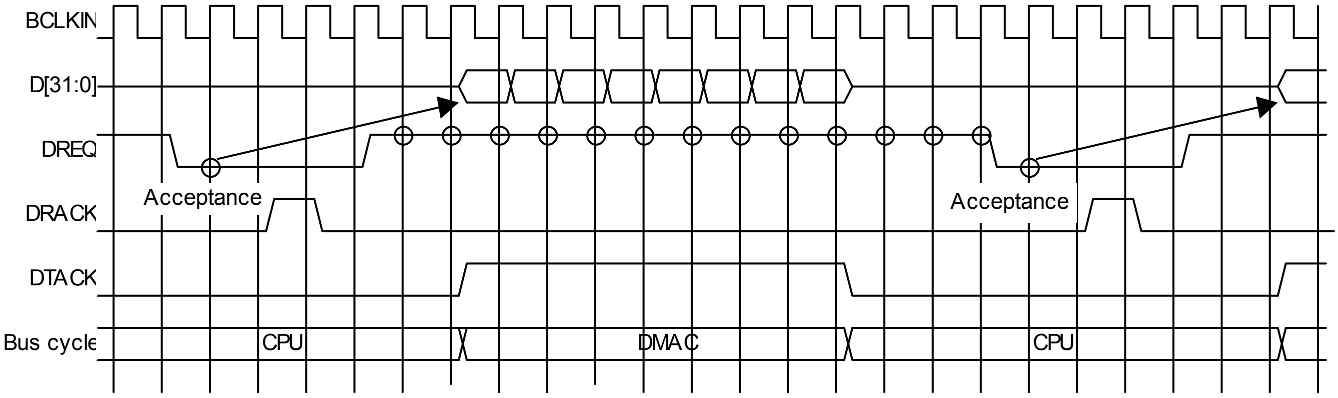
○: DREQ sampling and channel priority determination for SH mode (DREQ = level detection)

*1: In the cycle steal mode, even when DREQ is already asserted at the 2nd DREQ sampling, the right to use the bus is returned to the CPU temporarily. In the burst mode, DMAC secures the right to use the bus unless DREQ is negated.

Fig. SH4 Single-address DMA Write (Transfer of 1 Long Word)

CORAL writes data according to the DTACK assert timing. When data cannot be received, the DREQ signal is automatically negated. And then the DREQ signal is reasserted as soon as data reception is ready.

13.3.10 SH4 single-address DMA write (transfer of 8 long words)

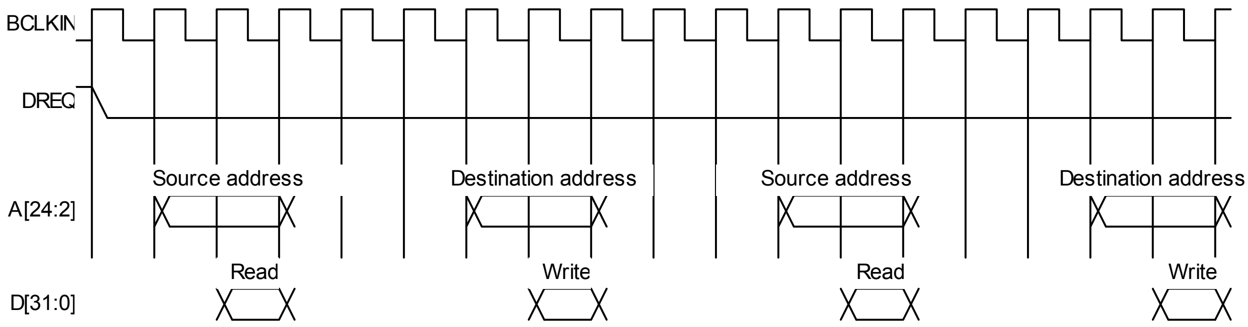


○: DREQ sampling and channel priority determination for SH mode (DREQ = level detection)

Fig. SH4 Single-address DMA Write (Transfer of 8 Long Words)

After the CPU has asserted DRACK, CORAL negates DREQ and receives 32-byte data in line with the DTACK assertion timing. As soon as the next data is ready to be received, CORAL reasserts DREQ but the reassertion timing depends on the internal status.

13.3.11 SH3/4 dual-address DMA (transfer of 1 long word)

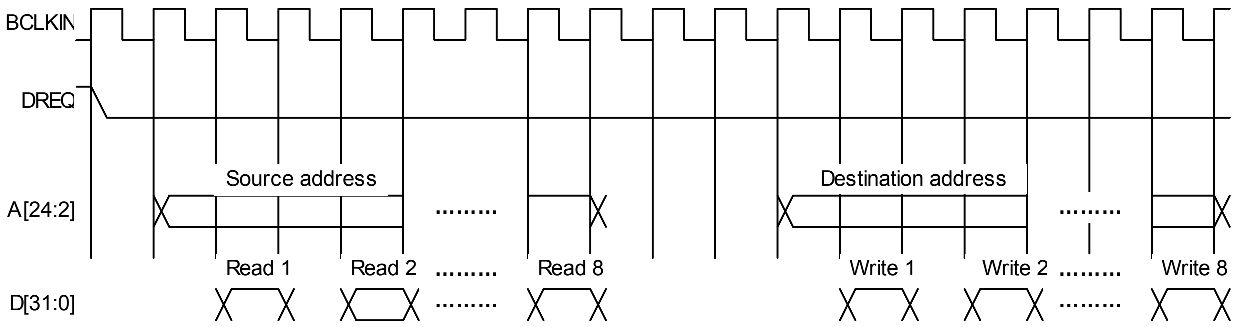


For the CORAL, the read/write operation is performed according to the SRAM protocol.

Fig. SH3/4 Dual-address DMA (Transfer of 1 Long Word)

In the dual-address mode, the DREQ signal is kept asserted until the transfer ends by default. Consequently, when CORAL cannot return the ready signal immediately, in order to negate the DREQ signal set the DBM register.

13.3.12 SH3/4 dual-address DMA (transfer of 8 long words)

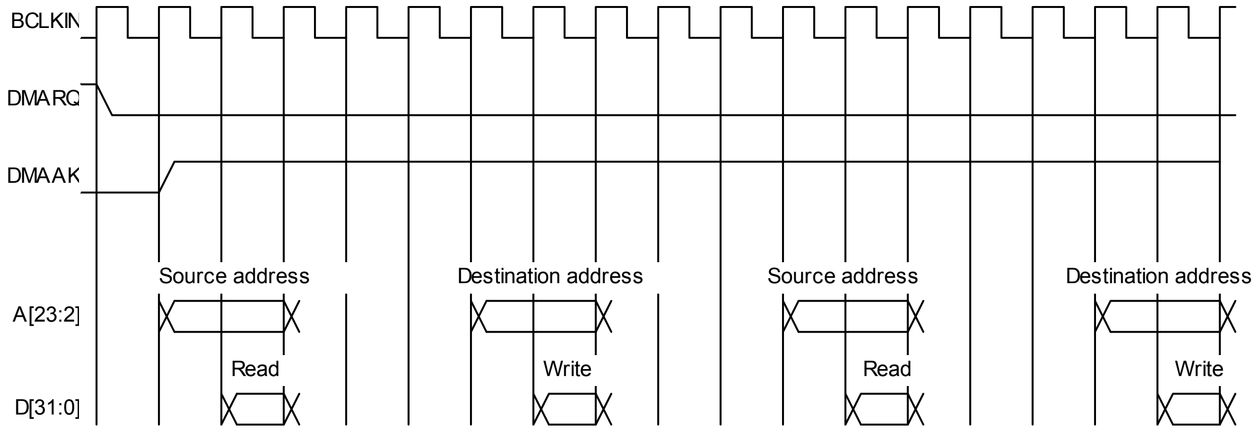


For the CORAL, the read/write operation is performed according to the SRAM protocol.

Fig. SH3/4 Dual-address DMA (Transfer of 8 Long Words)

In the dual-address mode, the DREQ signal is kept asserted until the transfer ends by default. Consequently, when CORAL cannot return the ready signal immediately, in order to negate the DREQ signal set the DBM register.

13.3.13 V832 DMA transfer

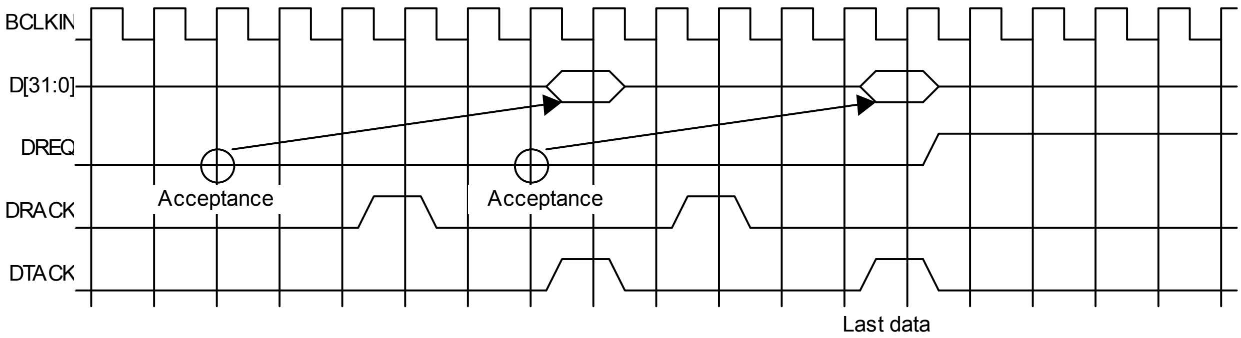


For the CORAL, the read/write operation is performed according to the SRAM protocol.

Fig. V832 DMA Transfer

In the dual-address mode, the DREQ signal is kept asserted until the transfer ends by default. Consequently, when CORAL cannot return the ready signal immediately, in order to negate the DREQ signal set the DBM register.

13.3.14 SH4 single-address DMA transfer end timing

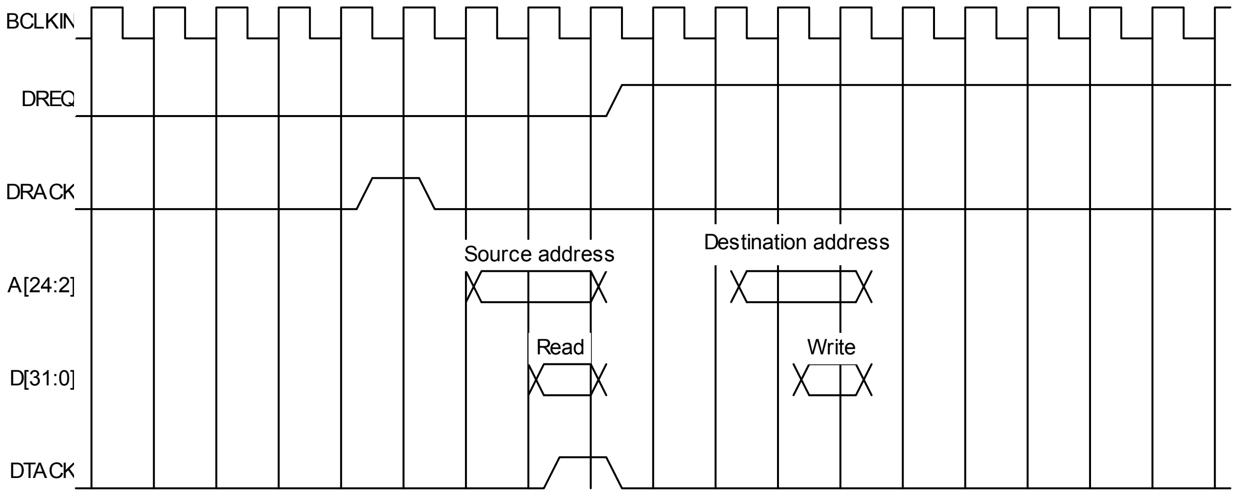


○: DREQ sampling and channel priority determination for SH mode (DREQ = level detection)

Fig. SH4 Single-address DMA Transfer End Timing

DREQ is negated three cycles after DRACK is written as the last data.

13.3.15 SH3/4 dual-address DMA transfer end timing



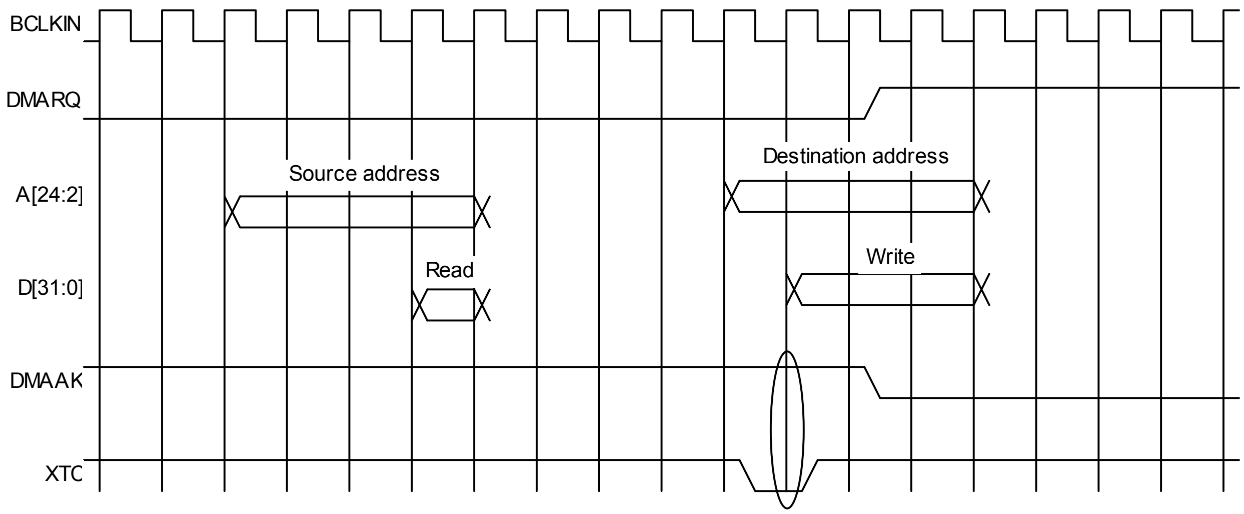
For the CORAL, the read/write operation is performed according to the SRAM protocol.

Fig. SH3/4 Dual-address DMA Transfer End Timing

DREQ is negated three cycles after DRACK is written as the last data.

Note: When the dual address mode (DMA) is used, the DTACK signal is not used.

13.3.16 V832 DMA transfer end timing



For the CORAL, the read/write operation is performed according to the SRAM protocol.

Fig. V832 DMA Transfer End Timing

DMMAK and XTC are logic ANDed inside CORAL to end DMA.

13.3.17 SH4 dual DMA write without ACK

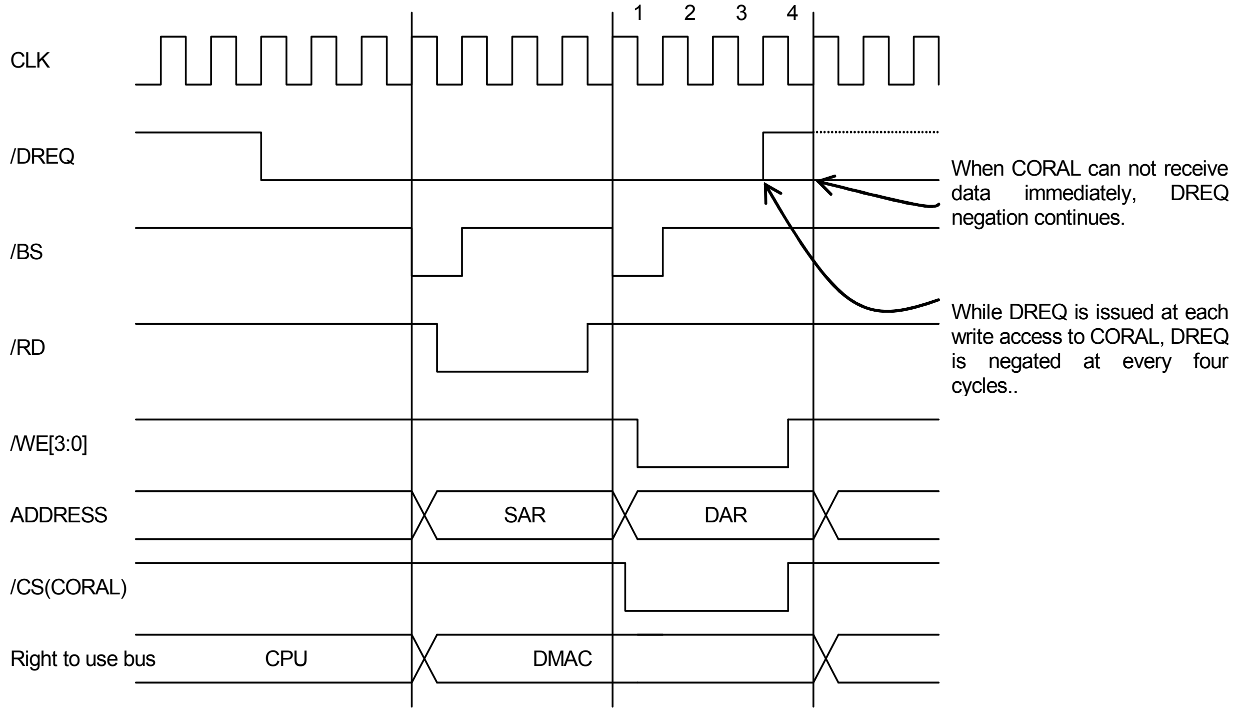


Fig. DREQ Negate Timing for Each Transfer

At each DMA transfer, DREQ is negated and then reasserted at the next cycle.

Only the FIFO address can be used as the destination address.

When CORAL cannot receive data immediately, DREQ negation continues. At that time, the negate timing is not only above diagram.

13.3.18 Dual-address DMA (without ACK) end timing

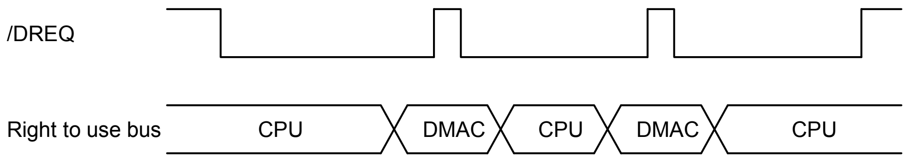


Fig. Dual-address DMA (without ACK) End Timing

Example: DMA operation when DMA transfer performed twice

(1) The CPU accesses the DREQ issue register (DRQ) of Coral to issue DREQ.

(2) The right to use bus is transferred from the CPU to the DMAC.

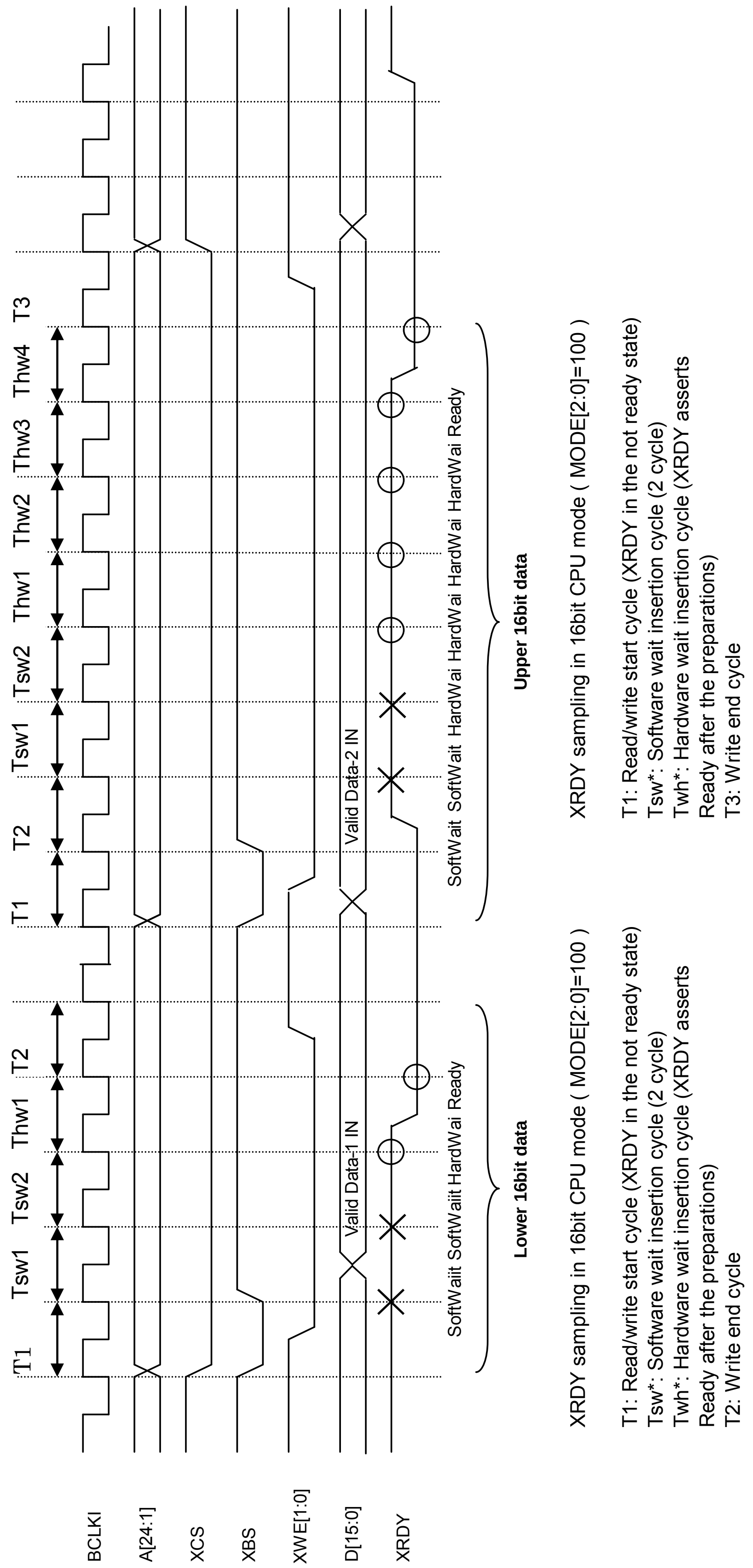
(3) In the first DMAC cycle, write is performed to CORAL and DREQ is negated; DREQ is reasserted in the next cycle.

(4) The right to use bus is returned to the CPU and the DREQ edge is detected, so the right to use bus is transferred to the DMAC.

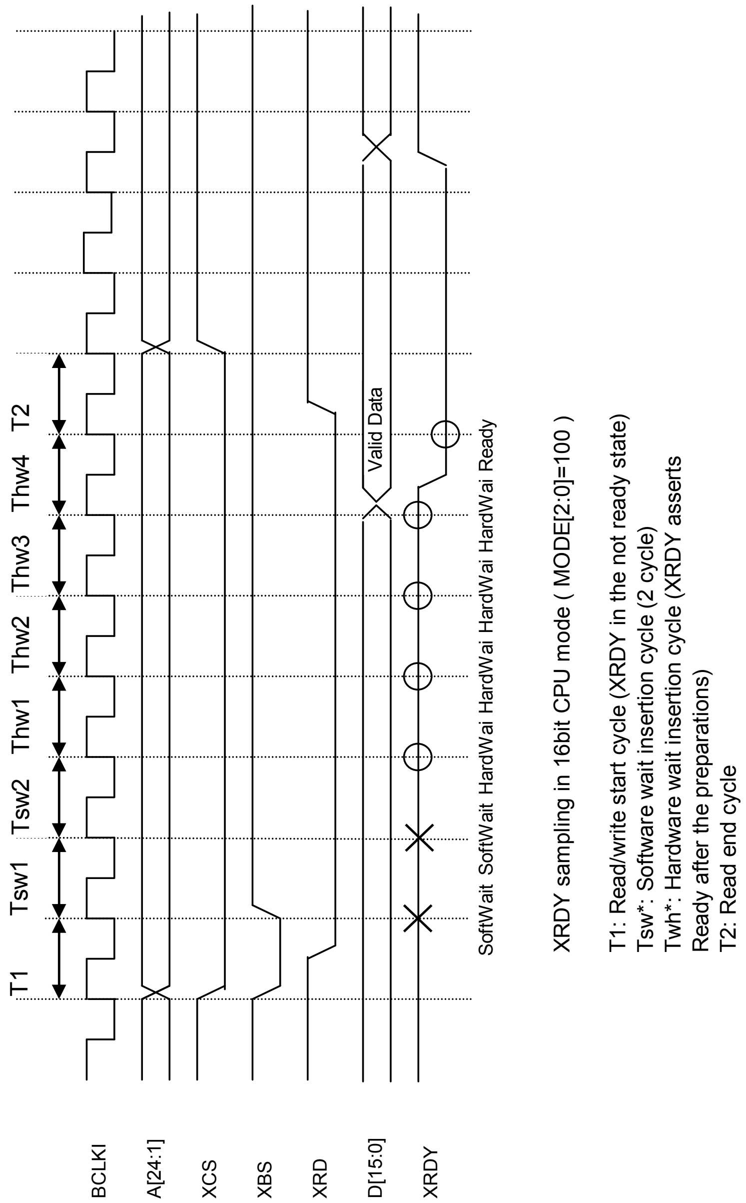
(5) The second write operation is performed and DREQ is negated, but DREQ is reasserted because CORAL does not recognize that the transfer has ended.

(6) The right to use bus is transferred to the CPU, so the CPU writes to the DTS register of CORAL to negate DREQ.

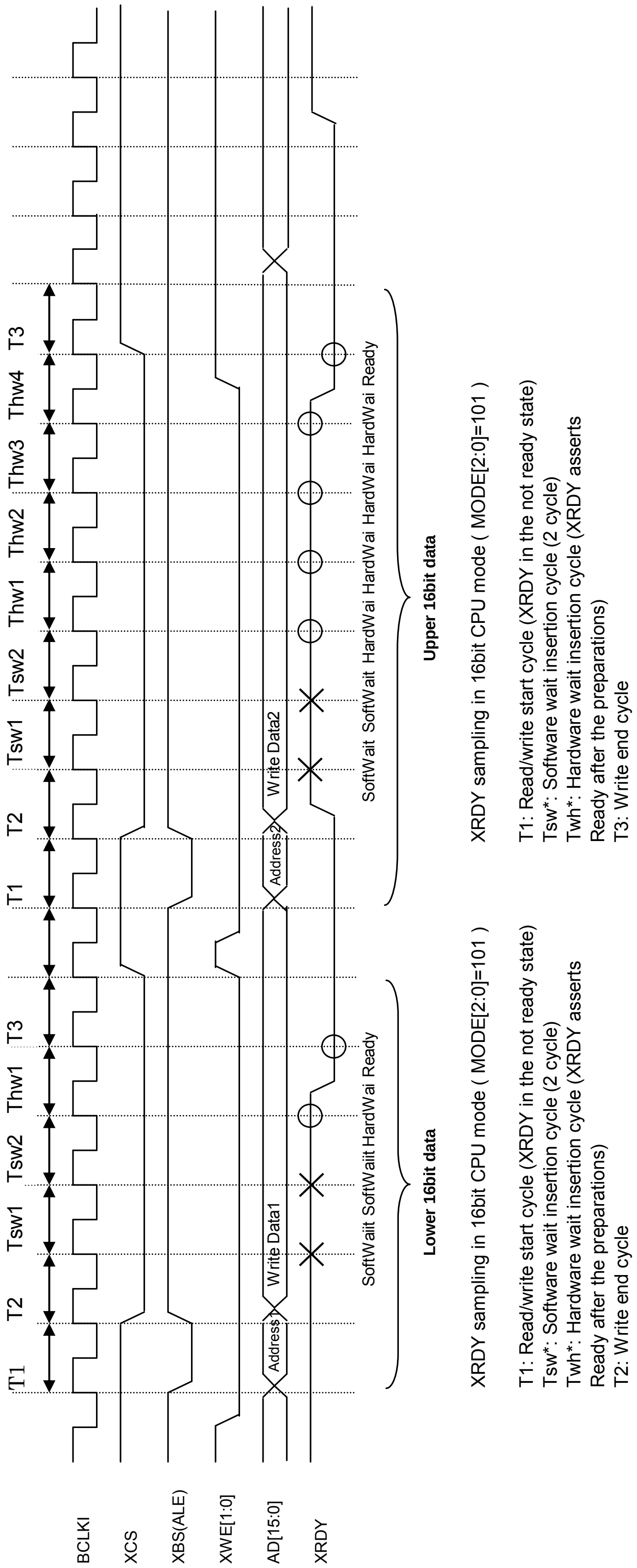
13.3.19 CPU write timing diagram in 16bit CPU mode (Normally Not Ready Mode)



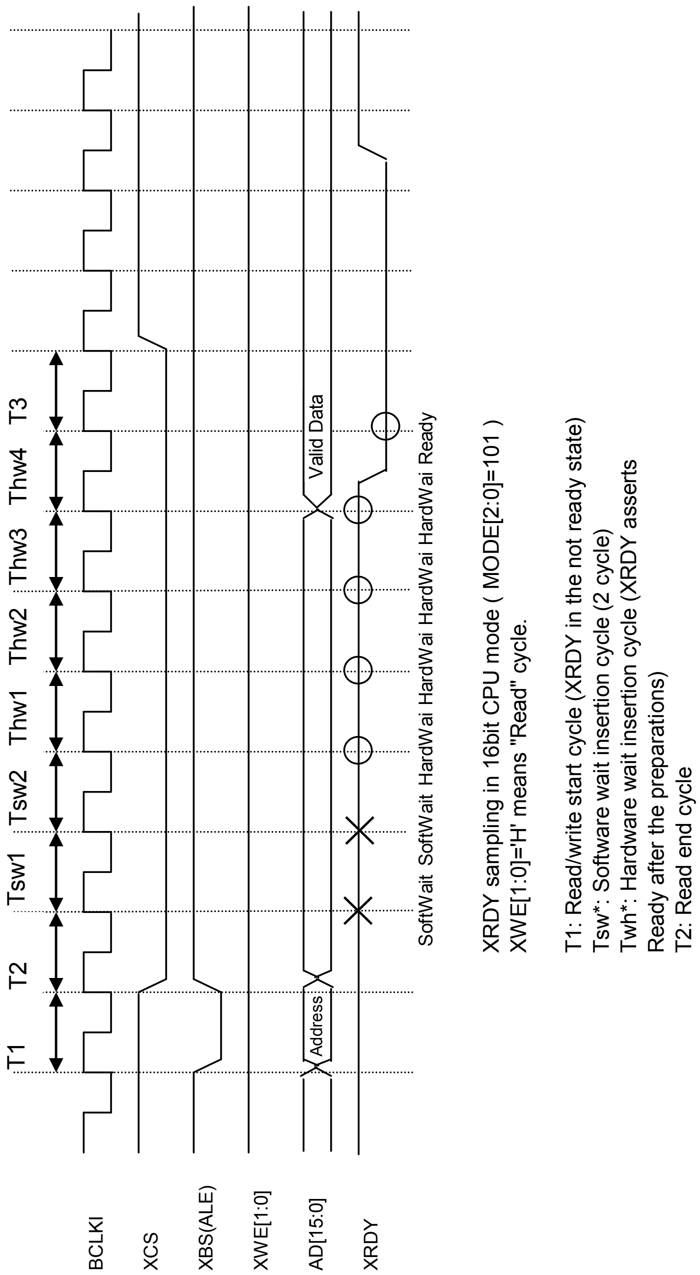
13.3.20 CPU read timing diagram in 16bit CPU mode (Normally Not Ready Mode)



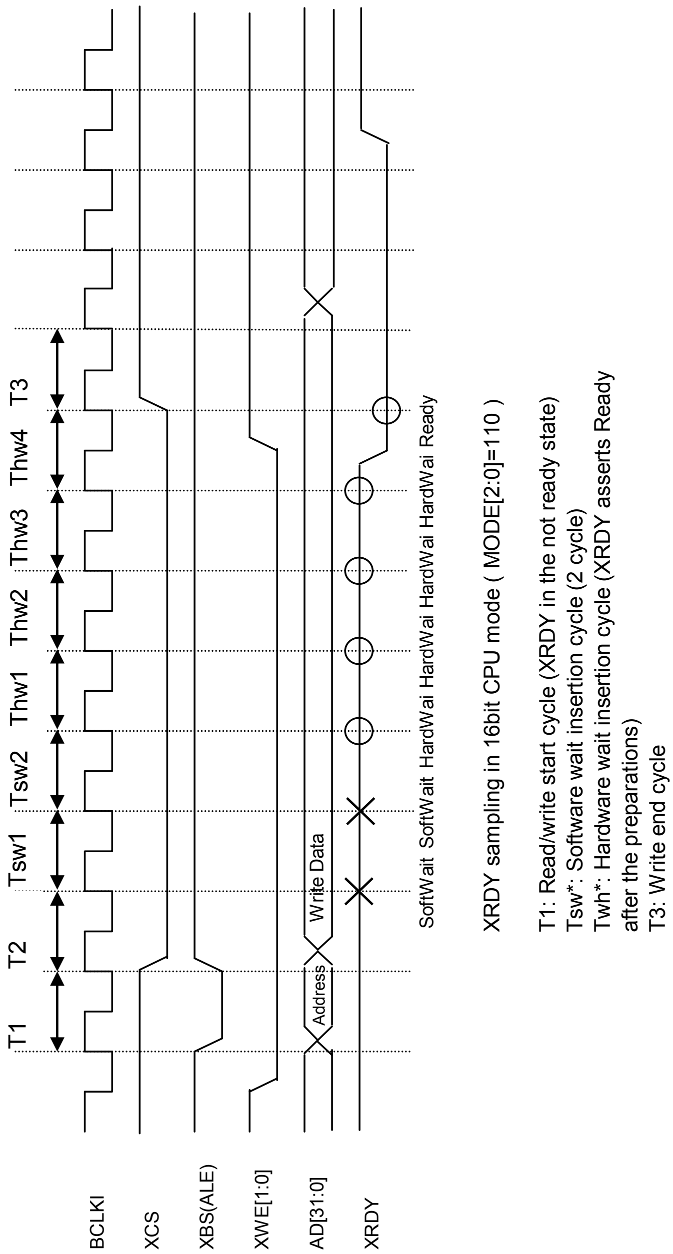
13.3.21 CPU write timing diagram in 16bit AD-MUX CPU mode (Normally Not Ready Mode)



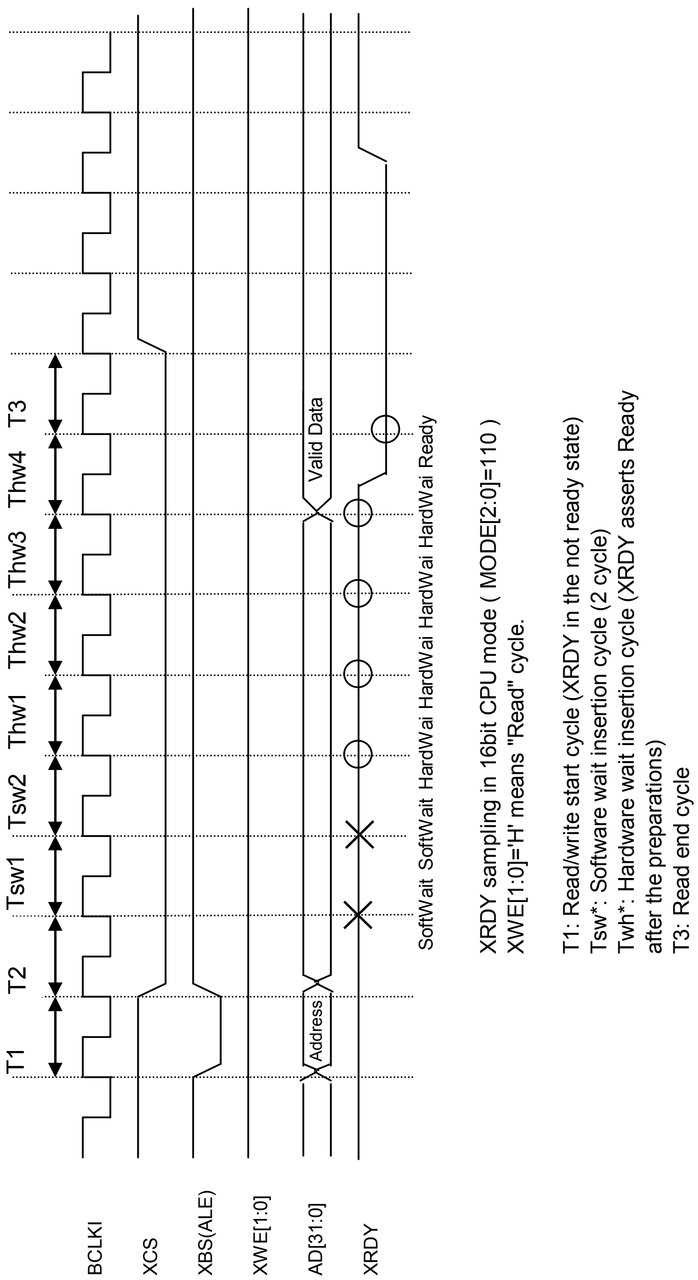
13.3.22 CPU read timing diagram in 16bit AD-MUX CPU mode (Normally Not Ready Mode)



13.3.23 CPU write timing diagram in 32bit AD-MUX CPU mode (Normally Not Ready Mode)



13.3.24 CPU read timing diagram in 32bit AD-MUX CPU mode (Normally Not Ready Mode)



14 ELECTRICAL CHARACTERISTICS

14.1 Introduction

The values in this chapter are the final specification for LIME.

14.2 Maximum Rating

Maximum Rating

Parameter	Symbol	Maximum rating	Unit
Power supply voltage	V_{DDL} *1 V_{DDH}	$-0.5 < V_{DDL} < 2.5$ $-0.5 < V_{DDH} < 4.0$	V
Input voltage	V_I	$-0.5 < V_I < V_{DDH}+0.5$ (<4.0)	V
Output current	I_O	±13	mA
Ambient for storage temperature	TST	-55 < TST < +125	°C

*1 Includes PLL power supply

<Notes>

- Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc) in excess of absolute maximum ratings. Do not exceed these ratings.
- Do not directly connect output pins or bidirectional pins of IC products to each other or VDD or VSS to avoid the breakdown of the device. However direct connection of the output pins or bidirectional pins to each other is possible, if the output pins are designed to avoid a conflict in a timing.
- Because semiconductor devices are particularly susceptible to damaged by static electricity, you must take the measure like ground all fixtures and instruments.
- In CMOS ICs, a latch-up phenomenon is caused when an voltage exceeding Vcc or an voltage below Vss is applied to input or output pins or a voltage exceeding the rating is applied across Vcc and Vss. When a latch-up is caused, the power supply current may be dramatically increased causing resultant thermal break-down of devices. To avoid the latch-up, make sure that the voltage does not exceed the maximum rating.

14.3 Recommended Operating Conditions

14.3.1 Recommended operating conditions

Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Supply voltage	V_{DDL} *1 V_{DDH}	1.65 3.0	1.8 3.3	1.95 3.6	V
Input voltage (High level)	V_{IH}	2.0		V_{DDH}+0.3	V
Input voltage (low level)	V_{IL}	−0.3		0.8	V
Ambient temperature for operation	TA	-40		85	°C

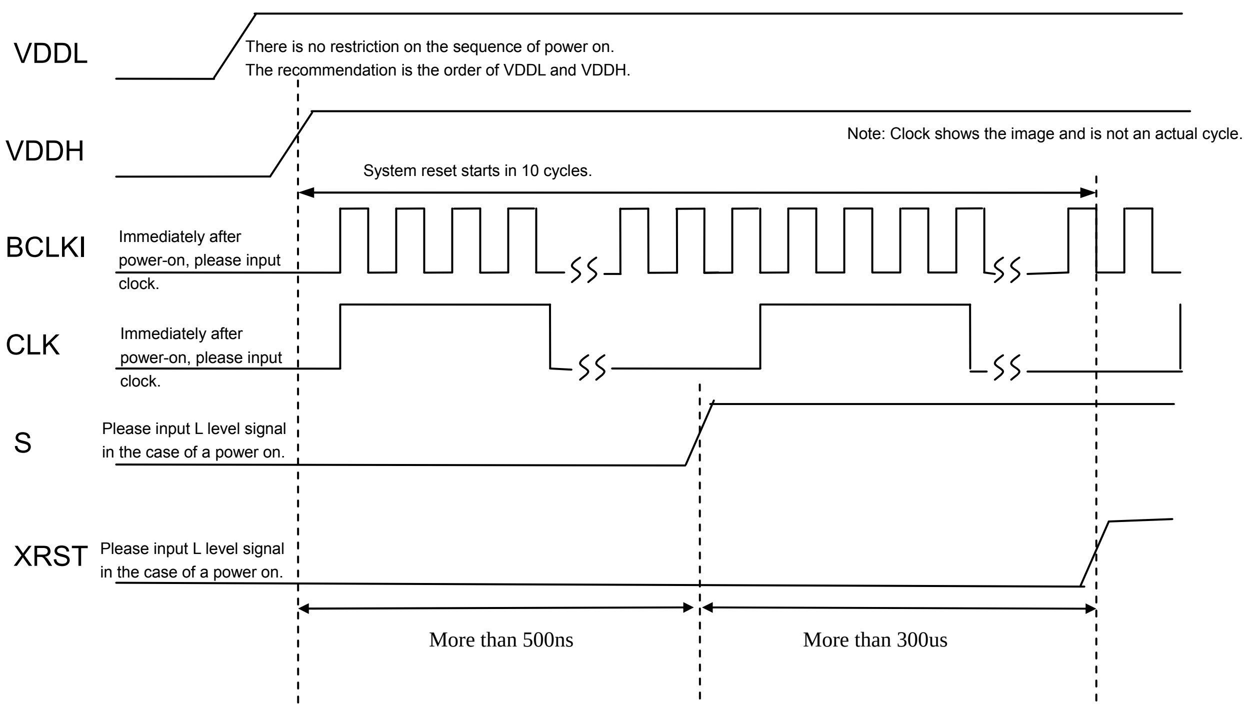
*1 Includes PLL power supply

<Note>

- Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges. Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the manual. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

14.3.2 Note at power-on

- There is no restriction on the sequence of power-on/power-off between V_{DDL} and V_{DDH}. However, do not apply only V_{DDH} for more than a few seconds.
- Do not input HSYNC and VSYNC signals when the power supply voltage is not applied. (See the input voltage item in ***Maximum rating***.)
- Immediately after power-on, please reset immediately because CMOS IC is in an unstable state.
  1) Immediately after power-on, input the "Low" level to the S and XRST pins.
  2) Immediately after power-on, input clock to the BCLKI pin. It is necessary to input 10 clk or more in order that "Low" level signal reach to the whole internal circuit completely.
  3) Immediately after power-on, input clock to the CLK pin.
  It is necessary to supply the stable clock before S pin is changed "Low" level to "High" level in order that PLL is oscillated stably.
- There is a reset sequences as described below.



Immediately after power-on, input the "Low" level to the S and XRST pins. After 500ns or more, input the "High" level to S pin. After the S pin is set to "High" level, input the "Low" level to the XRST pin for 300us or more.
Immediately after power-on, input clock to the BCLKI and CLK pins.

14.4 DC Characteristics

14.4.1 DC Characteristics

Measuring condition: V_{DDL} = 1.8 ± 1.5 V, V_{DDH} = 3.3 ± 0.3 V, V_{SS} = 0.0 V, Ta = -40 to +85°C

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Output voltage ("High" level)	V_{OH}	I_{OH}=-100uA	V_{DDH}-0.2		V_{DDH}	V
Output voltage ("Low" level)	V_{OL}	I_{OL}=100uA	0.0		0.2	V
Output current ("High" level)	--	V_{DDH}=3.3V±0.3V	(*1)			mA
Output current ("Low" level)	--	V_{DDH}=3.3V±0.3V	(*1)			mA
Input leakage current	IL				±5	µA
Pin capacitance	C				16	pF

*1: Please refer "V-I characteristics diagram".
L Type: Output characteristics of MD0-31 and MDQM0-3 pins
M Type: Output characteristics of pins other than signals indicated by L type and H type
H Type: Output characteristics of XINT, DREQ, XRDY pins

14.4.2 V-I characteristics diagram

Condition MIN: Process=Slow, Ta=85°C, V_{DD}=3.0V
TYP: Process=Typical, Ta=25°C, V_{DD}=3.3V
MAX: Process=Fast, Ta=-40°C, V_{DD}=3.6V

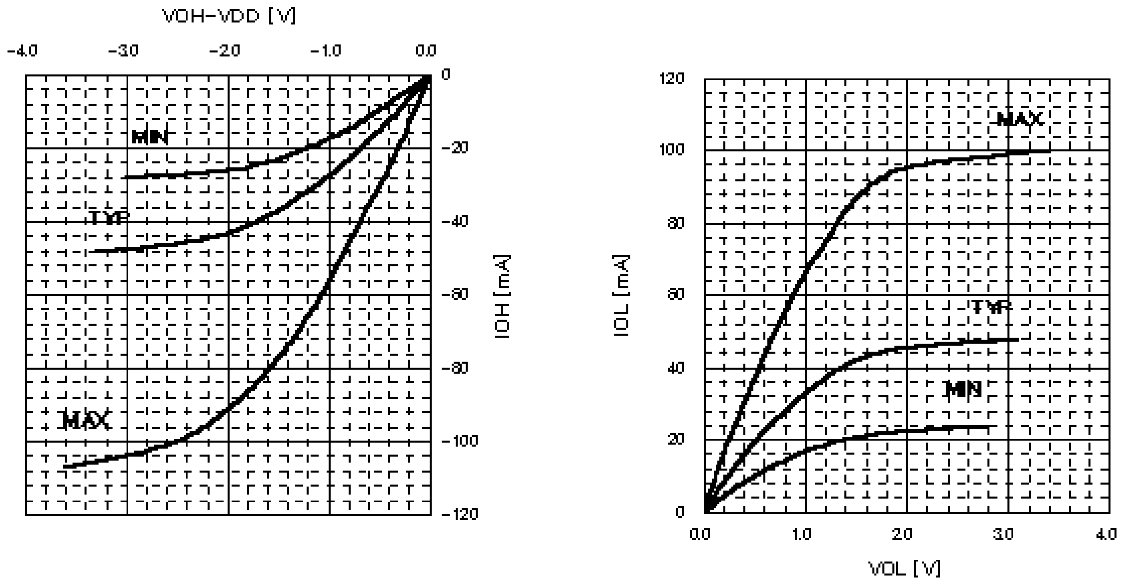


Fig. V-I characteristics L, M type

Condition MIN: Process=Slow, Ta=85°C, V_{DD}=3.0V
TYP: Process=Typical, Ta=25°C, V_{DD}=3.3V
MAX: Process=Fast, Ta=-40°C, V_{DD}=3.6V

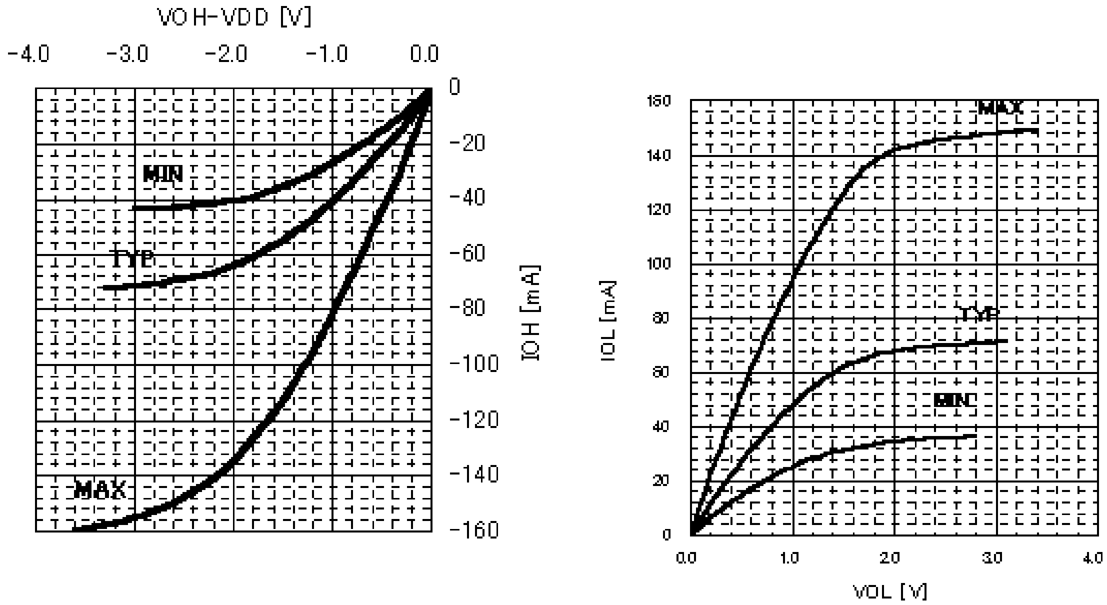


Fig. V-I characteristics H type

14.5 AC Characteristics

14.5.1 Host interface

Clock

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
BCLKI frequency	f_{BCLKI}				66	MHz
BCLKI H-width	t_{HBCLKI}		1			ns
BCLKI L-width	t_{LBCLKI}		1			ns

Host interface signals based on BCLK

(Operating condition: external load = 20 pF)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Address set up time	t_{ADS}		3.0			ns
Address hold time	t_{ADH}		0.0			ns
XBS Set up time	t_{BSS}		3.0			ns
XBS Hold time	t_{BSH}		0.0			ns
XCS Set up time	t_{CSS}		3.0			ns
XCS Hold time	t_{CSH}		0.0			ns
XRD Set up time	t_{RDS}		3.0			ns
XRD Hold time	t_{RDH}		0.0			ns
XWE Set up time	t_{WES}		5.0			ns
XWE Hold time	t_{WEH}		0.0			ns
Write data set up time	t_{WDS}		3.5			ns
Write data hold time	t_{WDH}		0.0			ns
DTACK Set up time	t_{DAKS}		3.0			ns
DTACK Hold time	t_{DAKH}		0.0			ns
DRACK Set up time	t_{DRKS}		3.0			ns
DRACK Hold time	t_{DRKH}		0.0			ns
Read data delay time (for XRD)	t_{RDDZ}		4.5		10.5	ns
Read data delay time	t_{RDD}	*2	4.5		9.5	ns
XRDY Delay time (for XCS)	t_{RDYDZ}		3.5		7.0	ns
XRDY Delay time	t_{RDYD}		2.5		6.0	ns
XINT Delay time	t_{INTD}		3.0		7.0	ns
DREQ Delay time	t_{DQRD}		3.5		7.0	ns
MODE Hold time	t_{MODH}	*1			20.0	ns

*1 Hold time required for canceling reset

*2 Valid data is output at assertion of XRDY and is retained until XRD is negated.

Serial Control interface signals

TBD

14.5.2 I²C Interface

I²C bus timing

symbol			MIN	MAX	unit
T_{S2SDAI}	SDA(I) setup time	standard	250		ns
		high-speed	100		ns
T_{H2SDAI}	SCL(I) hold time	standard	0		ns
		high-speed	0		ns
T_{CSCLI}	SCL(I) cycle time	standard	10.0		us
		high-speed	2.5		us
T_{WHSCLI}	SCL(I) H period	standard	4.0		us
		high-speed	0.6		us
T_{WLSCLI}	SCL(I) L period	standard	4.7		us
		high-speed	1.3		us
T_{CSCLO}	SCL(O) cycle time	standard	2*m+2(*2)		PCLK*1
		high-speed	int(1.5*m)+2(*2)		PCLK*1
T_{WHSCLO}	SCL(O) H period	standard	m+2(*2)		PCLK*1
		high-speed	int(0.5*m)+2(*2)		PCLK*1
T_{WLSCLO}	SCL(O) L period	standard	m(*2)		PCLK*1
		high-speed	m(*2)		PCLK*1
T_{W2SCLI}	SCL(I) setup time	standard	4.0		us
		high-speed	0.6		us
T_{H2SCLI}	SCL(I) hold time	standard	4.7		us
		high-speed	1.3		us
T_{WBFI}	bus free time	standard	4.7		us
		hirh-speed	1.3		us
T_{S2SCLO}	SCL(O) set up time	standard	m+2(*2)		PCLK*1
		high-speed	int(0.5*m)+2(*2)		PCLK*1
T_{H2SCLO}	SCL(O) hold time	standard	m-2(*2)		PCLK*1
		high-speed	int(0.5*m)-2(*2)		PCLK*1
T_{H2SDAO}	SDA(O) hold time		5		PCLK*1

*1 PCLK is an internal clock of I2C module. (16.6MHz)
*2 Refer to the clock control register (CCR) for the value of m.

14.5.3 Video interface

(1) Clock

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
CLK Frequency	f_{CLK}			14.318		MHz
CLK H-width	t_{HCLK}		25			ns
CLK L-width	t_{LCLK}		25			ns
DCLKI Frequency	f_{DCLKI}				80	MHz
DCLKI H-width	t_{HDCLKI}		5			ns
DCLKI L-width	t_{LDCLKI}		5			ns
DCLKO frequency	f_{DCLKO}				80	MHz

(2) Input signals

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
HSYNC Input pulse width	$t_{WHSYNC0}$	*1	3			clock
	$t_{WHSYNC1}$	*2	3			clock
HSYNC Input setup time	t_{SHSYNC}	*2	6			ns
HSYNC Input hold time	t_{HHSYNC}	*2	1			ns
VSYNC Input pulse width	$t_{WHSYNC1}$		1			HSYNC 1 cycle

*1 Applied only in PLL synchronization mode (CKS=0), reference clock output from internal PLL (cycle = 1/14*fCLK)

*2 Applied only in DCLKI synchronization mode (CKS=1), reference clock = DCLKI

(3) Output signals (standard)

This definition is applied for followig mode operations

1) single display & non-inverting DCLKO
(MDen=0) & (DCKinv=0)

2) dual display & single-edge & non-inverting DCLKO
(MDen=1) & (DCKed=0) & (DCKinv=0)

(Operating condition: external load = 20 pF)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
RGB Output delay time 1	T_{RGB1}		2		9	ns
DISPE Output delay time 1	t_{DEO1}		2		9	ns
HSYNC Output delay time 1	$t_{DHSYNC1}$		2		9	ns
VSYNC Output delay time 1	$t_{DVSYNC1}$		2		9	ns
CSYNC Output delay time 1	$t_{DCSYNC1}$		2		10	ns
GV Output delay time 1	t_{DGV1}		1.5		9	ns

(4) Output signals (inverting)

This definition is applied for followig mode operations

1) single display & inverting DCLKO
(MDen=0) & (DCKinv=1)

2) dual display & single-edge & inverting DCLKO
(MDen=1) & (DCKed=0) & (DCKinv=1)

(Operating condition: external load = 20 pF)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
RGB Output delay time 2	T_{RGB2}		2		9	ns
DISPE Output delay time 2	t_{DEO2}		2		9	ns
HSYNC Output delay time 2	$t_{DHSYNC2}$		2		9	ns
VSYNC Output delay time 2	$t_{DVSYNC2}$		2		9	ns
CSYNC Output delay time 2	$t_{DCSYNC2}$		2		10	ns
GV Output delay time 2	t_{DGV2}		1.5		9	ns

(5) Output signals (bi-edge)

This definition is applied for followig mode operations

dual display & bi-edge
(MDen=1) & (DCKed=1)

(Operating condition: external load = 20 pF)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
RGB Output delay time 3	T_{RGB3}		1.5		9	ns
DISPE Output delay time 3	t_{DEO3}		1.5		9	ns
HSYNC Output delay time 3	$t_{DHSYNC3}$		1.5		9	ns
VSYNC Output delay time 3	$t_{DVSYNC3}$		1.5		9	ns
CSYNC Output delay time 3	$t_{DCSYNC3}$		1.5		10	ns
GV Output delay time 3	t_{DGV3}		1.5		9	ns
RGB Output delay time 4	T_{RGB4}		1.5		9	ns
DISPE Output delay time 4	t_{DEO4}		1.5		9	ns
HSYNC Output delay time 4	$t_{DHSYNC4}$		1.5		9	ns
VSYNC Output delay time 4	$t_{DVSYNC4}$		1.5		9	ns
CSYNC Output delay time 4	$t_{DCSYNC4}$		1.5		10	ns
GV Output delay time 4	t_{DGV4}		1.5		9	ns

14.5.4 Video capture interface

clock

parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
CCLK (RGBCLK) frequency	f_{CCLK}			27*1		MHz
CCLK (RGBCLK) H-width	t_{HCCLKI}		5			ns
CCLK (RGBCLK) L-width	t_{LCCLKI}		5			ns

*1: Max buffer size of horizontal direction is 840.

Input signals

parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
VI setup time	t_{SVI}		6			ns
VI hold time	t_{HVI}		0			ns
HSYNCI setup time	t_{SHSI}		6			ns
HSYNCI hold time	t_{HHSI}		0			ns
VSYNCI setup time	t_{SVSI}		6			ns
VSYNCI hold time	t_{HVSI}		0			ns
RI setup time	t_{SRI}		6			ns
RI hold time	t_{HRI}		0			ns
GI setup time	t_{SGI}		6			ns
GI hold time	t_{HGI}		0			ns
BI setup time	t_{SBI}		6			ns
BI hold time	t_{HBI}		0			ns

14.5.5 Graphics memory interface

An assumed external capacitance

Parameter	An assumed external capacitance			Unit
	Min	Typ	Max	
Board pattern	5.0		15.0	pF
SDRAM (CLK)	2.5		4.0	pF
SDRAM (D)	4.0		6.5	pF
SDRAM (A, DQM)	2.5		5.0	pF

Clock

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
MCLKO Frequency	f_{MCLKO}				*1	MHz
MCLKO H-width	t_{HMCLKO}		1.0			ns
MCLKO L-width	t_{LMCLKO}		1.0			ns
MCLKI Frequency	f_{MCLKI}				*1	MHz
MCLKI H-width	t_{HMCLKI}		1.0			ns
MCLKI L-width	t_{LMCLKI}		1.0			ns

*1 For the bus-asynchronous mode, the frequency is 1/3 of the oscillation frequency of the internal PLL. For the bus-synchronous mode, the frequency is the same as the frequency of BCLKI.

Input signals

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
MD Input data setup time	t_{MDIDS}	*2	2.0			ns
MD Input data hold time	t_{MDIDH}	*2	0.7			ns

*2 It means against MCLKI.

There are some cases regarding AC specifications of output signals.

The following tables shows typical twelve cases of external SDFAM capacitance.

(1) External SDRAM capacitance case 1

External SDRAM capacitance

SDRAM x1	Total capacitance	Unit
MCLKO	9.8pF (DRAM CLK 2.5pF, Board pattern 5pF)	pF
MA,MRAS,MCAS,MWE	7.5pF (DRAM A.DQM 2.5pF, Board pattern 5pF)	pF
MD,DQM	9.0pF (DRAM D 4pF, Board pattern 5pF)	pF

Output signals

Parameter	Symbol	Condition	Rating *1			Unit
			Min.	Typ.	Max.	
MCLKI signal delay time against MCLKO	t_{DID}		0		4.2	ns
MA, MRAS, MCAS, MWE Access time	t_{MAD}		1.0		5.0	ns
MDQM Access time	t_{MDQMD}		1.1		5.4	ns
MD Output access time	t_{MDOD}		1.1		5.4	ns

(2) External SDRAM capacitance case 2

External SDRAM capacitance

SDRAM x1	Total capacitance	Unit
MCLKO	24.8pF (DRAM CLK 4.0pF, Board pattern 15pF)	pF
MA,MRAS,MCAS,MWE	20.0pF (DRAM A.DQM 5pF, Board pattern 15pF)	pF
MD,DQM	21.5pF (DRAM D 6.5pF, Board pattern 15pF)	pF

Output signals

Parameter	Symbol	Condition	Rating *1			Unit
			Min.	Typ.	Max.	
MCLKI signal delay time against MCLKO	t_{DID}		0		3.5	ns
MA, MRAS, MCAS, MWE Access time	t_{MAD}		1.0		5.2	ns
MDQM Access time	t_{MDQMD}		1.2		5.5	ns
MD Output access time	t_{MDOD}		1.2		5.5	ns

(3) External SDRAM capacitance case 3

External SDRAM capacitance

SDRAM x2	Total capacitance	Unit
MCLKO	12.3pF (DRAM CLK 2.5pF x2, Board pattern 5pF)	pF
MA,MRAS,MCAS,MWE	10.0pF (DRAM A.DQM 2.5pF x2, Board pattern 5pF)	pF
MD,DQM	9.0pF (DRAM D 4pF, Board pattern 5pF)	pF

Output signals

Parameter	Symbol	Condition	Rating *1			Unit
			Min.	Typ.	Max.	
MCLKI signal delay time against MCLKO	t_{DID}		0		4.1	ns
MA, MRAS, MCAS, MWE Access time	t_{MAD}		1.0		5.0	ns
MDQM Access time	t_{MDQMD}		1.1		5.2	ns
MD Output access time	t_{MDOD}		1.1		5.2	ns

(4) External SDRAM capacitance case 4

External SDRAM capacitance

SDRAM x2	Total capacitance	Unit
MCLKO	28.8pF (DRAM CLK 4.0pF x2, Board pattern 15pF)	pF
MA,MRAS,MCAS,MWE	25.0pF (DRAM A.DQM 5pF x2, Board pattern 15pF)	pF
MD,DQM	21.5pF (DRAM D 6.5pF, Board pattern 15pF)	pF

Output signals

Parameter	Symbol	Condition	Rating *1			Unit
			Min.	Typ.	Max.	
MCLKI signal delay time against MCLKO	t_{DID}		0		3.4	ns
MA, MRAS, MCAS, MWE Access time	t_{MAD}		1.1		5.4	ns
MDQM Access time	t_{MDQMD}		1.1		5.5	ns
MD Output access time	t_{MDOD}		1.1		5.5	ns

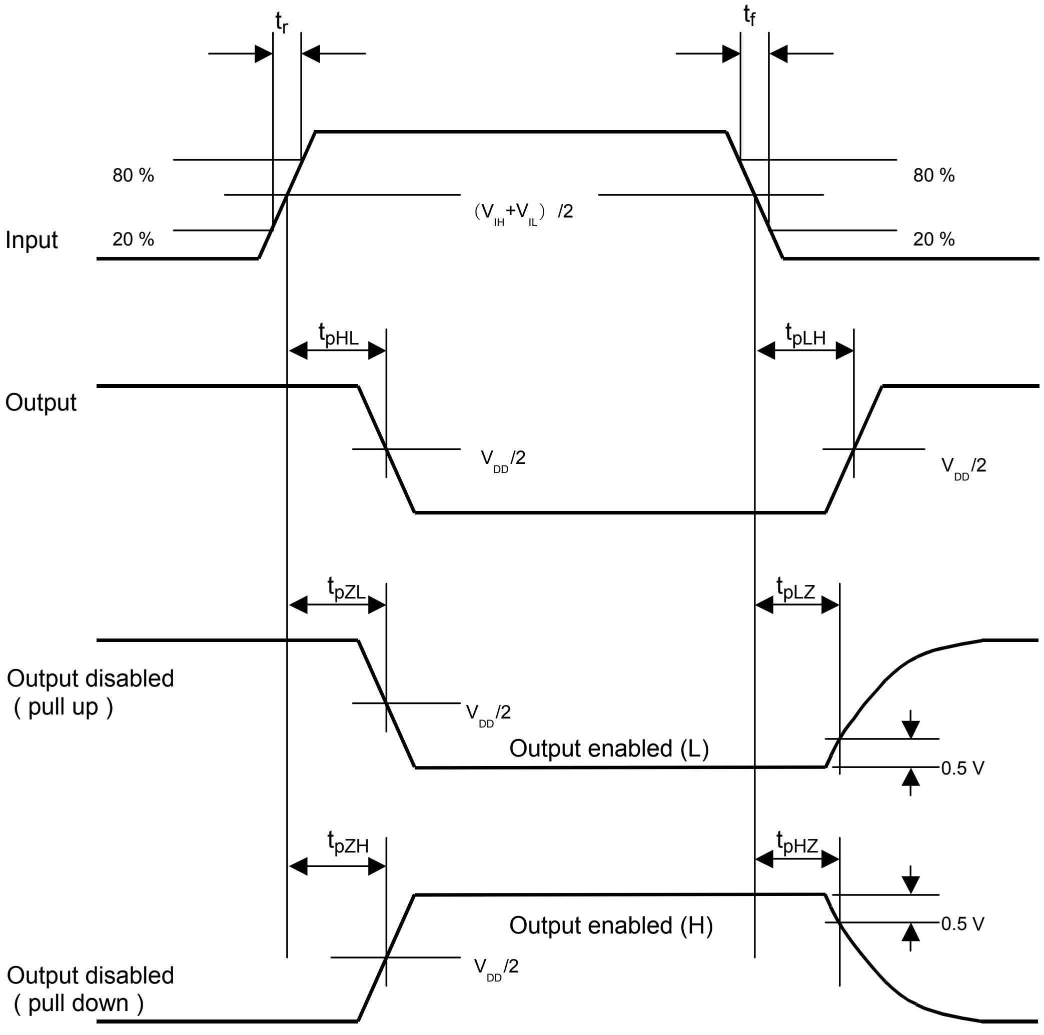
14.5.6 PLL specifications

Parameter	Rating	Description
Input frequency (typ.)	14.31818 MHz	
Output frequency	400.9090 MHz	× 28
Duty ratio	101.6 to 93.0%	H/L Pulse width ratio of PLL output
Jitter	60 to -60 ps	Frequency tolerant of two consecutive clock cycles

CLKSEL1	CLKSEL0	Input frequency	Assured operation range (*1)
L	L	13.5 MHz	13.365 to 13.5 MHz
L	H	14.32 MHz	14.177 to 14.32 MHz
H	L	17.73 Hz	17.553 to 17.73 MHz
H	H	33.33 Hz	32.997 to 33.33 MHz

*1 Assured operation input frequency range: Standard value –1%

14.6 AC Characteristics Measuring Conditions



t_r, t_f ≤ 5 ns :**All input signals have to change within 5ns.**

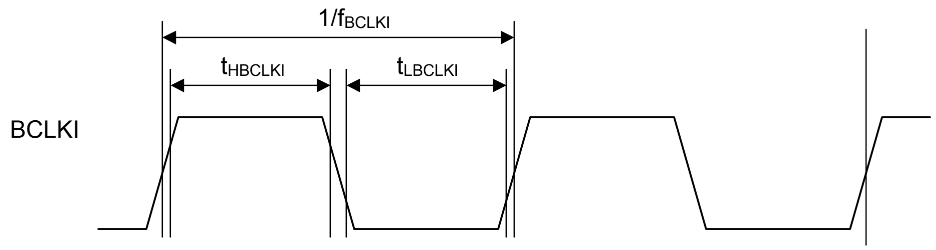
V_{IH}=2.0 V, V_{IL}=0.8V (3.3-V CMOS interface input)

14.7 Timing Diagram

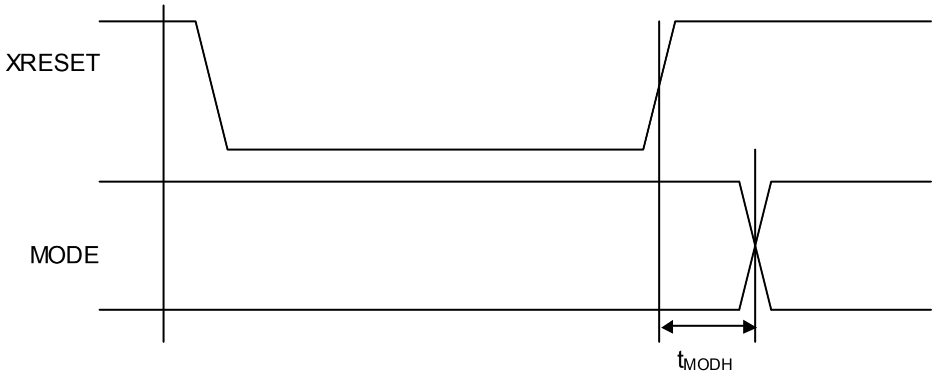
14.7.1 Host interface

Host interface based on BCLKI

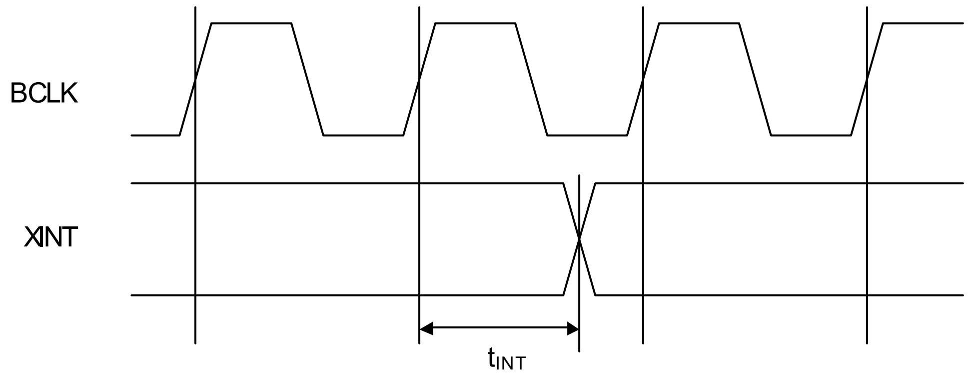
(1)Clock



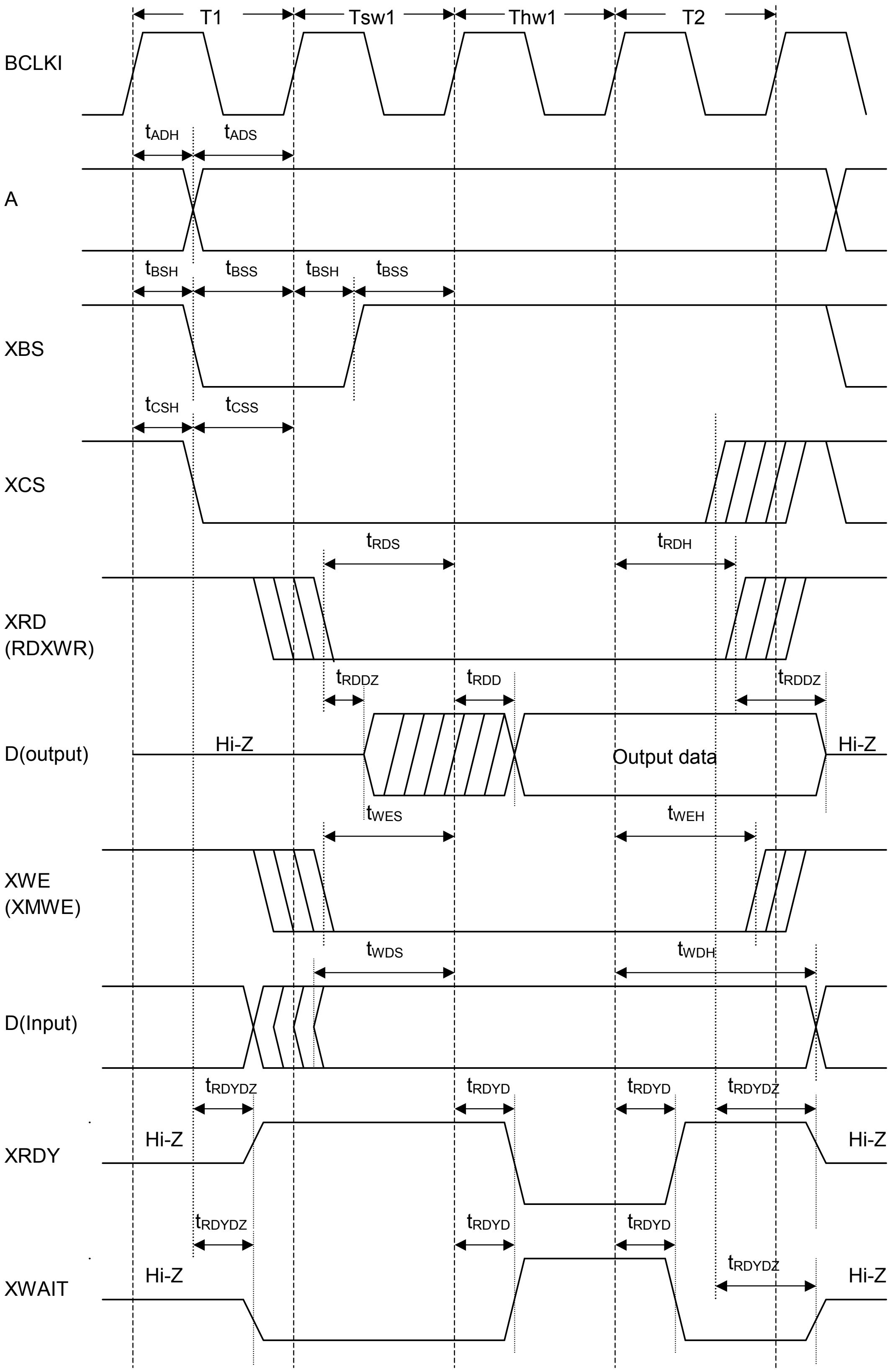
(2)MODE hold time



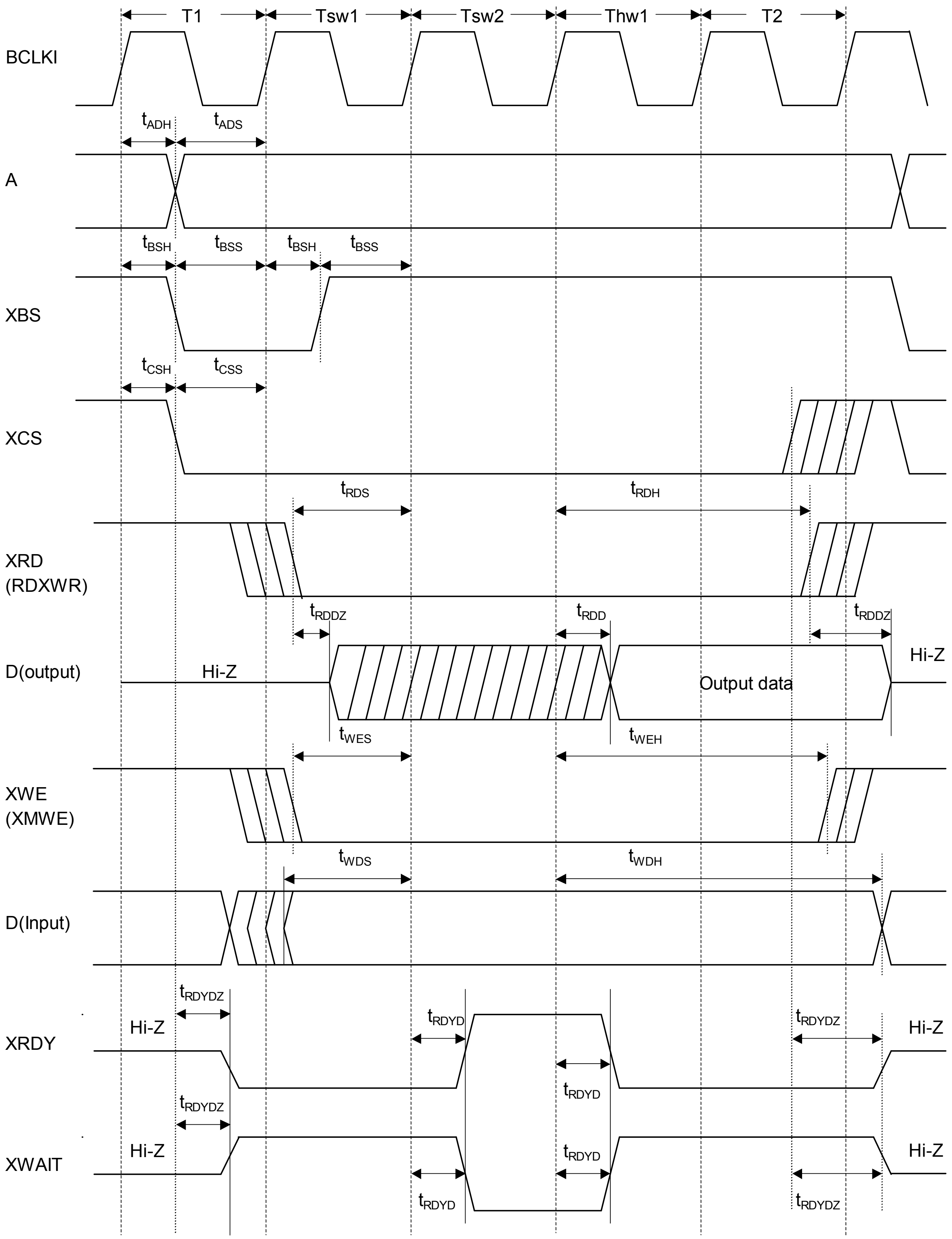
(3)XINT output delay times



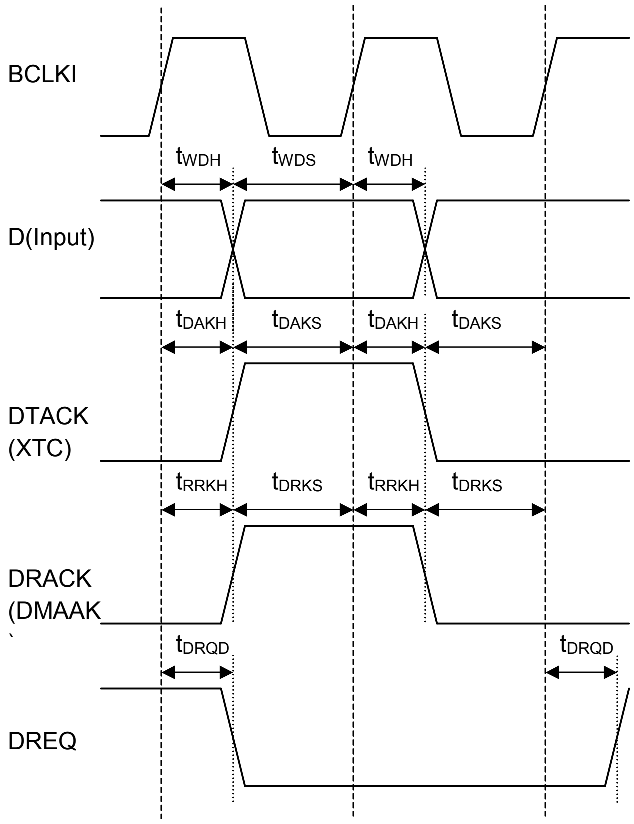
(4)**Host bus AC timing (Normally Not Ready)**



(5)**Host bus AC timing (Normally Ready)**



(6)**DMA AC timing**



*: The above timing diagram for the D pin is that of when a single DMA is used.

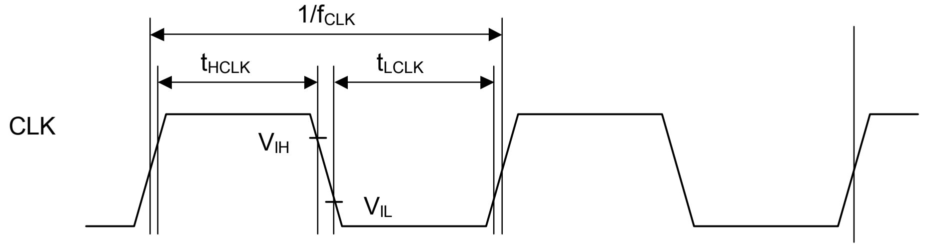
When a dual DMA is used, see the host bus-timing diagram.

Serial Control interface

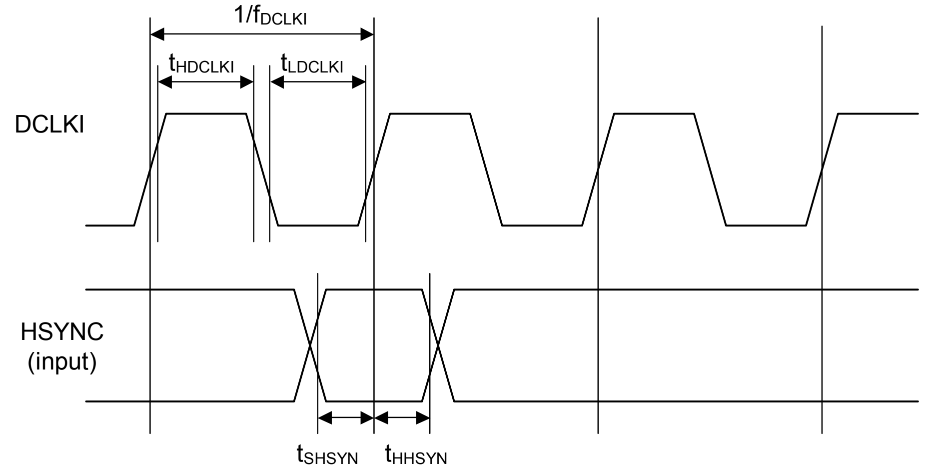
TBD

14.7.2 Video interface

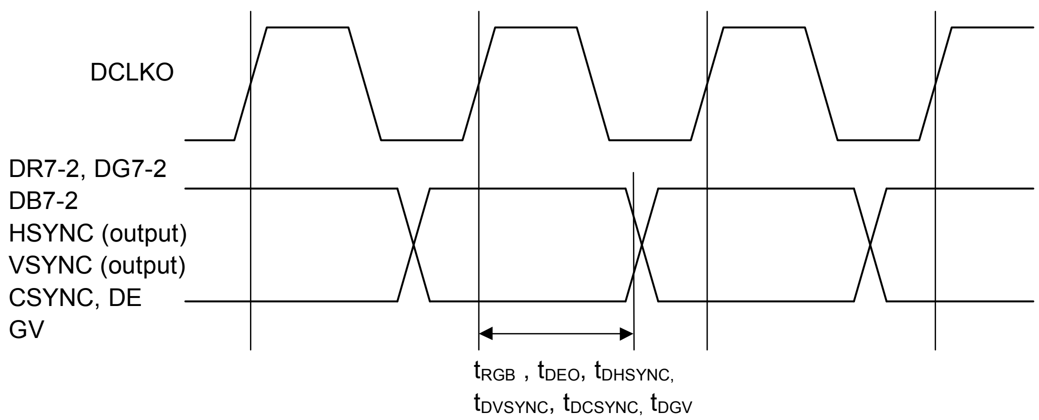
(1) Clock



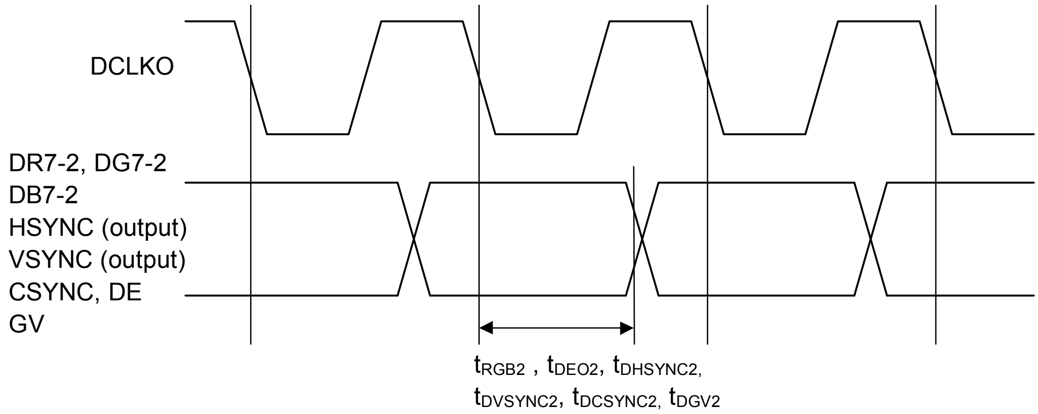
(2) HSYNC signal setup/hold



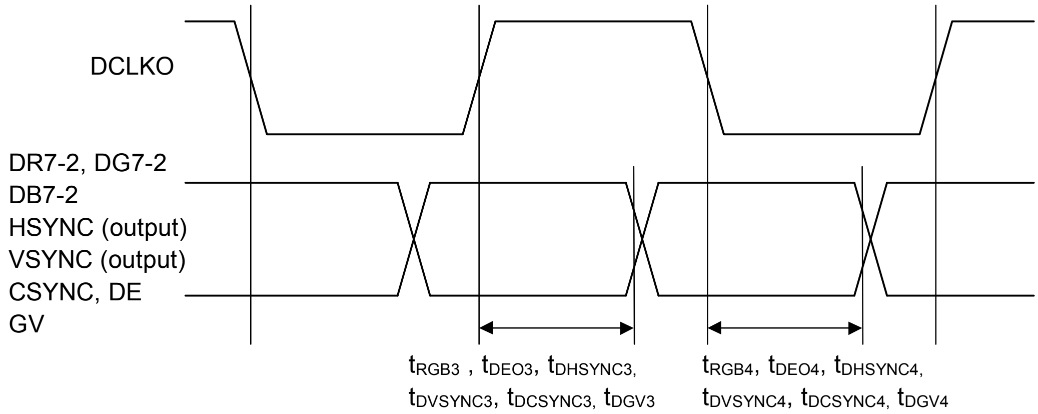
(3) Output signal delay (standard)



(4) Output signal delay (inverted)

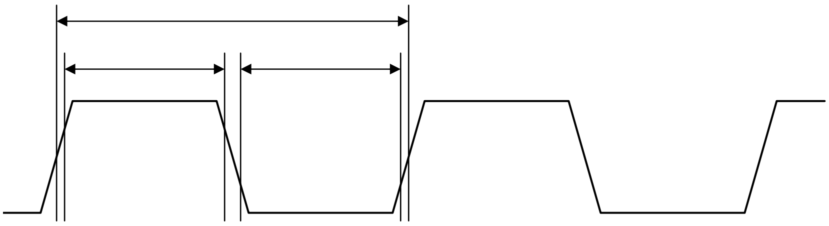


(5) Output signal delay (bi-edge)

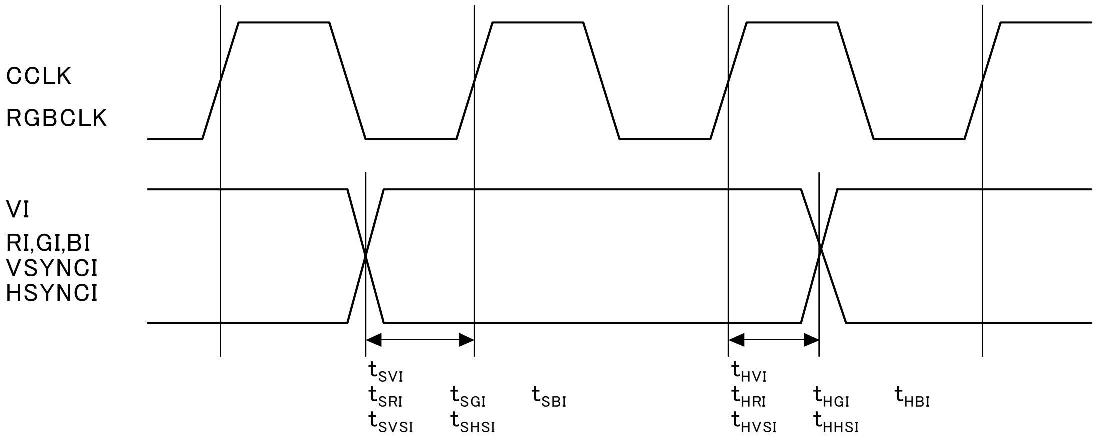


14.7.3 Video capture interface

clock

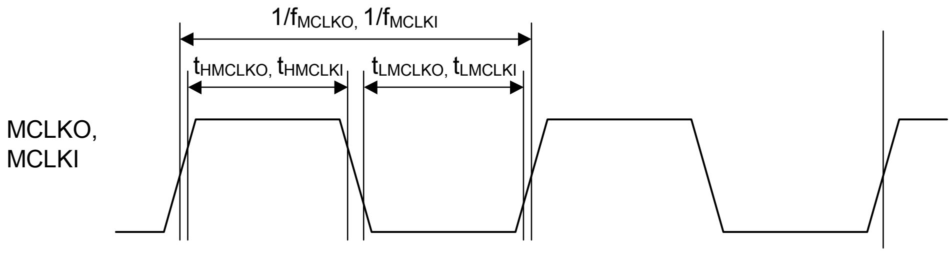


Video input

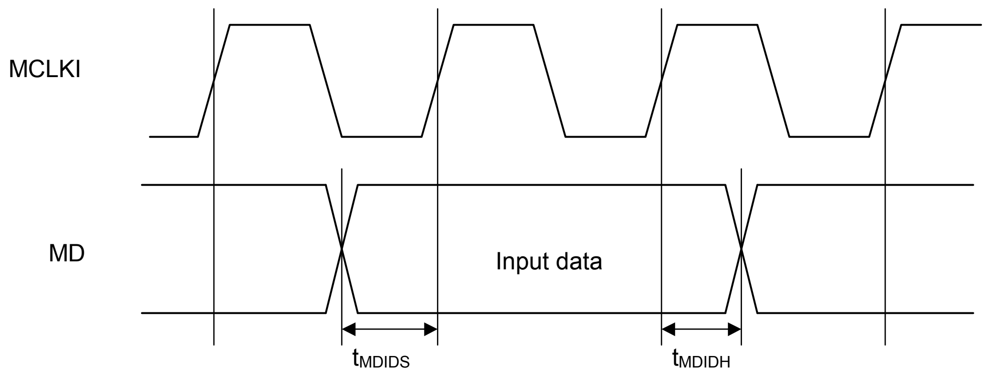


14.7.4 Graphics memory interface

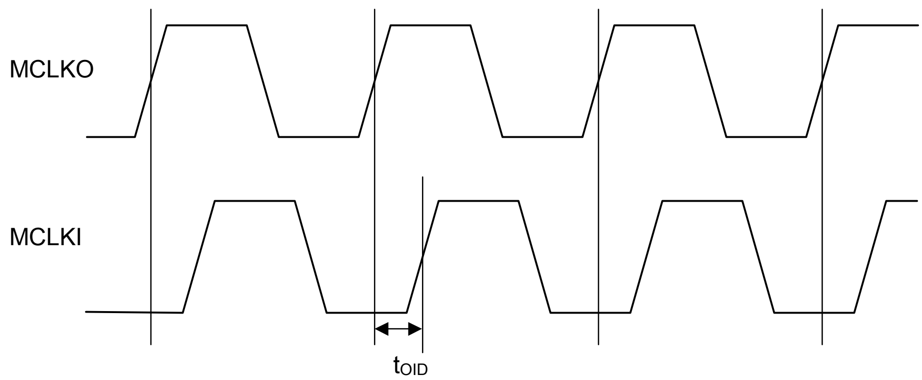
Clock



Input signal setup/hold time



MCLKI signal delay



Output signal delay