

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D $T_C = +25^\circ C$
20V	4.6mΩ @ $V_{GS} = 4.5V$	100A
	8.7mΩ @ $V_{GS} = 2.5V$	80A

Description

This new generation P-Channel Enhancement Mode MOSFET has been designed to minimize $R_{DS(ON)}$ and yet maintain superior switching performance. This device is ideal for use in Notebook battery power management and Loadswitch.

Applications

- Motor Control
- DC-DC Converters
- Power Management

Features

- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- <1.1mm Package Profile – Ideal for Thin Applications
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

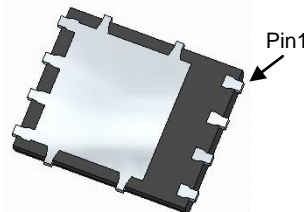
- Case: POWERDI®5060-8
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Weight: 0.097 grams (Approximate)

NEW PRODUCT

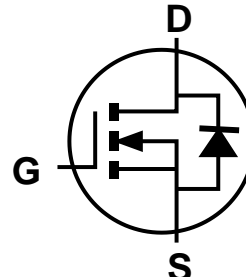
POWERDI®5060-8



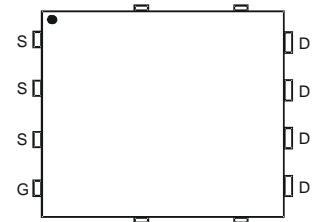
Top View



Bottom View



Internal Schematic



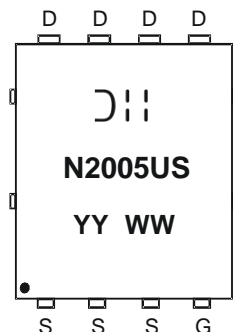
Top View
Pin Configuration


Ordering Information (Note 4)

Part Number	Case	Packaging
DMN2005UPS-13	POWERDI®5060-8	2,500 / Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



 = Manufacturer's Marking
 N2005US = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Last Two Digits of Year (ex: 15= 2015)
 WW = Week Code (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V _{DSS}	20	V
Gate-Source Voltage			V _{GSS}	±12	V
Continuous Drain Current (Note 6) V _{GS} = 10V	Steady State	T _A = +25°C	I _D	20	A
		T _A = +70°C		15	
Continuous Drain Current (Note 6) V _{GS} = 10V	Steady State	T _C = +25°C	I _D	100	A
		T _C = +70°C		88	
Pulsed Drain Current (380µs Pulse, Duty Cycle = 1%)			I _{DM}	150	A
Maximum Continuous Body Diode Forward Current (Mounted on Infinite Heatsink)			I _S	150	A
Avalanche Current (Note 7) L=0.2mH			I _{AS}	36	A
Avalanche Energy (Note 7) L=0.2mH			E _{AS}	133	mJ

Thermal Characteristics

Characteristic			Symbol	Value	Unit
Total Power Dissipation (Note 5)			P _D	1.5	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady state t<10s		R _{θJA}	98	°C/W
				83	
Total Power Dissipation (Note 6)			P _D	3.0	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady state t<10s		R _{θJA}	51	°C/W
				43	
Thermal Resistance, Junction to Case			R _{θJC}	1.5	
Operating and Storage Temperature Range			T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	20	—	—	V	V _{GS} = 0V, I _D = 250µA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	1	µA	V _{DS} = 20V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±12V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(TH)}	0.4	0.7	1.2	V	V _{DS} = V _{GS} , I _D = 250µA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	—	4.6	mΩ	V _{GS} = 4.5V, I _D = 13.5A
		—	—	8.7		V _{GS} = 2.5V, I _D = 13.5A
Diode Forward Voltage	V _{SD}	—	0.8	1.1	V	V _{GS} = 0V, I _S = 27A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	5337	—	pF	V _{DS} = 10V, V _{GS} = 0V, f = 1MHz
Output Capacitance	C _{oss}	—	560	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	505	—	pF	
Gate Resistance	R _g	—	0.7	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge (V _{GS} = 4.5V)	Q _g	—	60	—	nC	V _{DS} = 16V, I _D = 27A
Total Gate Charge (V _{GS} = 10V)	Q _g	—	142	—	nC	
Gate-Source Charge	Q _{gs}	—	7	—	nC	
Gate-Drain Charge	Q _{gd}	—	11	—	nC	
Turn-On Delay Time	t _{D(ON)}	—	12.4	—	ns	V _{GS} = 5V, V _{DS} = 10V, R _G = 4.7Ω, I _D = 13.5A
Turn-On Rise Time	t _R	—	29.8	—	ns	
Turn-Off Delay Time	t _{D(OFF)}	—	117	—	ns	
Turn-Off Fall Time	t _F	—	52	—	ns	
Body Diode Reverse Recovery Time	t _{RR}	—	17.8	—	ns	I _F = 13.5A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q _{RR}	—	8.6	—	nC	I _F = 13.5A, di/dt = 100A/µs

- Notes: 5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1 inch square copper plate.
7. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

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DMN2005UPS

Document number: DS37844 Rev. 2 - 2

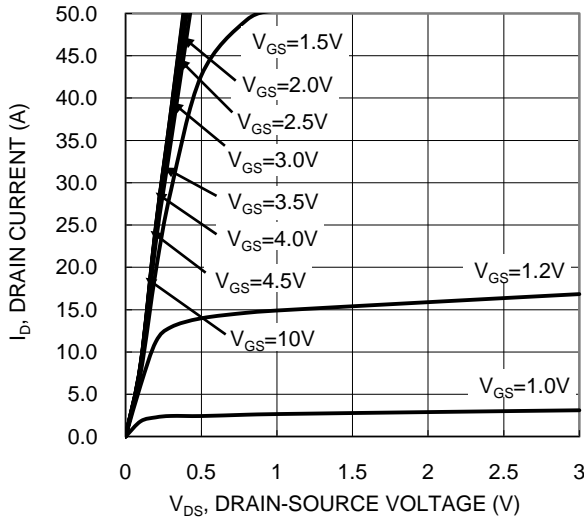


Figure 1. Typical Output Characteristic

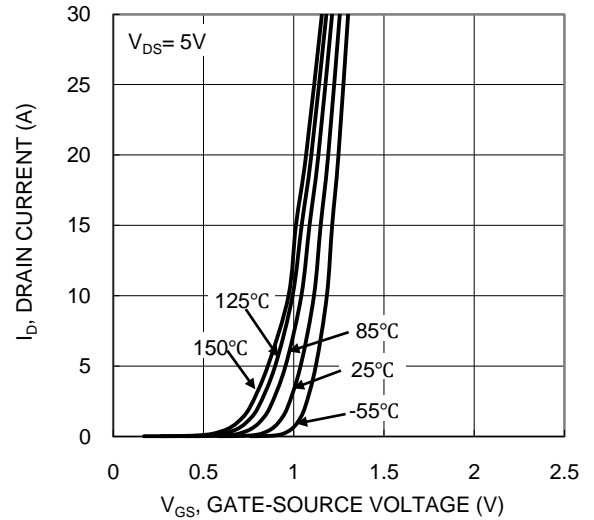


Figure 2. Typical Transfer Characteristic

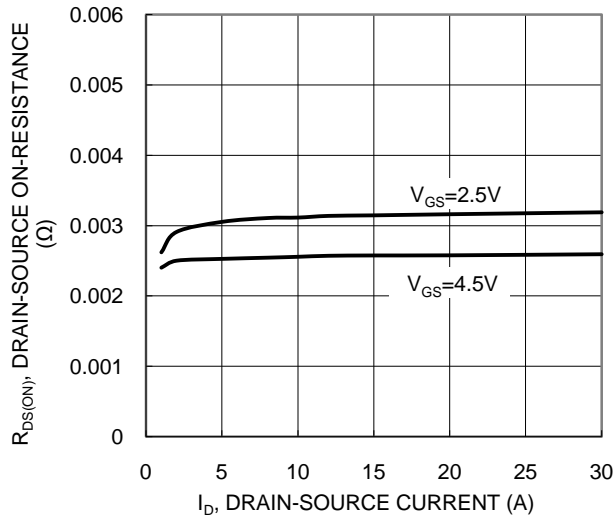


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

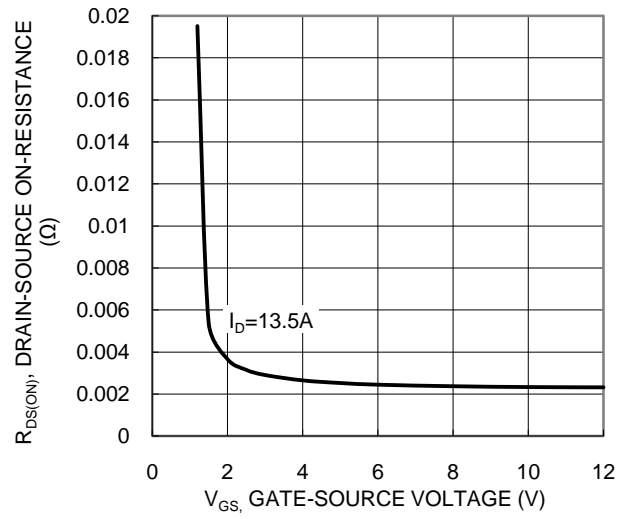


Figure 4. Typical Transfer Characteristic

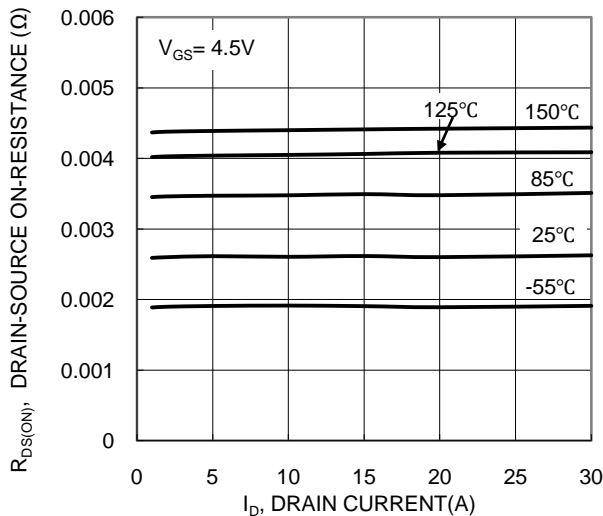


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

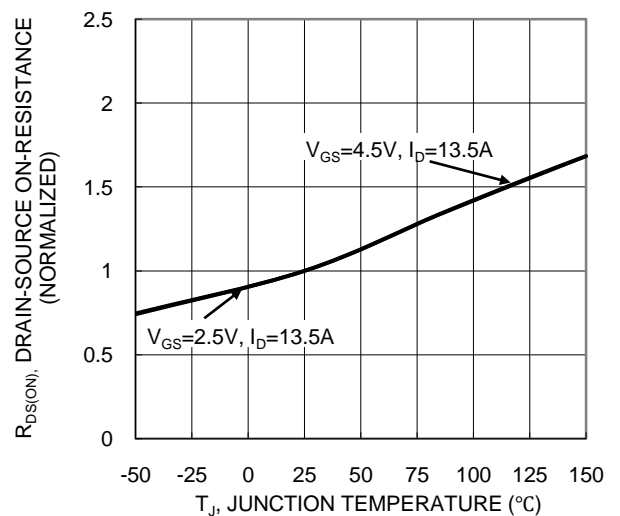


Figure 6. On-Resistance Variation with Junction Temperature

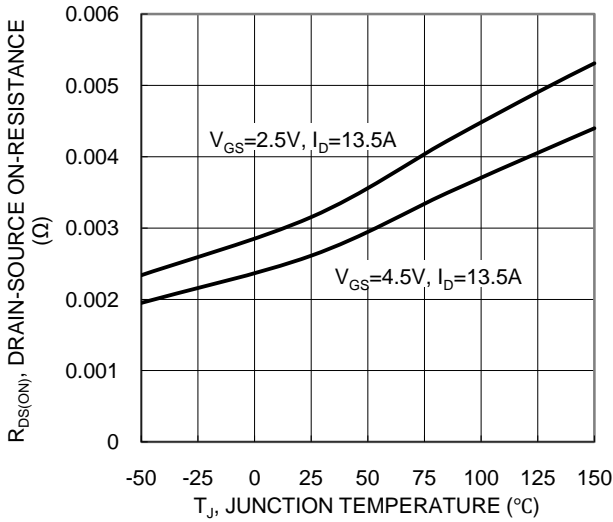


Figure 7. On-Resistance Variation with Junction Temperature

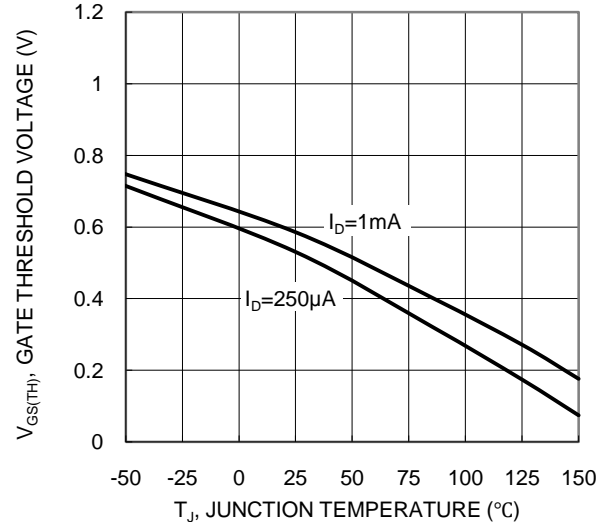


Figure 8. Gate Threshold Variation vs. Junction Temperature

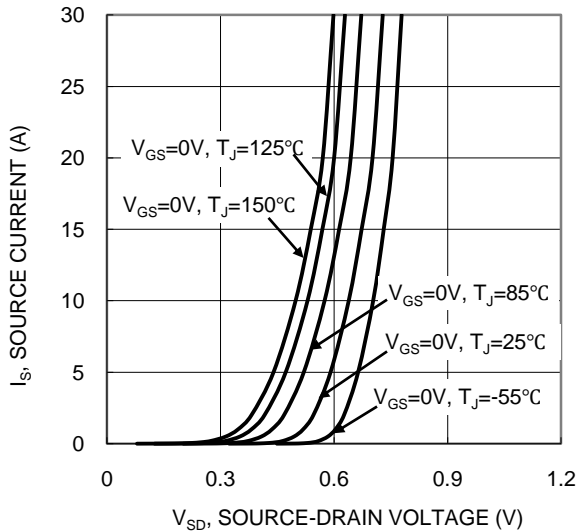


Figure 9. Diode Forward Voltage vs. Current

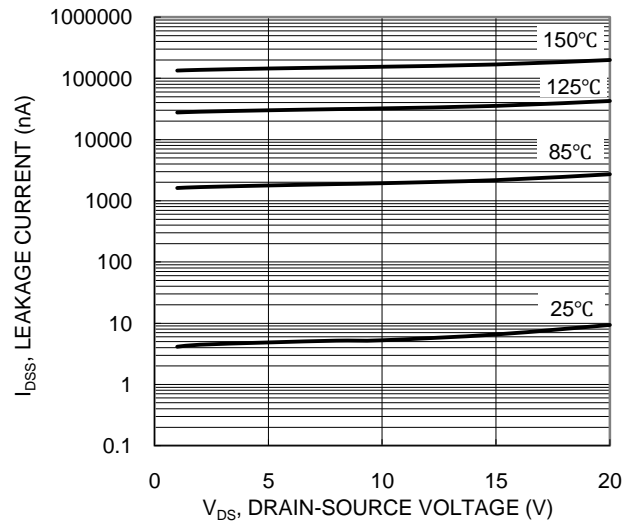


Figure 10. Typical Drain-Source Leakage Current vs. Voltage

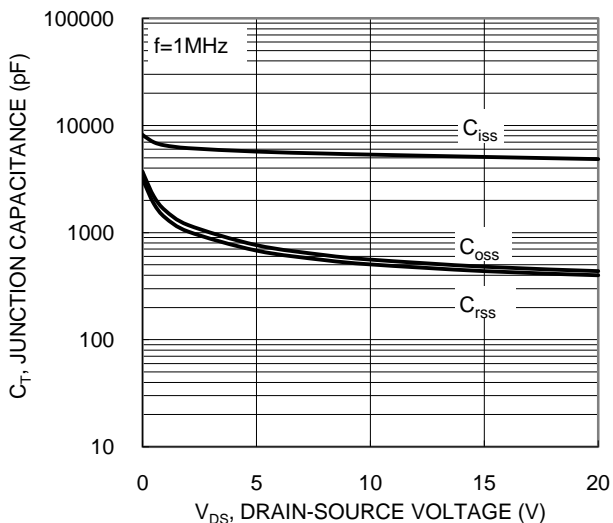


Figure 11. Typical Junction Capacitance

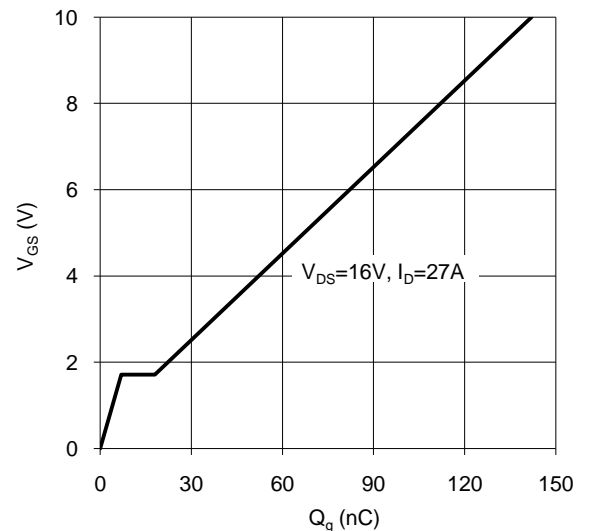
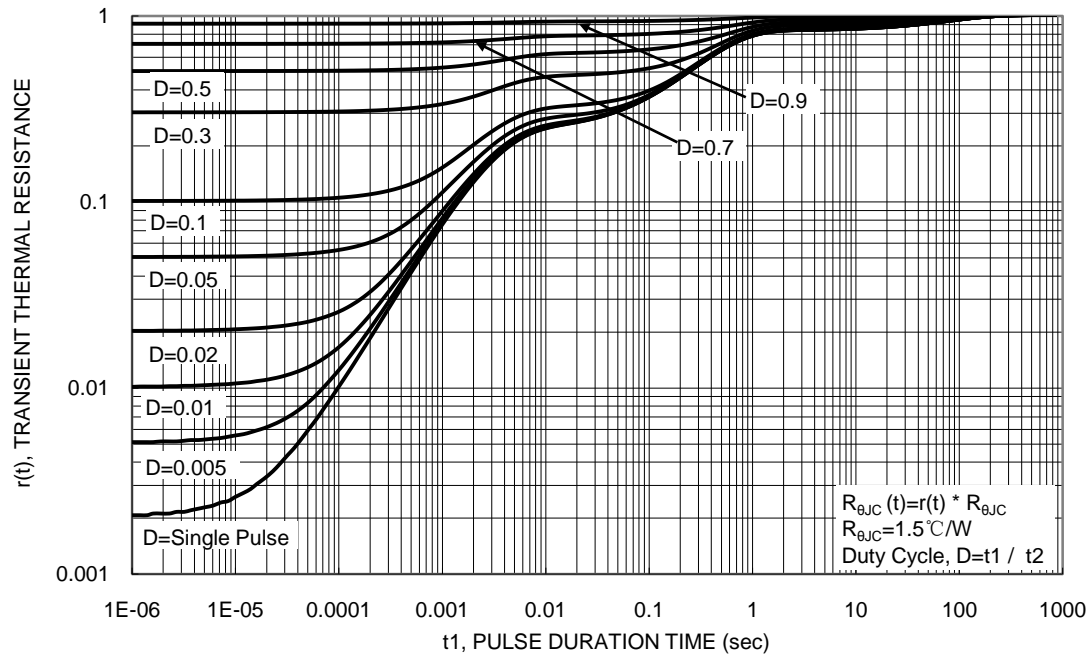
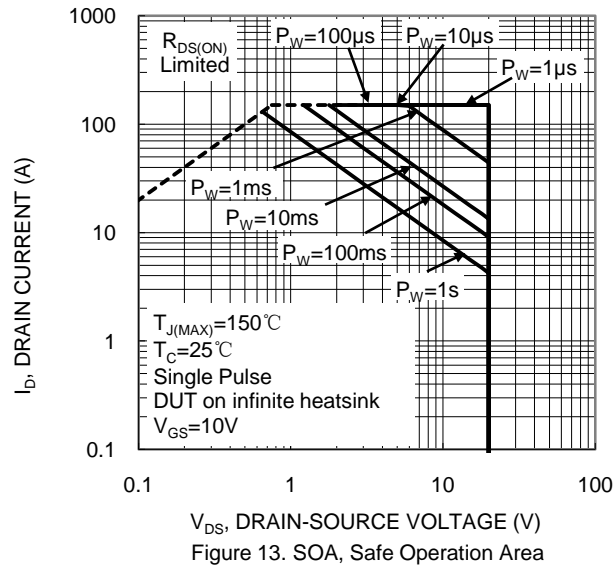
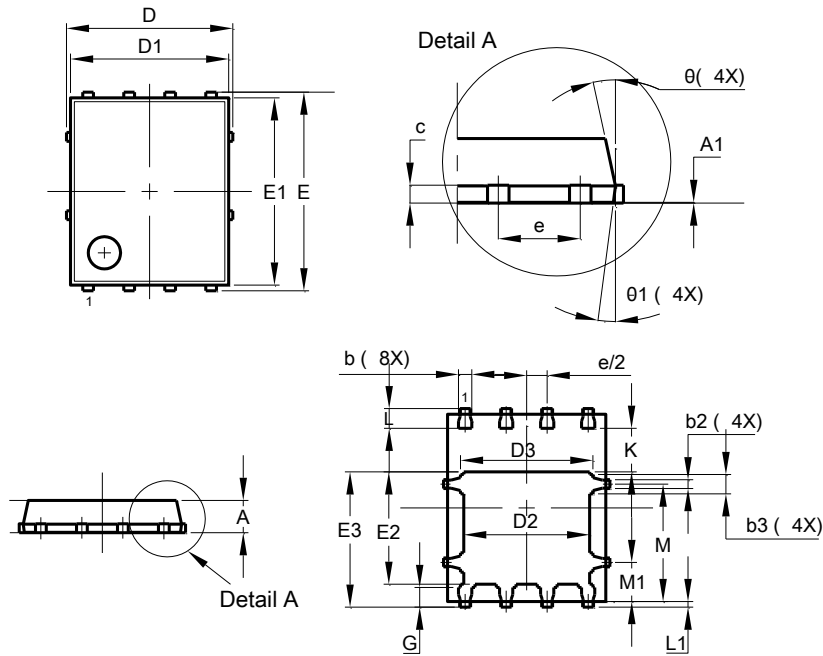


Figure 12. Gate Charge



Package Outline Dimensions

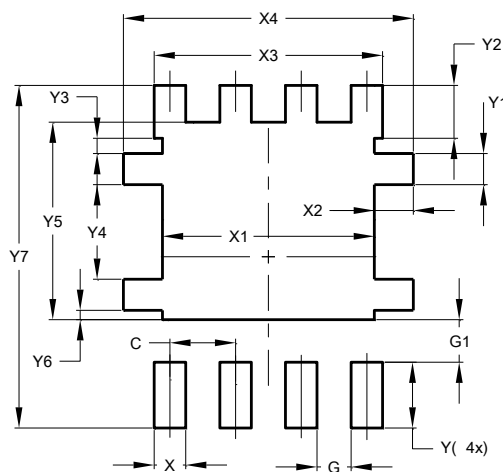
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



POWERDI [®] 5060-8			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0.00	0.05	-
b	0.33	0.51	0.41
b2	0.200	0.350	0.273
b3	0.40	0.80	0.60
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.70	4.10	3.90
D3	3.90	4.30	4.10
E	6.15 BSC		
E1	5.60	6.00	5.80
E2	3.28	3.68	3.48
E3	3.99	4.39	4.19
e	1.27 BSC		
G	0.51	0.71	0.61
K	0.51	-	-
L	0.51	0.71	0.61
L1	0.100	0.200	0.175
M	3.235	4.035	3.635
M1	1.00	1.40	1.21
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

NEW PRODUCT

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