Linduino SPI 1:8 Expander Shield

DESCRIPTION

Demonstration circuit 2430A is a Linduino® SPI 1:8 Expander Shield. The DC2430A shield routes SPI and I^2C signals from one DC2026 to one of eight selectable QuikEval™ connector sites. When a DC2430A QuikEval connector site is selected, an LED will illuminate next to the active site. The DC2430A shield comes with a mounted DC2026 as shown Figure 1.

DC2430A site selection can be controlled manually or through software. By default, Manual Site Select mode is enabled, which is controlled by the on-board rotary switch. LED D8 illuminates when Manual Site Select mode is enabled. For Software Site Select mode, example code is provided in the LTSketchbook.

The DC2430A provides ParallelSync™ support circuitry which aligns an asynchronous digital signal to the rising edge of a reference clock. This circuitry will allow for an easy demonstration of ParallelSync with Linear Technology's clock generation and distribution products, such as the LTC6951.

Design files for this circuit board are available at http://www.linear.com/demo/DC2430A

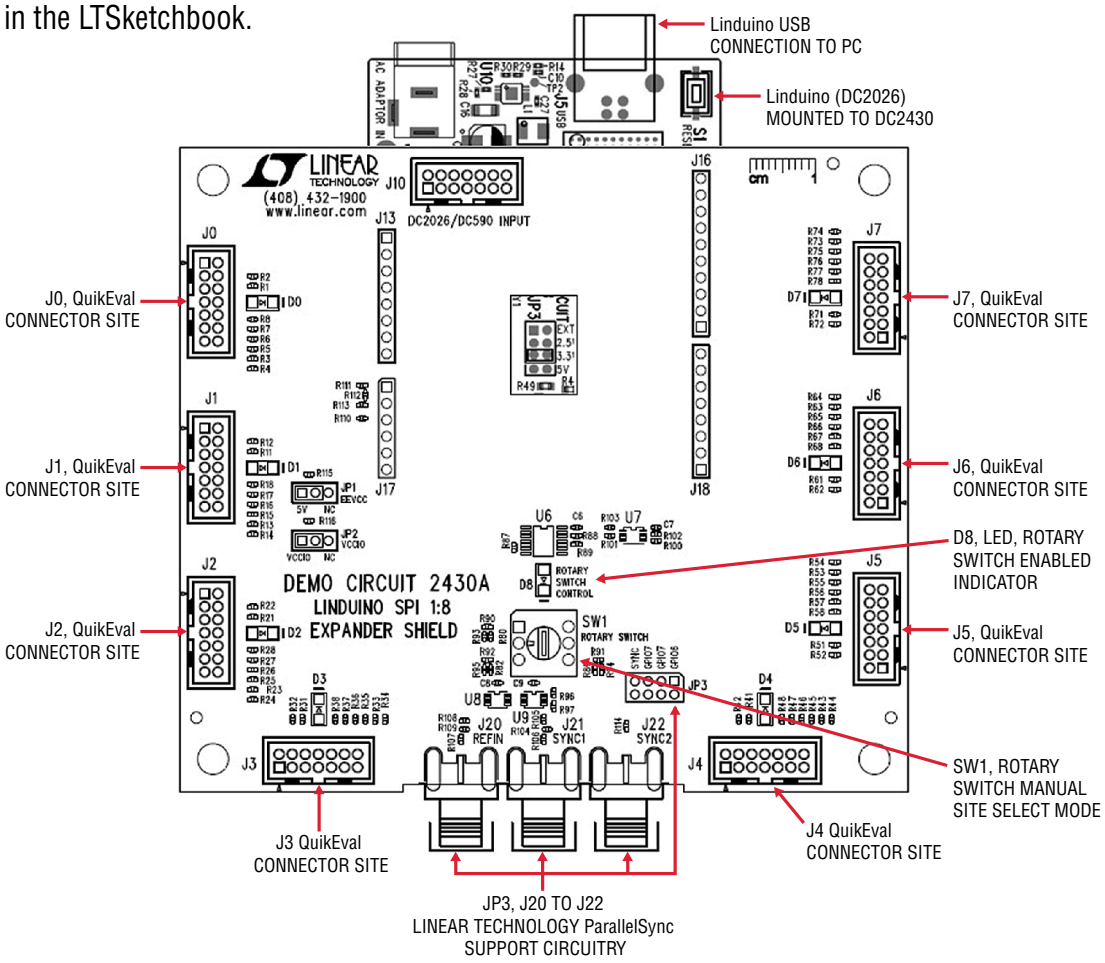


Figure 1. DC2430A Connections

QUICK START PROCEDURE

The DC2430A example is based off of the LTC6951 data sheet's ParallelSync Typical Application circuit. This example requires a 100MHz reference, one DC2430A (with DC2026C), two DC2248A and one DC1954A-B demo boards. This example uses three DC2430A QuikEval connector sites and the DC2430A ParallelSync circuitry.

DC2430A ParallelSync Example: Hardware

Refer to Figures 2 and 3

1. Modify both DC2248As to support an external reference
   a. C36 = 0.1µF
   b. C35 depopulate
   c. Remove JP1 jumper
2. QuikEval Connections
   a. DC2430A J7 to DC2248A #1 J14
   b. DC2430A J6 to DC2248A #2 J14
   c. DC2430A J5 to DC1954A-D J12
3. SMA Connections
   a. DC2430A J21 to DC2248A #2 J13
   b. DC2430A J22 to DC2248A #1 J13
   c. DC1954A-B J1 to DC2248A #2 J12
   d. DC1954A-B J2 to 50Ω termination
   e. DC1954A-B J3 to DC2248A #1 J12
   f. DC1954A-B J4 to 50Ω termination
   g. DC2430A J20 to DC1954A-B J6
4. Power Supply Connections
   a. DC2026 J5 USB to computer
   b. DC2248A #1 J16/J15 to +6V/GND
   c. DC2248A #2 J16/J15 to +6V/GND
   d. DC1954A-B J11/J10 to +3.3V/GND
5. Reference Connection: Connect a 100MHz reference to the DC1954A-B J8 connector. As an option Linear Technology provides the DC2429A, which has a 100MHz reference.
6. Set DC1954 jumpers to the following state
   a. OUTSEL0 (JP1): HIGH
   b. OUTSEL1 (JP2): HIGH
   c. OUTSEL2 (JP3): LOW
7. Sync Connection (Manual Site Select mode), connect DC2430A JP3 Sync pin to any external 3.3V digital signal. Set to LOW at start.

DC2430A ParallelSync Example: Manual Mode

To run this ParallelSync example in Software Site Select mode, refer to DC2430A Features section of this manual.

8. Refer to the LTC6951 and LTC6954 demo manuals to install their respective software programs.
9. Program LTC6954-2
   a. Turn DC2430A SW1 until DC2430A J5 is selected (D5 will illuminate)
   b. Start LTC6954_GUI
   c. Select LTC6954 settings shown in Figure 5
10. Program LTC6951 #2
    a. Turn DC2430A SW1 until DC2430A J6 is selected (D6 will illuminate)
    b. Start LTC6951Wizard
    c. In LTC6951 Wizard, click File → Load Settings. Select the directory/file "Data Sheet Typical Applications/6951_ParallelSyncw6954.6951set".
    d. Select CAL bit from the LTC6951 Wizard. The DC2248A's red STATUS LED (D1) should illuminate. A 200MHz signal should be present on the OUT0 outputs. Refer to Figure 4.
11. Program LTC6951 #1
    a. Turn DC2430A SW1 until DC2430A J7 is selected (D7 will illuminate)
    b. Repeat step 10C and 10D
12. Perform a ParallelSync operation by taking the DC2430A JP3 SYNC pin HIGH for >1ms. Return the DC2430A JP3 SYNC pin to LOW.

QUICK START PROCEDURE

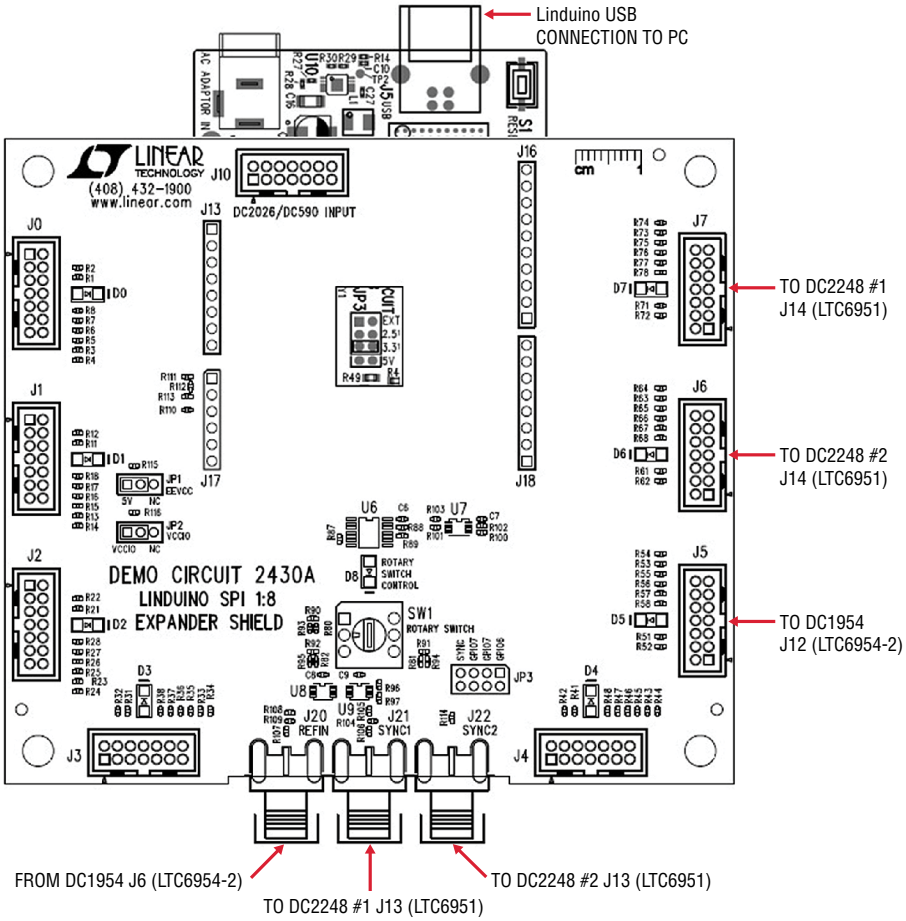


Figure 2. ParallelSync Setup, DC2430A

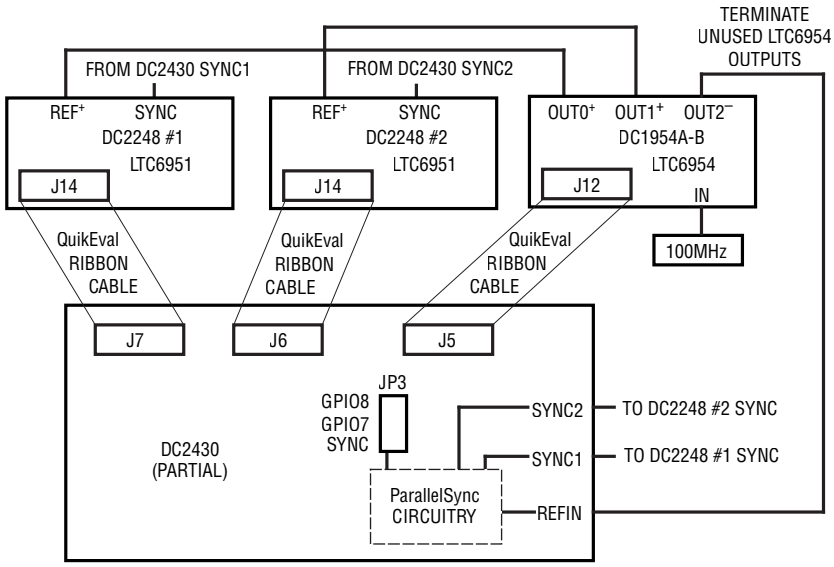


Figure 3. ParallelSync Setup, All Demo Boards

QUICK START PROCEDURE

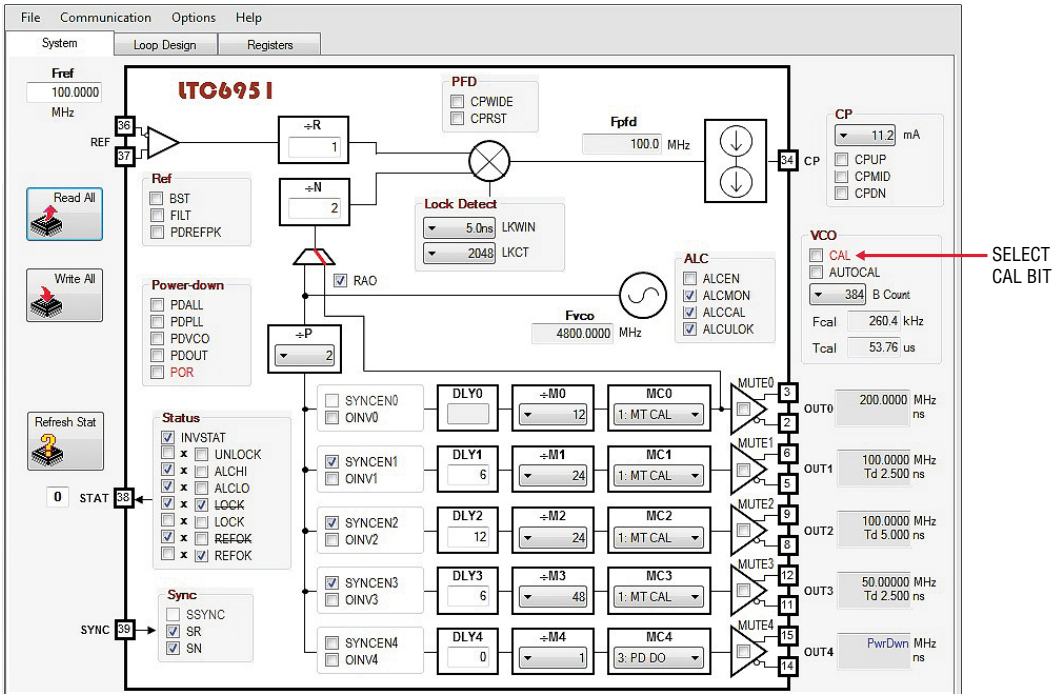


Figure 4. LTC6951 Settings

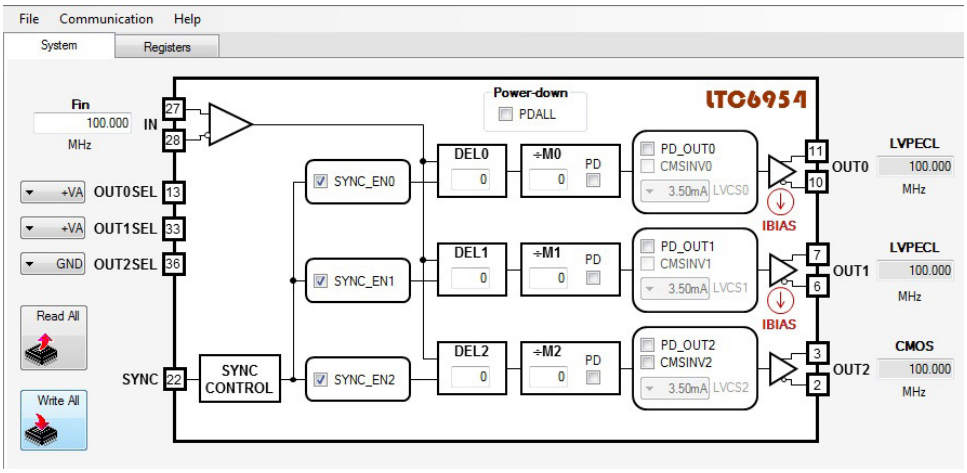


Figure 5. LTC6954-2 Settings

DC2430A FEATURES

QuikEval Site Selection

The user can select the DC2430A QuikEval Site manually or via software. Only one QuikEval Site can be active at a time, as shown in Table 1. An LED next to the selected QuikEval connector will illuminate.

Manual Site Select Mode: The rotary switch (SW1) determines which QuikEval connector (J0:J7) is selected. Manual Site Select mode is the DC2430A default power up option.

Software Site Select Mode: A Linduino sketch determines which QuikEval connector site (J0:J7) is selected. Refer to the DC2026 demo manual for instructions on downloading and installing the Arduino Integrated Development Environment and the LTSketchbook. After installation is complete, example code for automating the DC2430A ParallelSync Example above is provided. To locate example code refer to Figure 6. To run the DC2430A ParallelSync program refer to Figure 7. For this sketch to operate correctly, ensure a jumper is installed to connect DC2430A's SYNC and GPIO7 pins, refer to Table 2.

ParallelSync Circuitry: Sync to Reference Alignment

The DC2430A provides ParallelSync support circuitry that creates a sync pulse that meets ParallelSync's Sync to Ref timing requirements from an asynchronous digital signal. Refer to the ParallelSync device's data sheet for more details on Reference and Sync signal timing requirements.

Refer to Table 2 for details on the DC2430A's ParallelSync Circuitry's input and output requirements.

Table 1. QuikEval Site Selection

	DC2026 DIGITAL PIN STATE				DC2430A	
DC2430A MODE	D5	D4	D3	D2	QuikEval SITE	LED D8
Manual Site Select (Default State)	LOW	X	X	X	SW1 Setting	ON
Software Site Select	HIGH	LOW	LOW	LOW	J0	OFF
	HIGH	LOW	LOW	HIGH	J1	
	HIGH	LOW	HIGH	LOW	J2	
	HIGH	LOW	HIGH	HIGH	J3	
	HIGH	HIGH	LOW	LOW	J4	
	HIGH	HIGH	LOW	HIGH	J5	
	HIGH	HIGH	HIGH	LOW	J6	
	HIGH	HIGH	HIGH	HIGH	J7	

Table 2: ParallelSync Support Circuitry Input and Output Signals

PARAMETER	INPUT/OUTPUT	PHYSICAL LOCATION	DETAILS
Reference Input	Input	J20 SMA Connector	Connect a copy of the reference input signal that is supplied to the ParallelSync device's PLL/VCO reference input to J20.
SYNC1	Output	J21 SMA Connector	A CMOS sync pulse that has been time aligned to J20's reference input signal. Connect one of these signals to the SYNC pin of each ParallelSync device. Sync pulse signal levels are based on the VCCIO voltage selected by DC2026 JP3 setting. The Default DC2026 VCCIO voltage is 3.3V.
SYNC2	Output	J22 SMA Connector	
SYNC	Input	JP3 – Pin 7 (SYNC)	Asynchronous ParallelSync pulse input. Input sync pulse signal requirements are based on the VCCIO voltage selected by DC2026 JP3 setting. The default VCCIO voltage is 3.3V. The DC2430A JP3 SYNC input accepts LVTTL and LVCMOS signal levels. The SYNC signal can be generated from: 1. an external instrument tied to the DC2430A JP3 SYNC, or 2. the DC2026 digital pin 7, by shorting DC2430A JP3's SYNC to GPIO7 (default jumper location)
GPIO7	Output	JP3 – Pin 5 (GPIO7)	Controlled by the DC2026's digital pin 7. GPIO7's signal level has been level adjusted and can be connected directly to DC2430A JP3's SYNC pin. By default GPIO7 is programmed to a low state.

DC2430A FEATURES

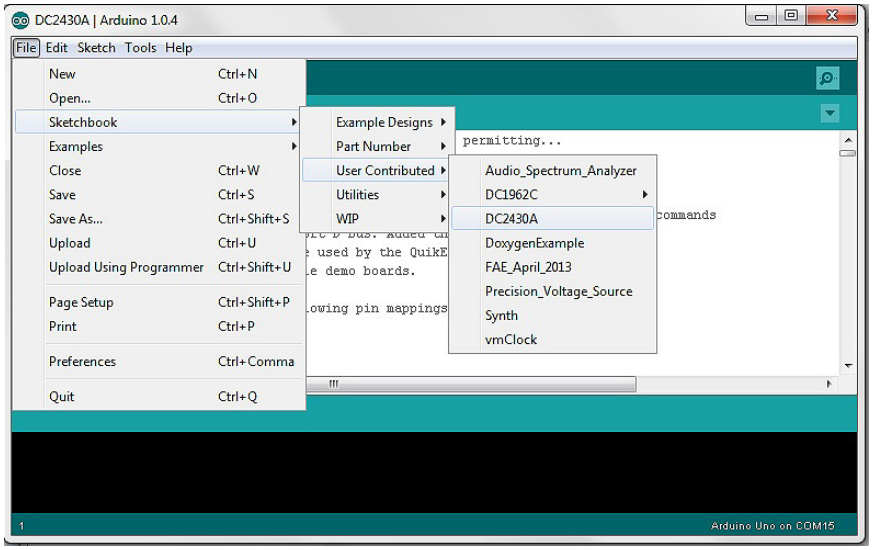


Figure 6. Locating ParallelSync Example Code

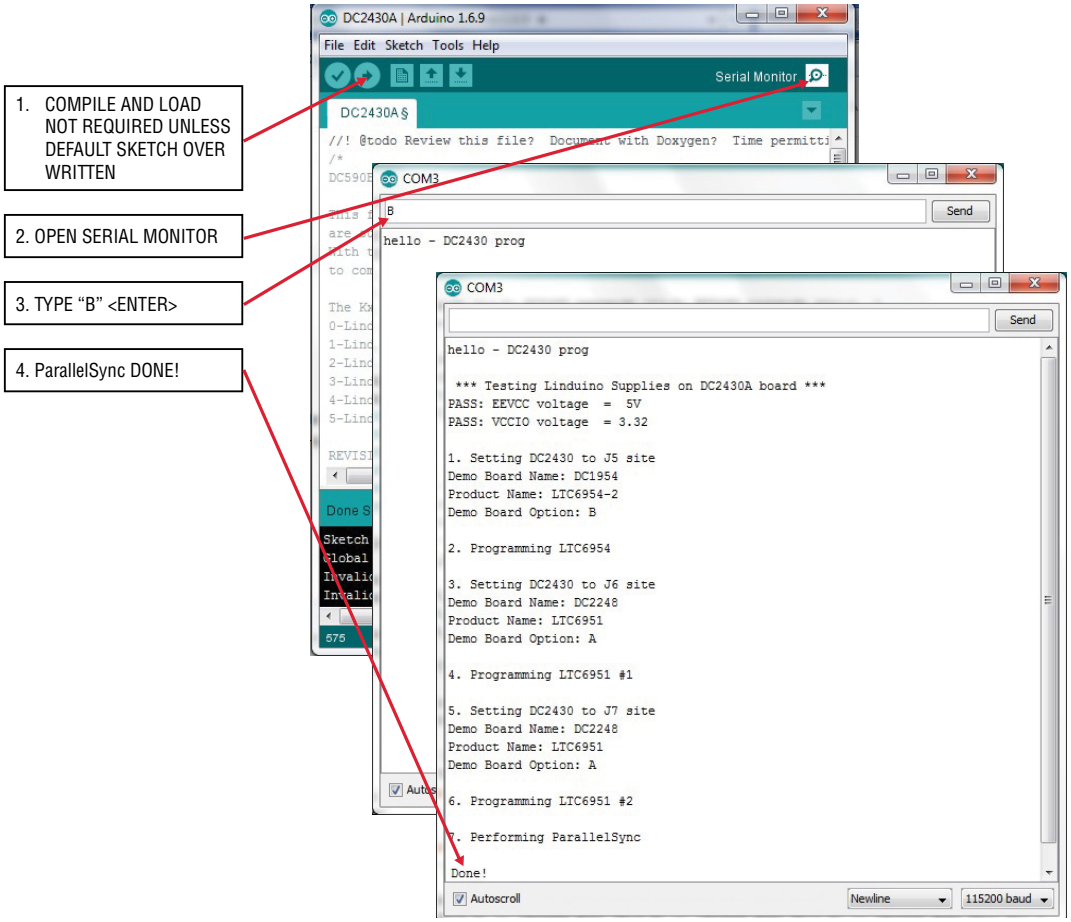
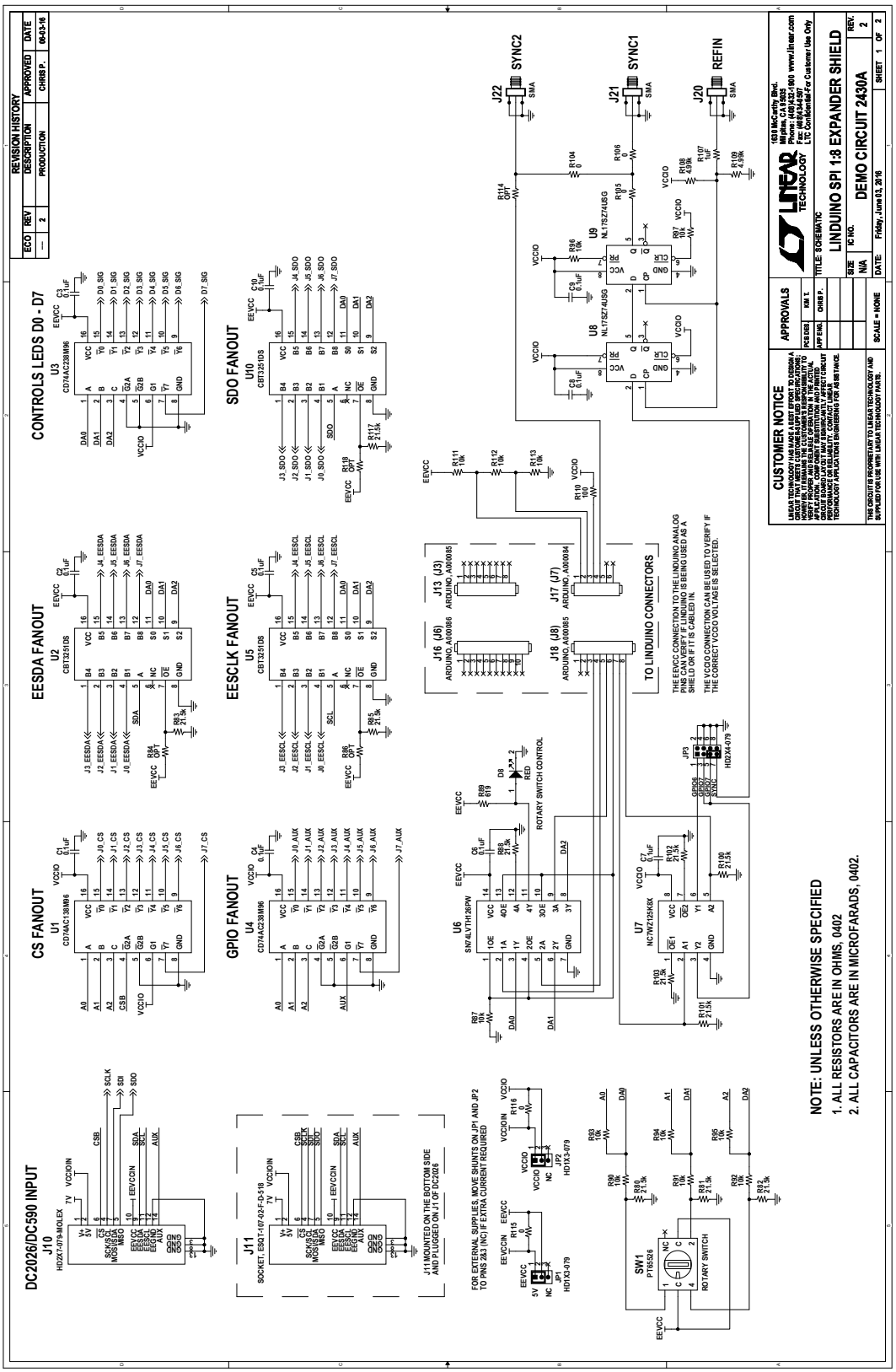


Figure 6. ParallelSync Example – Software Mode Site Select

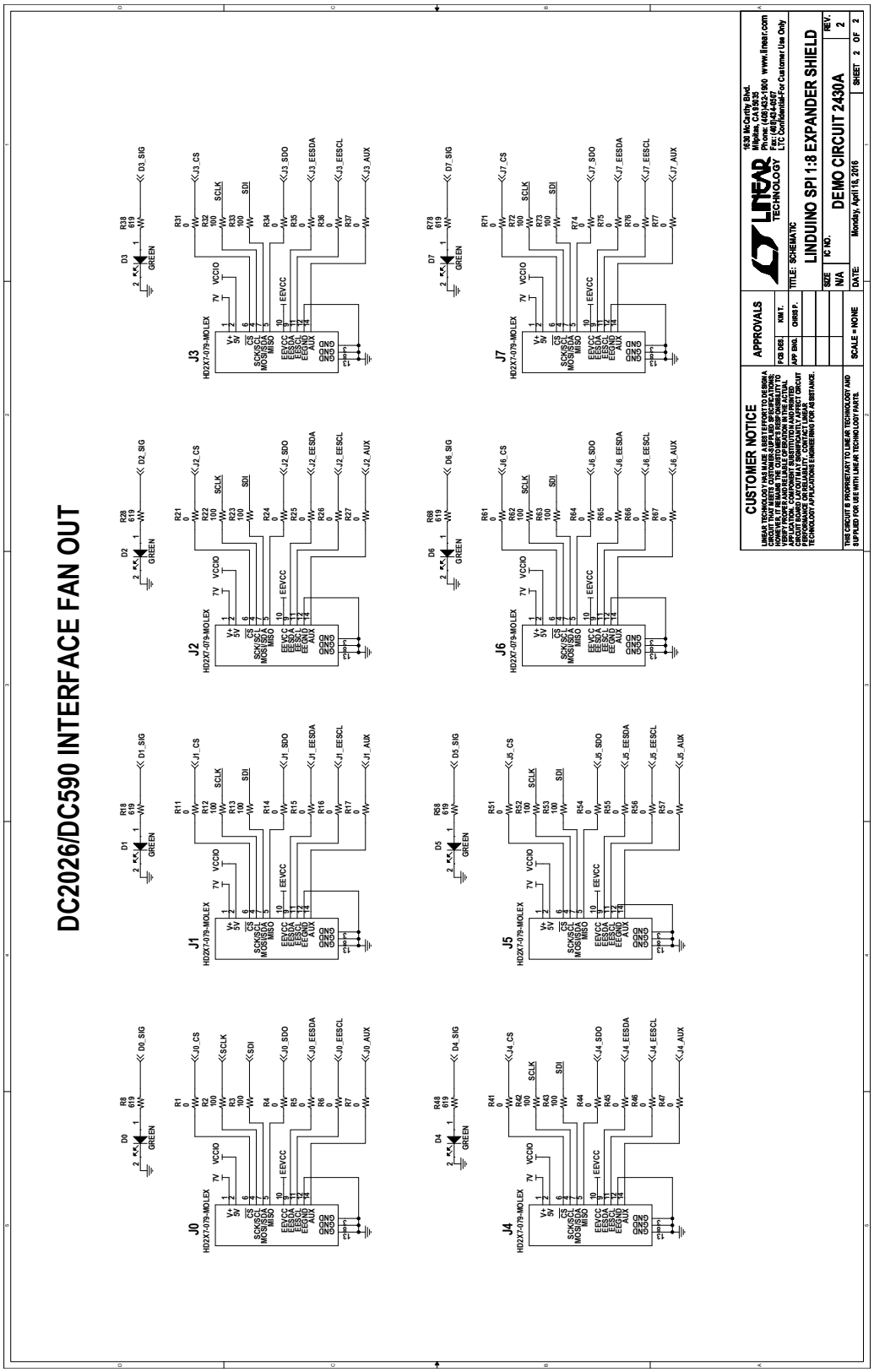
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	10	C1-C10	CAP., 0.1µF, X7R, 25V,10%, 0402	MURATA, GRM155R71E104KE14D
2	8	D0-D7	LED, GREEN, LED-ROHM-SML-01	ROHM, SML-012P8TT86
3	1	D8	LED, RED, LED-ROHM-SML-01	ROHM, SML-012V8TT86
4	2	JP1, JP2	CONN., HEADER, MALE, 1×3, 2mm, THT	WURTH ELEKTRONIK, 62000311121
5	1	JP3	CONN., HEADER, MALE, 2×4, 2mm, THT	WURTH ELEKTRONIK, 62000821121
6	9	J0-J7, J10	CONN., HEADER, 14-PIN, 2mm	MOLEX, 87831-1420
7	1	J11	CONN., SOCKET ELEVATED, 14-PIN, 2mm, THT	SAMTEC, ESQT-107-02-F-D-518
8	2	J13, J18	CONN., 0.100, 8 POSITION	ARDUINO, A000085
9	1	J16	CONN., 0.100, 10 POSITION	ARDUINO, A000086
10	1	J17	CONN., 0.100, 6 POSITION	ARDUINO, A000084
11	3	J20, J21, J22	CONN., SMA 50Ω, EDGE-LAUNCH	EF JOHNSON, 142-0701-851
12	45	R1, R4-R7, R11, R14-R17, R21, R24-R27, R31, R34-R37, R41, R44-R47, R51, R54-R57, R61, R64-R67, R71, R74-R77, R104-R106, R115, R116	RES., 0Ω, 1%, 1/16W, 0402	VISHAY, CRCW04020000Z0ED
13	17	R2, R3, R12, R13, R22, R23, R32, R33, R4, R43, R52, R53, R62, R63, R72, R73, R110	RES., 100Ω, 1%, 1/16W, 0402	VISHAY, CRCW0402100RFKED
14	9	R8, R18, R28, R38, R48, R58, R68, R78, R89	RES., 619Ω, 1%, 1/16W, 0402	VISHAY, CRCW0402619RFKED
15	11	R80-R83, R85, R88, R100-R103, R117	RES., 21.5k, 1%, 1/16W, 0402	VISHAY, CRCW040221K5FKED
16	0	R84, R86, R114, R118	RES., 0402	OPT
17	12	R87, R90-R97, R111-R113	RES., 10k, 1%, 1/16W, 0402	VISHAY, CRCW040210K0FKED
18	1	R107	CAP., 1µF, X7R, 6.3V,10%, 0402	MURATA, GRM155R70J105KA2D
19	2	R108, R109	RES., 4.99k, 1%, 1/16W, 0402	VISHAY, CRCW04024K99FKED
20	1	SW1	SWITCH, ROTARY DIP, CODE 26, OCTAL	APEM, PT65526
21	1	FOR SW1 (SEGMENT WHEEL)	SWITCH, OPERATING ELEMENT, SNAP-FIT	APEM, SRPT659544/BLK
22	1	U1	IC, DECODERS/DEMULTIPLEXERS, SO16	TEXAS INST., CD74AC138M96
23	3	U2, U5, U10	IC, FET DECODERS/DEMULTIPLEXERS, SSOP16	NXP, CBT3251DS,118
24	2	U3, U4	IC, DECODERS/DEMULTIPLEXERS, SO16	TEXAS INST., CD74AC238M96
25	1	U6	IC, BUS BUFFER, TSSOP14	TEXAS INST., SN74LVTH126PW
26	1	U7	IC, DUAL BUFFER, US8	FAIRCHILD SEMI., NC7WZ125K8X
27	2	U8, U9	IC, SINGLE D FLIP FLOP, US8	ON SEMI., NL17SZ74USG
28	3	SHUNTS FOR JP1-JP3 AS SHOWN ON ASSY DWG.	SHUNT, 2mm	WURTH ELEKTRONIK, 60800213421
29	4	MH1-MH4	STANDOFF, NYLON, SNAP-ON, 1	WURTH ELEKTRONIK, 702939000
30	2		STENCILS (TOP & BOTTOM)	STENCIL DC2430A-2

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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