# High-Performance DrBLADE

6.6 mm x 4.5 mm x 0.6 mm

# TDA21321

## Data Sheet

Revision 2.4, 2015-07-16

Power Management and Multi Market

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| Revision History | |
|---|---|
| **Page or Item** | **Subjects (major changes since previous revision)** |
| **Revision 2.4, 2015-07-16** | |
| | Package drawings figures 18 – 20 updated |
| | Inserted chapter 10 (packaging information) |
| | |

# 1 Applications

- Desktop and Server Vcore and non-Vcore buck-converter
- Single Phase and Multiphase POL
- CPU/GPU Regulation in Notebook, Desktop Graphics Cards, DDR Memory, Graphic Memory
- High Power Density Voltage Regulator Modules (VRM).

# 2 Features

- **Input voltage range +4.5 V to +16 V**
- Maximum average current up to 50 A
- For synchronous Buck step down voltage applications
- Power MOSFETs rated 25 V for safe operation under all conditions
- Fast switching technology for improved performance at high switching frequencies (> 750 kHz)
- Includes bootstrap diode
- Shoot through protection
- Max +8 V $V_{GS}$, high-side and low-side MOSFET gate driving voltage
- Compatible to standard +3.3 V PWM controller integrated circuits
- Tri-state PWM input functionality
- Small package: LG-WIQFN-38-1 (6.6x4.5x0.6 mm³)
- RoHS compliant
- Integrated temperature sense
- Integrated current sense

**Table 1 Product Identification**

| Part Number | Temp Range | Package | Marking |
|---|---|---|---|
| TDA21321 | -25°C to 125°C | LG-WIQFN-38-1 (6.6x4.5x0.6 mm³) | TDA21321 |

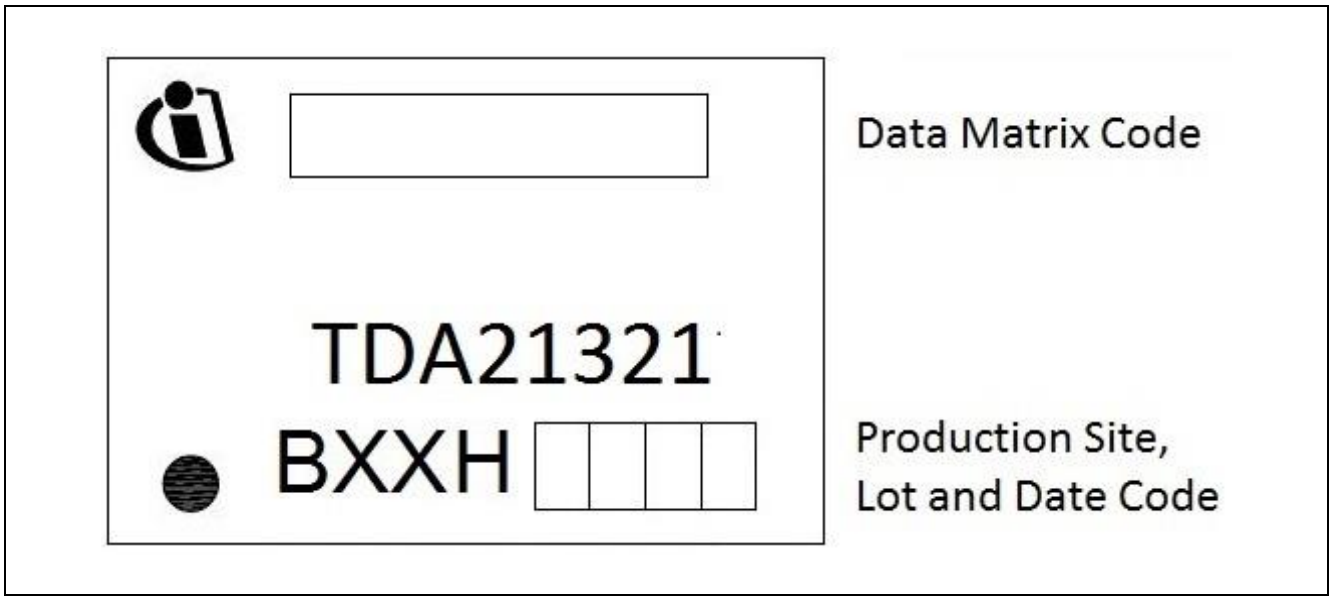


**Figure 1 Picture of the Product**

# 3 Description

## 3.1 Pinout

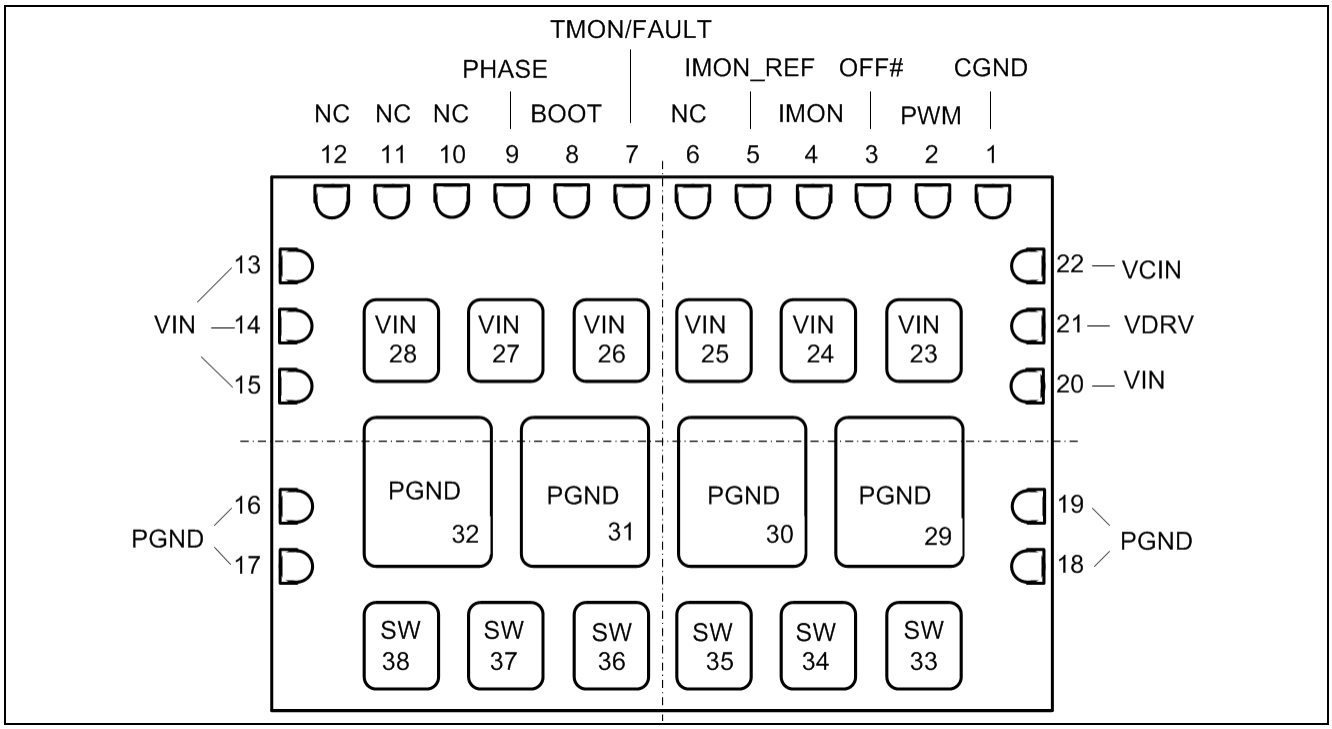


**Figure 2 Pinout, Numbering and Name of Pins (transparent top view)**

**Table 2 I/O Signals**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 2 | PWM | I/O | +3.3 V logic | **PWM drive logic input, Status output for VCIN**<br>The tri-state PWM input is compatible with 3.3 V. |
| 3 | OFF# | I | +3.3 V logic | **Deactivates LS-MOSFET**<br>Pull low to prevent LS-FET turn-on. Leave open if not used. (If traced out in noisy layout it may require external pull up.) |
| 4 | IMON | O | Analog | **Load current Sensing**<br>Provides a voltage proportional to the high/low-side MOSFET currents; Leave open if not used. |
| 5 | IMONREF | O | Analog | **Load current Sensing**<br>Reference to pin 4; Leave open if not used. |
| 7 | TMON/FAULT | O | Analog/ Digital | **Thermal Sensing / Fault Pin**<br>Temperature reporting, fault signaling by logic “H”; Status output of VDRV, Leave open if not used. |
| 8 | BOOT | I | Analog | **Bootstrap voltage pin**<br>Connect to BOOT capacitor |
| 9 | PHASE | I | Analog | **Switch node input**<br>Internally connected to SW pins, Connect to BOOT capacitor as reference pin for boot voltage |
| 33-38 (pads) | SW | O | Analog | **Switch node output**<br>High current output switching node |

**Table 3 Power Supply**

| Pin No. | Name | Pin Type | Function |
|---|---|---|---|
| 13 – 15, 20, 23-28 (pads) | VIN | POWER | **Input voltage**<br>Converter input voltage (connected to drain of the high-side MOSFET and driver) |
| 21 | VDRV | POWER | **MOSFET gate drive supply voltage**<br>High and low-side gate drive |
| 22 | VCIN | POWER | **Driver logic supply voltage**<br>bias voltage for the internal logic |

**Table 4 Ground Pins**

| Pin No. | Name | Pin Type | Function |
|---|---|---|---|
| 1 | CGND | GND | **Control signal ground**<br>Should be connected to local PGND externally, preferably by vias to GND plane |
| 16 – 19, 29-32 (pads) | PGND | GND | **Power ground**<br>All these pins must be connected to the power GND plane through multiple low inductance vias. |

**Table 5 Not Connected**

| Pin No. | Name | Pin Type | Function |
|---|---|---|---|
| 6, 10, 11, 12 | NC | – | **No internal connection**<br>Leave pin floating, tie to VIN or GND. |

## 3.2 General Description

The Infineon TDA21321 is a multichip module that incorporates Infineon's premier MOSFET technology into a single high-side and a single low-side MOSFET. This is coupled with a robust, high performance, high switching frequency gate driver on a single 38 pin LG-WIQFN-38-1 (6.6x4.5x0.6 mm³) package. The optimized gate timing enables significant light load efficiency improvements over discrete solutions. State of the art MOSFET technology provides exceptional performance at full and light load.

When combined with Infineon's Primarion™ Controller Family of Digital Multi-phase Controllers, the TDA21321 forms a complete core-voltage regulator solution for advanced micro and graphics processors as well as point-of-load applications. The device package height is 0.6 mm. It is an excellent choice for applications with critical height limitations and has reduced thermal impedance from junction to top case compared to DrMOS, allowing for top side cooling.

The power density for transmitted power of this approach is approximately 50 W within a 28 $mm^2$ area.

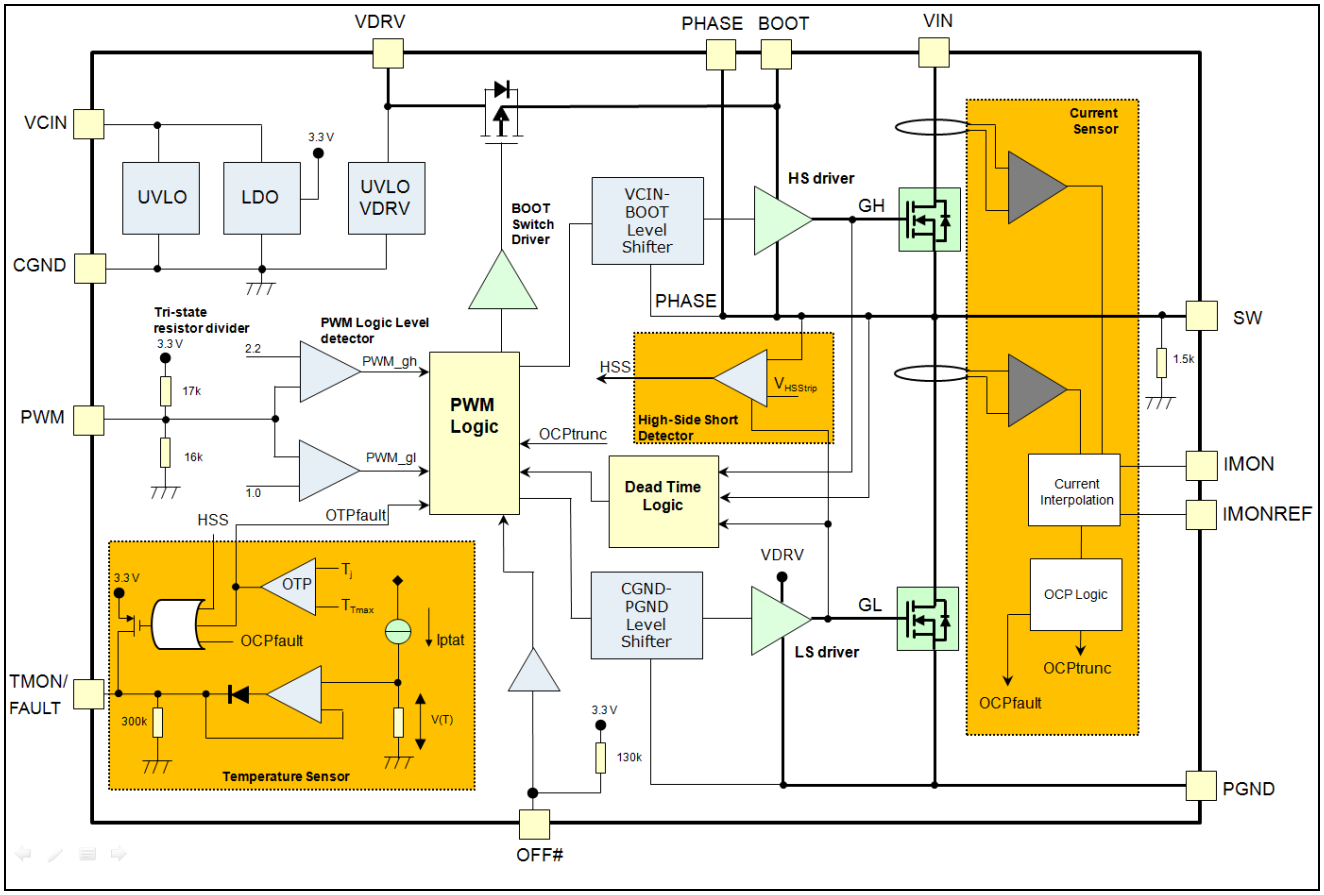


**Figure 3 Simplified Block Diagram**

***Attention: GH and GL are not accessible on this package, but are mentioned for clarity in this block diagram.***

# 4 Electrical Specification

## 4.1 Absolute Maximum Ratings

*Note: $T_A$ = 25°C*

Stresses above those listed in Table 6 “Absolute Maximum Ratings” and Figure 4 “Repetitive Voltage Stress at Phase Node - Safe Operating Area” may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied or recommended at these or any other conditions in excess of those given in the operational sections of this specification. Exposure over values of the recommended ratings (Table 8) for extended periods may adversely affect the operation and reliability of the device.

**Table 6 Absolute Maximum Ratings**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Frequency of the PWM input | $f_{SW}$ | 0.01 (in CCM) | – | 1.2 | MHz | rated current sense accuracy between 100 kHz and 800 kHz |
| Maximum average load current | $I_{OUT}$ | – | – | 50 | A | – |
| Input Voltage | $V_{IN}$ (DC) | -0.30 | – | 18 | V | – |
| Logic supply voltage | $V_{CIN}$ (DC) | -0.30 | – | 9 | V | – |
| High and low-side driver voltage | $V_{DRV}$ (DC) | -0.30 | – | 9 | V | – |
| Switch node voltage | $V_{SW}$ (DC) | -1 | – | 18 | V | – |
| | $V_{SW}$ (AC) | -10[1] | – | 25[1] | V | – |
| PHASE voltage pin (9) | $V_{PHASE}$ (DC) | -1 | – | 18 | V | – |
| | $V_{PHASE}$ (AC) | -10[1] | – | 25[1] | V | – |
| BOOT voltage | $V_{BOOT}$ (DC) | -0.3 | – | 25 | V | – |
| | $V_{BOOT}$ (AC) | – | – | 30[1] | V | – |
| | $V_{BOOT-PHASE}$ (DC) | -0.3 | – | 9 | V | – |
| OFF# voltage | $V_{OFF\#}$ | -0.3 | – | 4 | V | Maximum value valid for operation up to 24h accumulated over lifetime in temperature range of -25˚C ≤ $T_j$ ≤ 125˚C. Else the maximum value is 3.6V. |
| PWM voltage | $V_{PWM}$ | -0.3 | – | 4 | V | |
| TMON/FAULT | $V_{TMON/FAULT}$ | -0.3 | – | 3.6 | V | – |
| IMON | $V_{IMON}$ | -0.3 | – | 3.6 | V | – |
| IMONREF | $V_{IMONREF}$ | -0.3 | – | 3.6 | V | – |
| Junction temperature | $T_{Jmax}$ | -40 | – | 150 | °C | – |
| Storage temperature | $T_{STG}$ | -55 | – | 150 | °C | – |

*Note: All rated voltages are relative to voltages on the CGND and PGND pins unless otherwise specified.*

[1] AC is limited to 10 ns

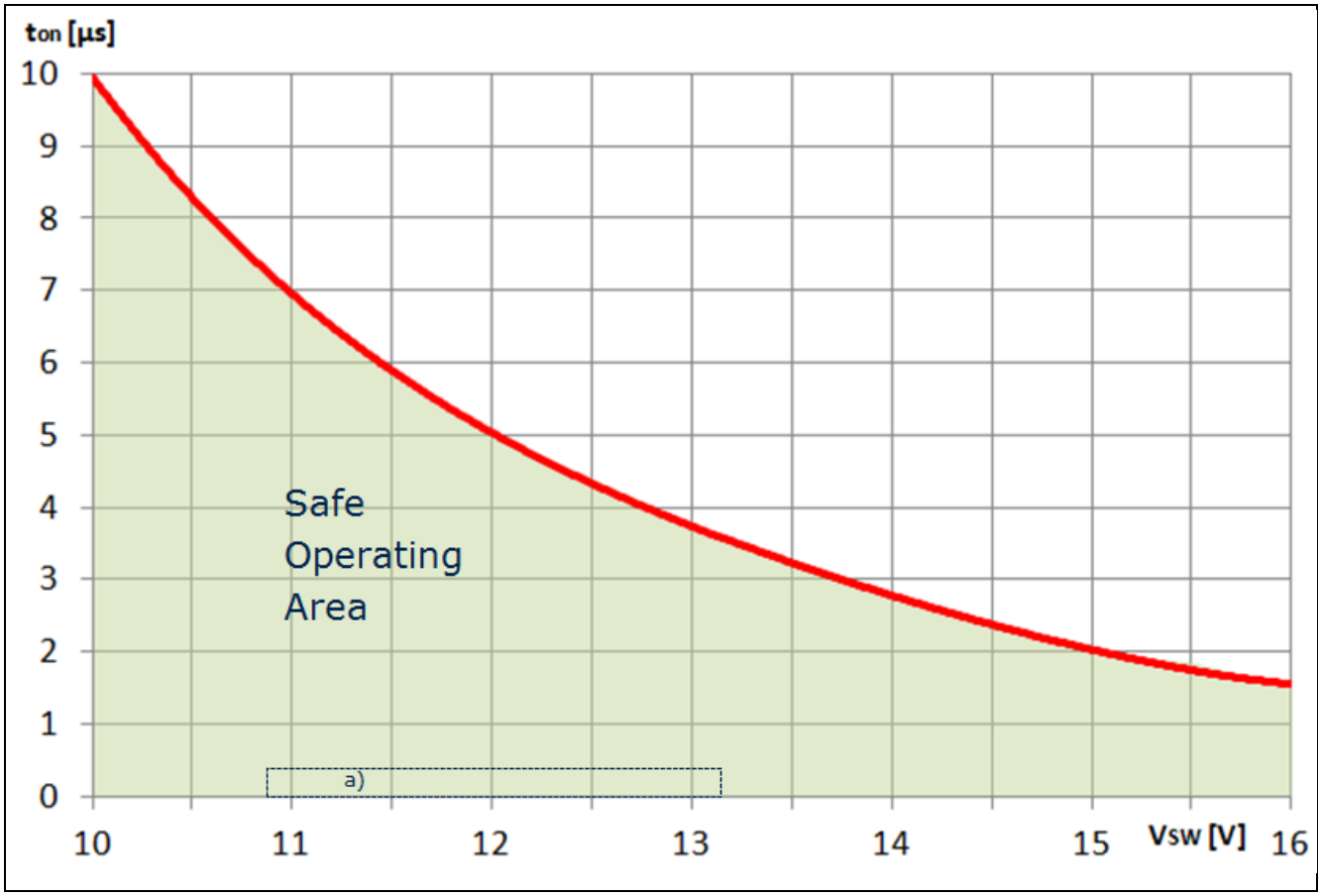


**Figure 4 Repetitive Voltage Stress at Phase Node - Safe Operating Area**

Note: $t_{on}$ refers to the on-time of the HS-MOSFET. For input voltages below 10 V no limits on the duration of $t_{on}$ need to be applied.

Information: a) - Area of typical computing applications with 12 V input supply voltage

## 4.2 Thermal Characteristics

**Table 7 Thermal Characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance to case (soldering point) | $\theta_{JC}$ | – | 3.5 | – | K/W | – |
| Thermal resistance to top of package | $\theta_{JCtop}$ | – | 3.7 | – | | – |
| Thermal resistance to ambient | $\theta_{JA}$ | – | 14 | – | | $P_{loss}$ = 4.5 W, $T_A$ = 70 °C, 8 layer server board (2 oz copper) |

## 4.3 Recommended Operating Conditions and Electrical Characteristics[2]

*Note: $V_{IN}$ =12V, $V_{DRV}$ = $V_{CIN}$ = 5 V, $T_A$ = 25 °C unless otherwise specified*

**Table 8 Recommended Operating Conditions**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **Input voltage** | **$V_{IN}$** | **4.5** | **–** | **16** | **V** | – |
| MOSFET driver voltage | $V_{DRV}$ | 4.5 | – | 8 | V | – |
| Logic supply voltage | $V_{CIN}$ | 4.5 | – | 8 | | – |
| Frequency of the PWM | $f_{sw}$ | 100 | – | 800 | kHz | CCM operation with stated current sense accuracy |
| Junction temperature | $T_{jOP}$ | -25 | – | +125 | °C | – |

[2] Exposure over values of the recommended ratings for extended periods may adversely affect the operation and reliability of the device. Min/Max values are based on empirical Cpk.

**Table 9 Voltage Supply And Biasing Current**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| UVLO VCIN rising | $V_{UVLO1\_R}$ | 3.0 | – | 4.0 | V | Driver enable threshold; above threshold driver is active, driver responds to PWM input when UVLO VDRV and UVLO BOOT are enabled, TMON/FAULT reports driver temperature when UVLO VDRV is enabled |
| UVLO VCIN falling | $V_{UVLO1\_F}$ | 2.6 | – | 3.6 | | Driver disable threshold; below threshold driver is inactive, PWM and TMON/FAULT held low by pull-down resistors |
| UVLO VDRV rising | $V_{UVLO2\_R}$ | 4.16 | 4.25 | 4.34 | V | GL, GH and TMON/FAULT enable threshold; when UVLO VCIN is enabled then: above threshold GL is enabled, GH depends on UVLO BOOT, TMON/FAULT is released to report driver temperature |
| UVLO VDRV falling | $V_{UVLO2\_F}$ | 3.7 | 3.8 | 3.9 | | GL, GH and TMON/FAULT disable threshold; when UVLO VCIN is enabled: below threshold after 3 consecutive cycles or 15 µs (typ.) the driver outputs GL/GH are disabled, TMON/FAULT stops temperature reporting and is held low by pull-down resistor |
| UVLO BOOT rising | $V_{UVLOboot\_R}$ | 3.88 | 4.05 | 4.22 | V | $V_{BOOT}$-$V_{SW}$ rising, GH enable threshold; when UVLO VCIN and UVLO VDRV are active: above threshold GH responds to PWM |
| UVLO BOOT falling | $V_{UVLOboot\_F}$ | 3.5 | 3.63 | 3.76 | | $V_{BOOT}$-$V_{SW}$ falling, GL/GH disable threshold; when UVLO VCIN and UVLO VDRV are enabled: below threshold counter starts, after 3 consecutive PWM cycles driver outputs are disabled |
| Driver current | $I_{VDRV\_600kHz}$ | – | 18 | – | mA | OFF# = 3.3 V, $f_{SW}$ = 600 kHz |
| | $I_{VDRV\_1MHz}$ | – | 30 | – | | OFF# = 3.3 V, $f_{SW}$ = 1 MHz |
| IC current (control) | $I_{VCIN\_O}$ | – | 1.0 | – | mA | OFF# = 3.3 V, PWM = Open for > 19 µs (typ.) |
| IC quiescent | $I_{CIN}$+$I_{DRV}$ | – | 1.2 | – | | |
| Pre-Bias at SW | $V_{SW\_0}$ | – | 120 | 160 | mV | PWM in Tri-state ($V_{PWM\_S}$), VCIN = VDRV = 5V, internal pull-down resistor 1.5 kΩ |

**Table 10 Current Sense**

| Parameter | | Symbol | Values | | | Unit | Note / Test Condition | |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | | |
| IMON | Voltage Range | $V_{IMON}$ | 0.8 | – | 2.2 | V | IMONREF is a current mirror output serving as unfiltered reference node. At IMON a filtered voltage signal proportional to the current is provided. It tracks the average value of IMONREF. | |
| IMONREF | IMON gain resistor range | $R_{IMON}$ | 0.2 | – | 1.0 | kΩ | | |
| | Current sense gain | $a_{CS}$ | - | 6.67 | - | µA/A | | |
| | Leakage current | $I_{Leak}$ | -2 | 0 | 2 | µA | $I_D$ = 0, $V_{CM}$ = 1.5, PWM in tri-state | |
| Current Monitoring | Zero current offset | $I_{Offset}$ | -3 | 0 | 3 | µA | Corresponds to 2.25 mV at 5 mV/A ($R_{IMON}$ = 750Ω), device in regulation | |
| | Accuracy at 25 °C … 125 °C<br>$V_{DRV}$ = 5 V ± 10 %<br>$V_{CIN}$ = 5 V ± 10 % | a11 | -3 | – | 3 | % | for 45 A < Iout < $I_{OCPtrip}$ | tested at 25 A, other guaranteed by design |
| | | a12 | -2.5 | – | 2.5 | % | for 25 A ≤ Iout ≤ 45 A | |
| | | a13 | -0.5 | – | 0.5 | A | for -25 < Iout < 25 A | |
| | | a14 | -20 | – | 20 | % | for -50 A ≤ Iout ≤ -25 A | |

**Table 11 Temperature Sense**

| Parameter | | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Temp. Sense and Accuracy | Temp. FAULT | $T_{TMAX}$ | 140 | 145 | 150 | °C | Temperature monitors driver junction. Circuit reports temperatures to -25 °C accurately (0.4V). The maximum temperature reported is $T_{TMAX}$. Above $T_{TMAX}$ a logic 'H' is asserted to indicate a fault (latched). At OTP fault PWM input is suspended and driver is being set to tri-state mode until VCIN and/or VDRV have been re-cycled. |
| | Output high | $V_{TMON\_H}$ | 2.6 | – | – | V | |
| | Output monitor | $V_{TMON}$ | 0.4 | – | 1.8 | | |
| | Fault delay[3] | $t_{TMONdeg}$ | – | 3 | – | µs | |
| | Temp. range[4] | $T_{TMON}$ | -25 | – | 150 | °C | |
| | Temp. coefficient[5] | TC | – | 8 | – | mV/K | |
| | Nominal | $V_{25C}$ | – | 800 | – | mV | |
| | Accuracy at -25 °C … 125 °C (tested at 25 °C, other guaranteed by design) | $a_{TMON}$ | -4 | – | 4 | K | -25 °C … 125 °C, unspecified below -25 °C |

**Table 12 Other Logic Functions, Inputs/Outputs And Thresholds**

| Parameter | | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| OFF# | Input low | $V_{OFF\#\_L}$ | – | – | 0.8 | V | $V_{OFF\#}$ falling |
| | Input high | $V_{OFF\#\_H}$ | 2.0 | – | – | | $V_{OFF\#}$ rising |
| PWM | Input low | $V_{PWM\_L}$ | – | – | 0.8 | V | $V_{PWM}$ falling |
| | Input high | $V_{PWM\_H}$ | 2.4 | – | – | | $V_{PWM}$ rising |
| | Input resistance | $R_{IN-PWM}$ | 6 | – | 10 | kΩ | $V_{PWM}$ = 1 V |
| | Open voltage | $V_{PWM\_O}$ | – | 1.6 | – | V | $V_{PWM\_O}$ |
| | Tri-state shutdown window[6] | $V_{PWM\_S}$ | 1.2 | – | 2.0 | | – |
| | Min pulse width[7] | $t_{PWMdetect}$ | 5 | – | 10 | ns | Minimum pulse width to detect PWM pulse |
| | Min pulse time[8] | $t_{PWMmin}$ | – | 30 | – | ns | PWM pulses shorter than $t_{PWMmin}$ will be extended to $t_{PWMmin}$ |
| OCP | Overcurrent Protection | $I_{OCPtrip}$ | 58 | 65 | 72 | A | Duty cycle limitation at $I_{OCPtrip}$, fault asserted and latched after 10 truncated consecutive switching cycles |
| HSS | High-Side-Short Protection | $V_{HSStrip}$ | – | 0.83 | – | V | Voltage tested at phase node during LS-MOSFET on-time. If voltage exceeds $V_{HSStrip}$, fault is asserted and latched. |

[3] Guaranteed by design
[4] Guaranteed by design
[5] Guaranteed by design
[6] Maximum voltage range for tri-state
[7] Guaranteed by design
[8] Guaranteed by design

**Table 13 Timing Characteristics** [9]

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| PWM tri-state to SW falling delay | t_pts2 | – | 16 | – | ns | $V_{OUT}$ prebiased at 1 V, other conditions as for t_pts |
| PWM tri-state to SW rising delay | t_pts | – | 19 | – | ns | $I_{LOAD}$ = 0, VDRV = VCIN = 5 V, VIN = 12 V, fsw = 600 kHz |
| PHASE Shutdown Hold-Off time from PWM low | t_tsshd | – | 41 | – | | |
| PHASE Shutdown Hold-Off time from PWM high | t_tssh | – | 45 | – | | |
| PWM to SW Turn-off propagation delay | t_pdlu | – | 31 | – | | |
| PWM to SW Turn-on propagation delay | t_pdll | – | 21 | – | | |
| OFF# Turn-off propagation delay falling | t_pdl_OFF# | – | 17 | – | ns | |
| OFF# Turn-on propagation delay rising | t_pdh_OFF# | – | 25 | – | | |

Corresponding diagrams can be found under section “Gate Driver Timing Diagram”.

[9] All timing data are guaranteed by design

# 5 Theory of Operation

The TDA21321 features a power stage with MOSFET driver. Temperature and current are being monitored. Data and various fault conditions can be reported to the controller.

The power MOSFETs are optimized for 5 V gate drive enabling excellent high load and light load efficiency. The gate driver is a robust high-performance driver rated at the switching node for DC voltages ranging from -1 V to +18 V.

## 5.1 Driver Characteristics

The gate driver has 2 voltage inputs, VCIN and VDRV. VCIN is the 5 V logic supply for the driver. VDRV sets the driving voltage for the high-side and low-side MOSFETs. The reference for the gate driver control circuit (VCIN) is CGND. To decouple the sensitive control circuitry (logic supply) from a noisy environment a ceramic capacitor must be placed between VCIN and CGND close to the pins. VDRV needs also to be decoupled using a ceramic capacitor (MLCC) between VDRV and PGND in close proximity to the pins. PGND serves as reference for the power circuitry including the driver output stage.

## 5.2 Power-Up Sequence

Without the logic supply VCIN the device remains off. PWM is held low by an internal pull down resistor. PWM information cannot be fed to the driver. VCIN supplies power to the driver logic. With the presence of VCIN on power-up of the gate drive voltage VDRV, the driver and the PWM input will be enabled, the unforced PWM level will be within its tri-state window. This signals that the driver supply voltages have cleared their respective UVLO thresholds. TMON/FAULT reports temperature. The PWM controller is expected to wait for this to happen before initiating PWM signals to start up the system.

Note that with VCIN and VDRV present, the switching node can rise up to $V_{SW\_0}$ with PWM in tri-state condition.

## 5.3 Inputs to the Internal Control Circuits

**PWM** is the control input to the IC from an external PWM controller and is compatible with 3.3 V logic. The PWM input has tri-state functionality. When the voltage remains in the specified PWM-shutdown-window for at least the PWM-shutdown-holdoff time t_tsshd, the operation will be suspended by keeping both MOSFET gate outputs low. Once left open, the pin is held internally at a tri-state level of $V_{PWM\_O}$. The PWM signal must prevail for at least $t_{PWMmin}$ to initiate a response from the driver.

The PWM threshold voltages $V_{PMW\_O}$, $V_{PWM\_H}$, $V_{PWM\_L}$ do not vary over the wide range of VCIN supply voltages (4.5 V to 8 V).

The **OFF#** pin provides a means to keep the low-side MOSFET disabled regardless of the PWM signal. It is an active low signal. An internal pull up resistor ensures regular operation when the pin is not used.

When pulled low, the low-side MOSFET is kept in off-state. In multiphase systems the OFF# pins of all phases may be connected together. One controller output is then able to toggle the LS-FET operation mode.

**Table 14 PWM and OFF# Pin Functionality, Driver Outputs**

| PWM logic level | OFF# logic level | Gate HS-FET (GH) | Gate LS-FET (GL) |
|---|---|---|---|
| High | Any | High | Low |
| Open (Tri-state: left floating, or high impedance) | | Low | |
| Low | Low | | |
| | High or open | | High |

## 5.4 Monitoring and Protection Circuits

The TDA21321 is designed with the various protection functions. Most of these protection features require a PWM controller that reacts properly on the assertion of a fault signal at TMON/FAULT to shutdown the circuit. Fault assertion is latched and is being removed when VCIN and/or VDRV will be re-cycled. A reported fault is always indicating a critical condition with high stress levels on the device and/or load that requires immediate action in form of shutdown to prevent imminent catastrophic failure.

In multiphase regulators the TMON/FAULT outputs of the power stages will have to be connected together. The TMON/FAULT output voltage follows the highest voltage output of any phase connected. The pull-down capability of any TMON/FAULT output is weak so that a fault assertion of any phase will always override other phase outputs.

### 5.4.1 High-Side Short Protection (HSS)

The voltage at the switching node is being monitored during the LS-MOSFET being driven in on-state. When during that time the switching node voltage exceeds a critical threshold of $V_{HSStrip}$ the HSS fault is being asserted by pulling TMON/FAULT to ‘high’. The PWM controller has to shut down the power stage to prevent catastrophic failure. TMON/FAULT is latched and will be released when VCIN and/or VDRV will be re-cycled.

HSS can lead to a very sudden current rise that can impact voltage potentials in and in vicinity of the power device so that early reset events could potentially occur. Therefore, it is important to always have the system controller terminate the power supply as soon as a critical event has been reported by the power stage.

### 5.4.2 Thermal Protection and Temperature Monitoring

The driver monitors and reports its temperature. In multiphase systems with connected TMON/FAULT pins only the highest temperature of any of the connected phases will be reported. The PWM controller is supposed to react on the reported temperature with power throttling commands to the load. If the system fails to respond and the temperature continues to rise to a value of $T_{TMAX}$ for at least $t_{TMONdeg}$, TMON/FAULT is being pulled high to report an Over-Temperature Fault (OTP).

TMON/FAULT is latched and will be released when VCIN and/or VDRV will be re-cycled. At OTP fault the driver outputs will be deactivated until VCIN and/or VDRV have been re-cycled. The PWM controller is ecxpected to shut down the power stage to prevent catastrophic failure.

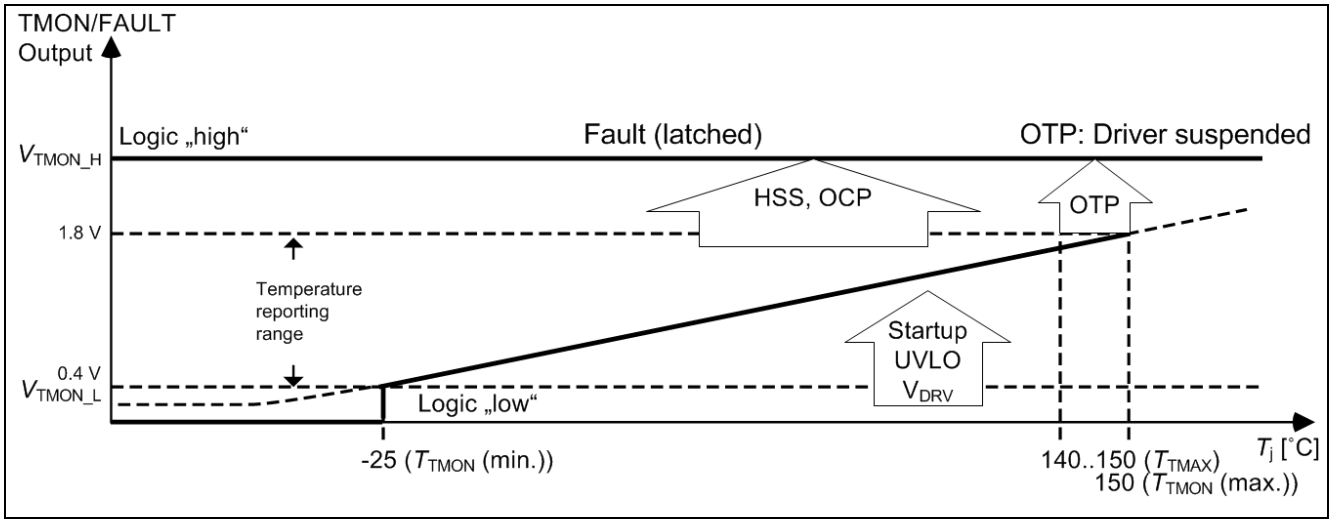


**Figure 5 Thermal monitoring and protection**

*Note: Temperature reporting below $T_{TMON\_min}$ occurs with limited accuracy. $T_{TMON\_min}$ is being defined by the corresponding controller detection threshold for logic 'L'.*

The reported voltage as function of temperature follows this equation:

$$V_{TMON} = 0.6V + 8\,{}^{mV}\!/_{K} \cdot T(°C) \quad (1)$$

### 5.4.3 Undervoltage Lockout (UVLO)

The power stage should not be operated when its supply voltages are out of the nominal range. UVLO conditions occurring during power up and power down must be accommodated by proper sequencing. An UVLO condition under normal operation can indicate a problem with the driver voltage and must be handled with a shutdown to prevent damage to the power stage.

A primary UVLO circuit monitors VCIN. Only after having VCIN in regulation range the UVLO monitoring on VDRV takes place. During startup UVLO on VDRV is being signaled by keeping TMON/FAULT low.

With VCIN being below $V_{UVLO1\_R}$ at startup the driver is inactive, PWM and TMON/FAULT are held low.
When VCIN exceeds $V_{UVLO1\_R}$ the driver becomes active, pin PWM is being enabled as input and held internally at its tri-state level of $V_{PWM\_O}$. Then VDRV determines TMON/FAULT:
- Below $V_{UVLO2\_R}$ TMON/FAULT remains 'low'.
- When VDRV exceeds $V_{UVLO2\_R}$ TMON/FAULT is released and reports temperature.
- When VDRV falls below $V_{UVLO2\_F}$ for 3 consecutive cycles or 15 µs (typ.) TMON/FAULT is being pulled 'low'.

If at startup VCIN and/or VDRV are below their respective undervoltage lockout rising thresholds ($V_{UVLO1\_R}$, $V_{UVLO2\_R}$) GL and GH remain disabled. Once these thresholds have been cleared, the driver provides GL output

signal following PWM. When the voltage $V_{BOOT}$-$V_{SW}$ has been exceeding $V_{UVLOboot\_R}$, GH is being released to respond to PWM.

When VCIN and/or VDRV are falling below their respective undervoltage lockout falling thresholds ($V_{UVLO1\_F}$, $V_{UVLO2\_F}$) the driver disables its outputs GH and GL to drive the MOSFETs.

When the voltage $V_{BOOT}$-$V_{SW}$ has been falling below $V_{UVLOboot\_F}$ for 3 consecutive PWM cycles the driver will be disabled.

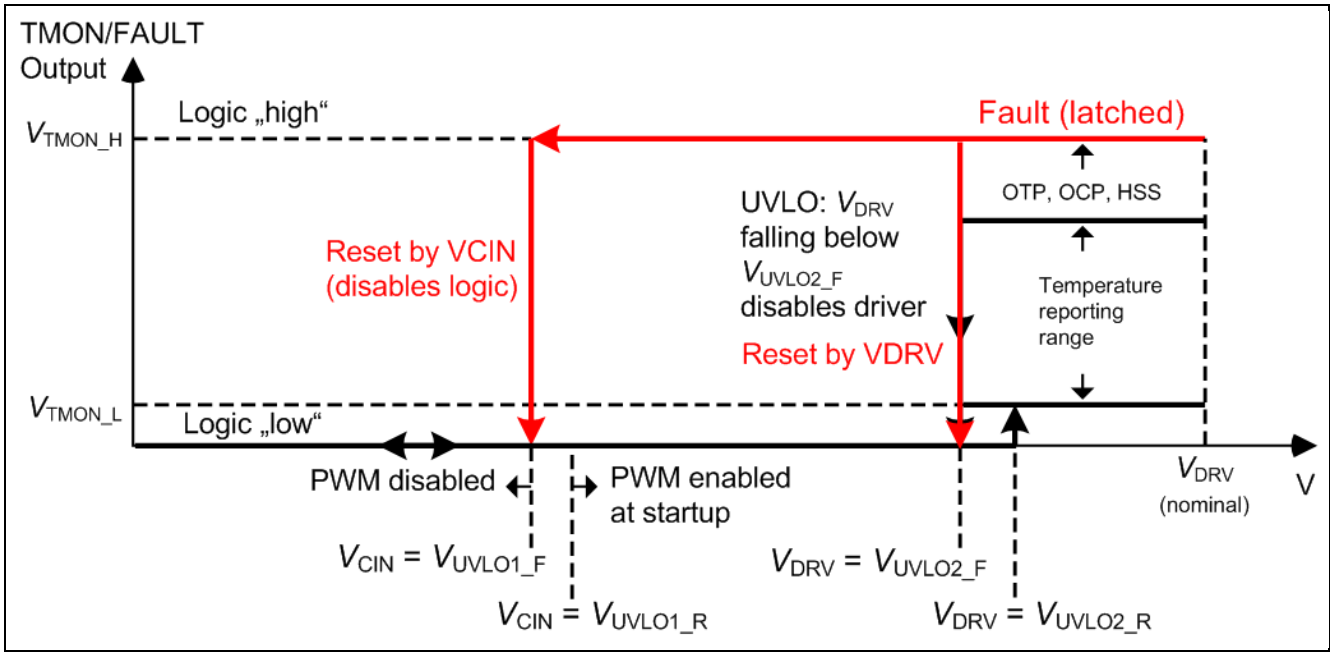


**Figure 6 Output Signal at TMON/Fault**

### 5.4.4 BOOT - Undervoltage Protection ($UVLO_{BOOT}$)

The voltage between BOOT and SW pins (boot-voltage) is being monitored when VCIN and VDRV have been clearing their respective UVLO conditions. At startup, the LS-MOSFET gate (GL) is enabled to respond to the PWM signal when VDRV is being active. If the voltage at the boot capacitor is insufficient to clear the $V_{UVLOboot\_R}$ threshold, GH remains disabled until the active LS-MOSFET has forced sufficient charge onto the boot capacitor during the PWM “L” state. When the boot capacitor voltage exceeds $V_{UVLOboot\_R}$, the GH output for the gate drive of the HS-MOSFET is enabled.

At startup and anytime when the boot voltage is below $V_{UVLOboot\_F}$ an internal boot-error flag is set. The boot-error flag is being reset when the boot voltage exceeded $V_{UVLOboot\_R}$.

If during the falling edge of the PWM (from ‘H’ to tri-state or from ‘H’ to ‘L’) the $UVLO_{BOOT}$ error flag is set, an internal counter increases by one. When the counter reaches three, the driver outputs GH/GL are being disabled (i.e. latched in tri-state), regardless of the PWM input.

To reset the driver and resume operation, the PWM input has to be held in tri-state for 19 µs (typ). After that, the $UVLO_{BOOT}$ counter is being reset to zero and the driver performs a startup sequence as described before in order to bring sufficient charge onto the boot capacitor.

The $UVLO_{BOOT}$ counter is also being reset to zero whenever during the falling edge of the PWM the $UVLO_{BOOT}$ error flag was not set, i.e. the error condition had been temporary for less than three consecutive instances of the falling edge of the PWM signal.

To prevent depletion of the boot capacitor during extended time in tri-state during regular operation, a boot refresh circuit will engage after 19 µs (typ) in consecutive tristate condition when the voltage at the boot capacitor has fallen below $V_{UVLOboot\_F}$. This circuit remains active until $V_{UVLOboot\_R}$ has been reached or the PWM input signal leaves the region of tri-state. The boot refresh circuit is powered by $V_{IN}$. To ensure full effectiveness the voltage difference ($V_{IN}$-$V_{SW}$) should be more than 4.8 V.

If the driver was disabled due to an $UVLO_{BOOT}$ error, it will be reset to resume operation when VCIN and/or VDRV will be re-cycled or PWM will be held at tri-state level for more than 19 µs (typ).

In case of an $UVLO_{BOOT}$ error it is expected that the system controller discovers a missing phase, phase current mismatch, excessive temperature or OCP events on other phases and initiates shutdown.

### 5.4.5 Current Monitoring and Overcurrent Protection (OCP)

The TDA21321 senses and reports current back to the controller via the voltage at IMON. This voltage is a filtered representation of the voltage at IMONREF. IMONREF is a current source output:

$$I_{IMONREF} = I_{OUT} \cdot a_{CS} \quad (2)$$

The voltage at IMONREF depends on the impedance its current is being passed through. A recommended target voltage at zero output current is 1.5V (common mode voltage). The series resistor $R_{IMONREF}$ between IMONREF and the common mode voltage reference sets the voltage gain of the current sense according to:

$$V_{IMONREF} = V_{IMONREF\_CM} + R_{IMONREF} \cdot I_{MONREF} \quad (3)$$

The output current is now represented by the voltage difference between IMON and $V_{IMONREF\_CM}$. $V_{IMONREF\_CM}$ is the voltage at IMONREF when the load current is zero.

$$V_{IMON} - V_{IMONREF\_CM} = I_{OUT} \cdot R_{IMONREF} \cdot a_{CS} \quad (4)$$

$a_{cs}$ is given in Table 10 for VDRV = 5V. If VDRV has been chosen to be different, $a_{cs}$ has to be calculated as:

$$a_{CS} = 6.67\,{}^{\mu A}\!/_{A} \cdot \left(1 + \left(VDRV\left[V\right] - 5\right) \cdot 0.012\right) \quad (5)$$

A filter capacitor $C_{IMON}$ of 10 pF has to be placed between IMON and $V_{IMONREF\_CM}$ (reference voltage pin of $R_{IMONREF}$). $C_{IMON}$ and $R_{IMONREF}$ have to be arranged in a tight loop close to the pins of the TDA21321. An additional resistor $R_{IMON}$ has to be connected in parallel to $C_{IMON}$. Its location is flexible and can also be at the controller. The value for $R_{IMON}$ should be chosen identical to $R_{IMONREF}$ within the range of 200 Ω to 1 kΩ.

At the voltage receiver side the measurement loop has to be closed. It is important to not inject noise into this loop. Therefore differential routing of IMON and IMONREF is required.

For example, having a permissible 500 mV voltage range at the receiver side to report positive current of 100 A, the resistor that has to be used in the IMONREF path can be calculated as:

$$V_{IMON} - V_{IMONREF\_CM} = 500mV$$
$$R_{IMONREF} = \frac{V_{IMON} - V_{IMONREF\_CM}}{I_{OUT} \cdot a_{CS}} = \frac{500mV}{100A \cdot 6.67 \cdot 10^{-6}} = 750\Omega \quad (6)$$

Having a resistor value of 348 Ω will result in the following voltage difference:

$$V_{IMON} - V_{IMONREF\_CM} = R_{IMONREF} \cdot I_{OUT} \cdot a_{CS} = 348\Omega \cdot 100A \cdot 6.67 \cdot 10^{-6} = 232mV \quad (7)$$

The sensing of current occurs in the HS-MOSFET and the LS-MOSFET during their respective on-times. During tri-state condition both MOSFETs are in off-state without sensing. The current reported is then zero. If the tri-state condition was present for more than 19 µs (typ.), current reporting resumes with a delay of 1 µs (typ.).

OCP: By design of the application the current should never exceed the OCP tripping threshold $I_{OCPtrip}$. The duty cycle is being truncated by the TDA21321 when the current exceeds $I_{OCPtrip}$. This prevents the part from being destroyed by excessive current. A counter is being increased counting consecutive PWM duty cycle truncations. The counter is being reset at the first non-truncated PWM duty cycle. When the counter reaches the value of 10, a fault will be reported at TMON/FAULT by pulling it to ‘high’ level signaling the PWM controller the need for immediate action to prevent catastrophic failure. This fault is latched and will be released when VCIN and/or VDRV are being re-cycled.

### 5.4.6 Shoot Through Protection

The TDA21321 driver includes gate drive functionality to protect against shoot through. In order to protect the power stage from overlap, both high-side and low-side MOSFETs being on at the same time, the adaptive control circuitry monitors specific voltages. When the PWM signal transitions to low, the high-side MOSFET will begin to turn-off after the propagation delay time t_pdlu. When $V_{GS}$ of the high-side MOSFET is discharged below 1 V (a threshold below which the high-side MOSFET is off), a secondary delay t_pdhl is initiated. After that delay the low-side MOSFET turns on regardless of the state of the “PHASE” pin. It ensures that the converter can sink current efficiently and the bootstrap capacitor will be refreshed appropriately during each switching cycle. See Figure 9 for more detail.

# 6 Application

## 6.1 Implementation

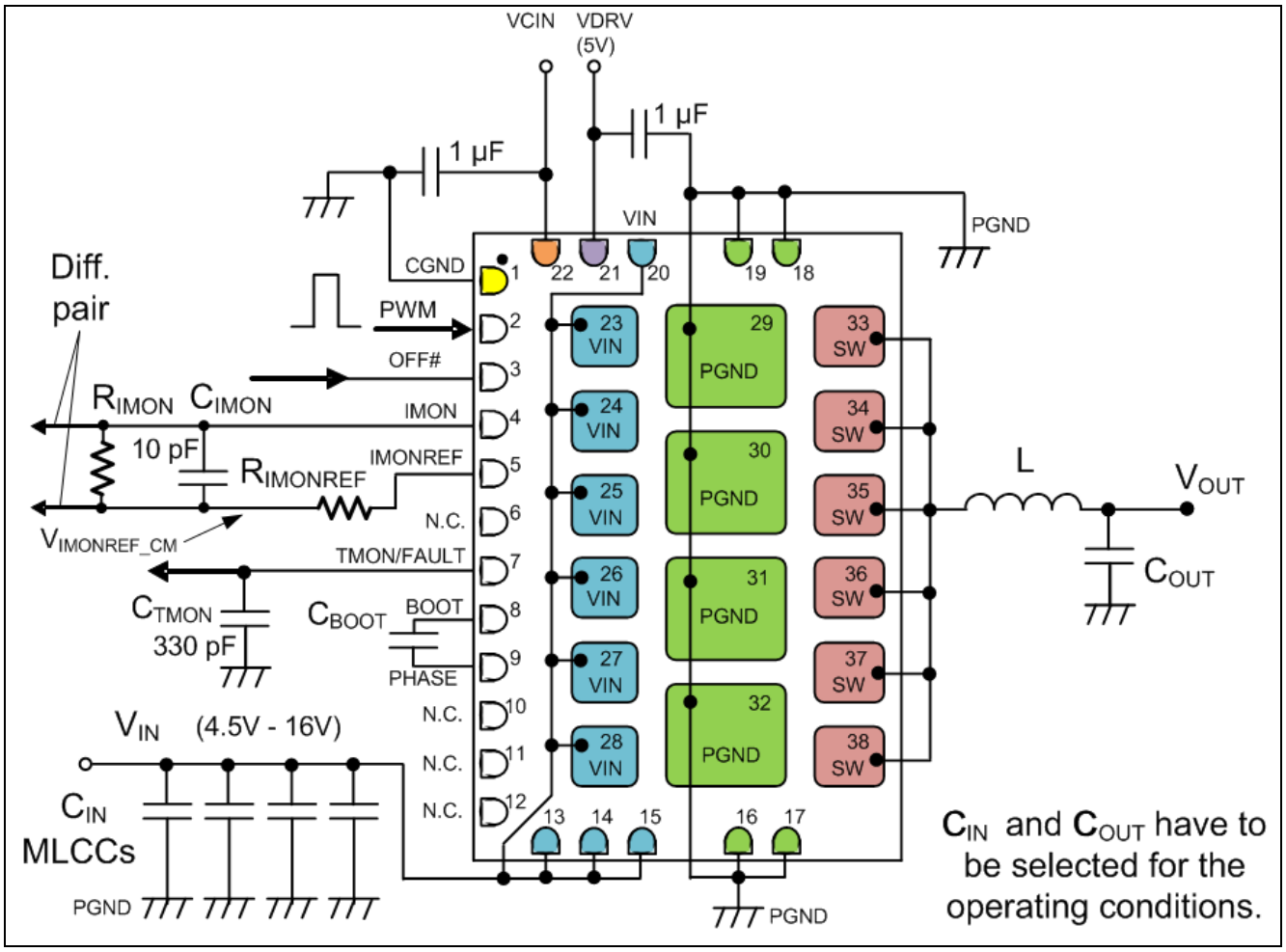


**Figure 7 Pin Interconnection Outline (transparent top view)**

*Note:*

1. *Pin 9 (PHASE) is internally connected to the SW pads 33-38.*
2. *The capacitor $C_{TMON}$ is used to filter noise from the TMON/FAULT connection. The capacitor has to be placed at the input of the controller. Its value should be set between 0.1 nF and 0.5 nF.*
3. *$R_{IMON}$ should be chosen identical to $R_{IMONREF}$.*
4. *$C_{IMON}$ and $R_{IMONREF}$ have to be arranged in a tight loop close to the pins of the TDA21321.*
5. *To lower the pre-bias voltage at Vout to below $V_{SW\_0}$, place a resistor from Vout to GND.*
6. *$C_{IN}$ should consist of a 0.1 µF and a 1 µF very close to the pins 15/16 and a 1 µF capacitor at pins 19/20. In addition place sufficient MLCCs in relative proximity of each power stage to deliver energy for the on-time of the HS-MOSFET.*
7. *The value of capacitor $C_{BOOT}$ should be chosen according to the corresponding application note.*

## 6.2 Typical Application

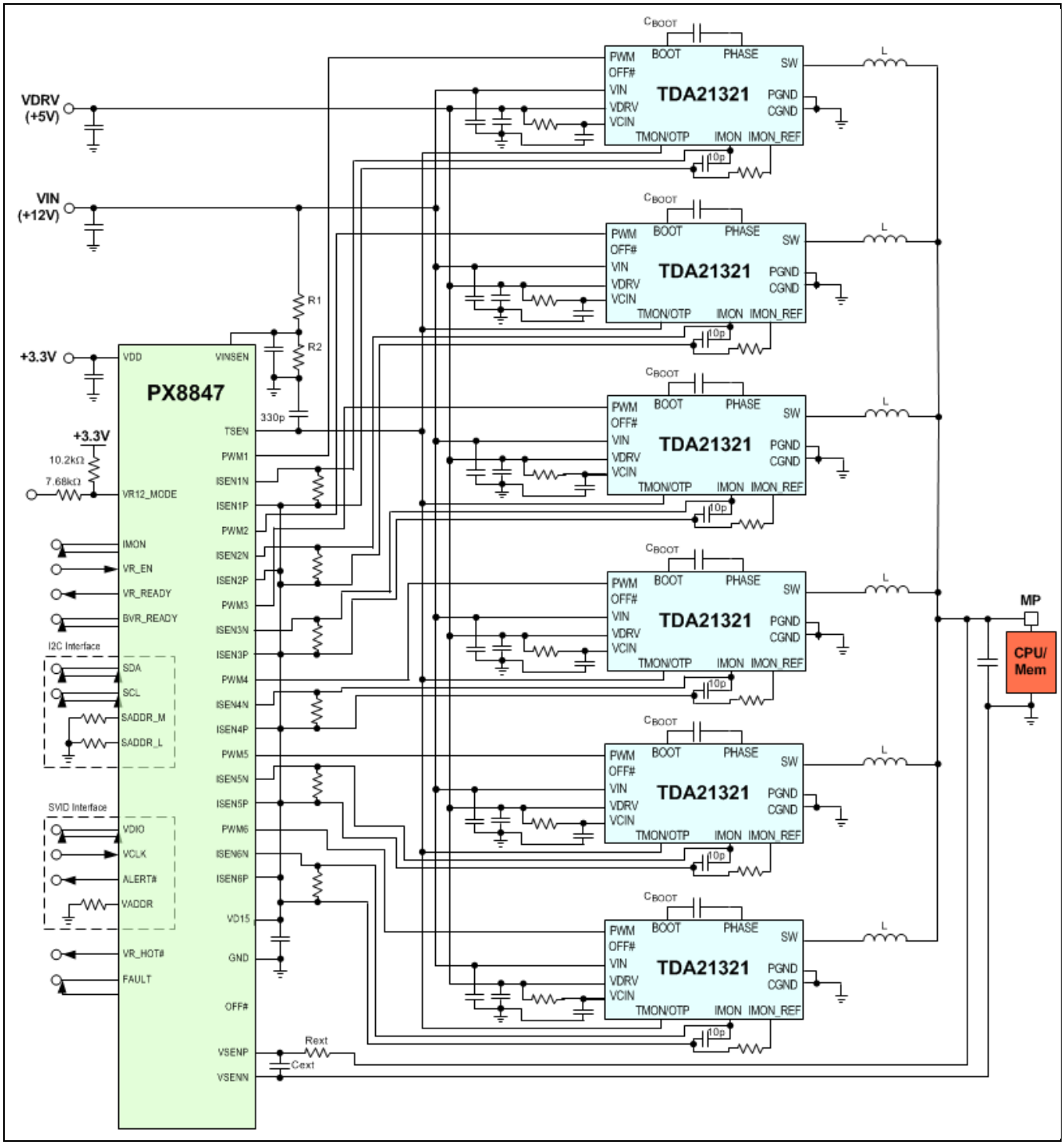


**Figure 8 Six-phase voltage regulator - typical application (simplified schematic)**

# 7 Gate Driver Timing Diagram

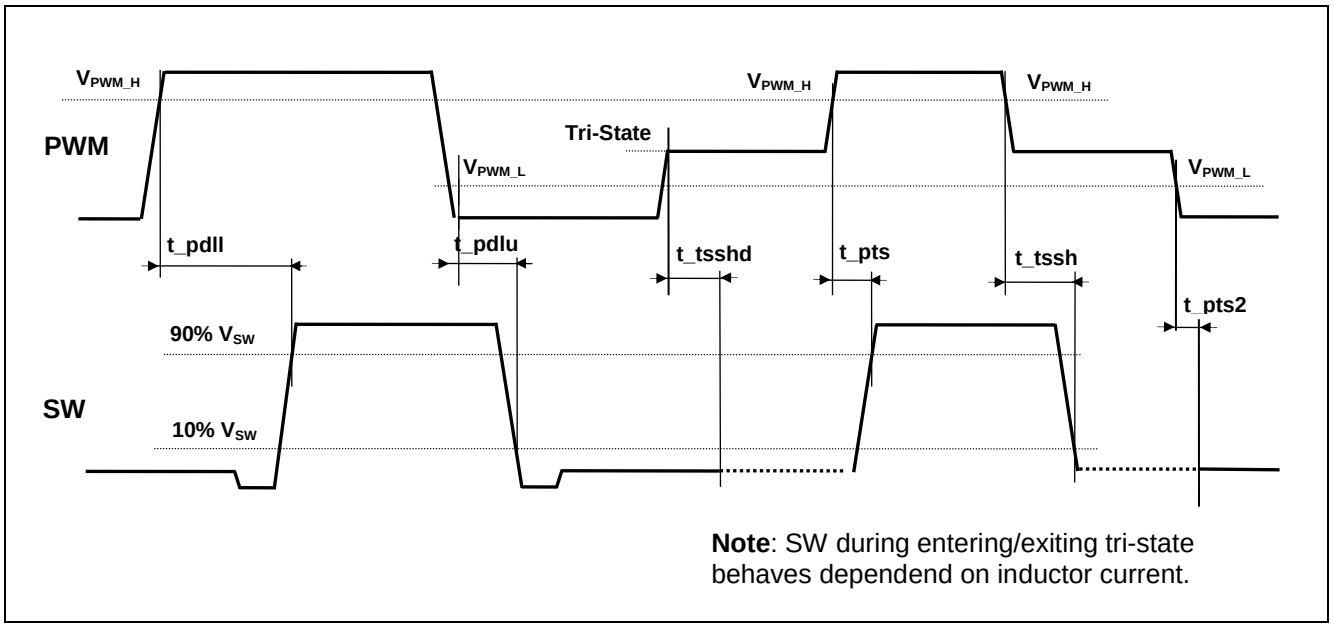


**Figure 9 Adaptive Gate Driver Timing Diagram**

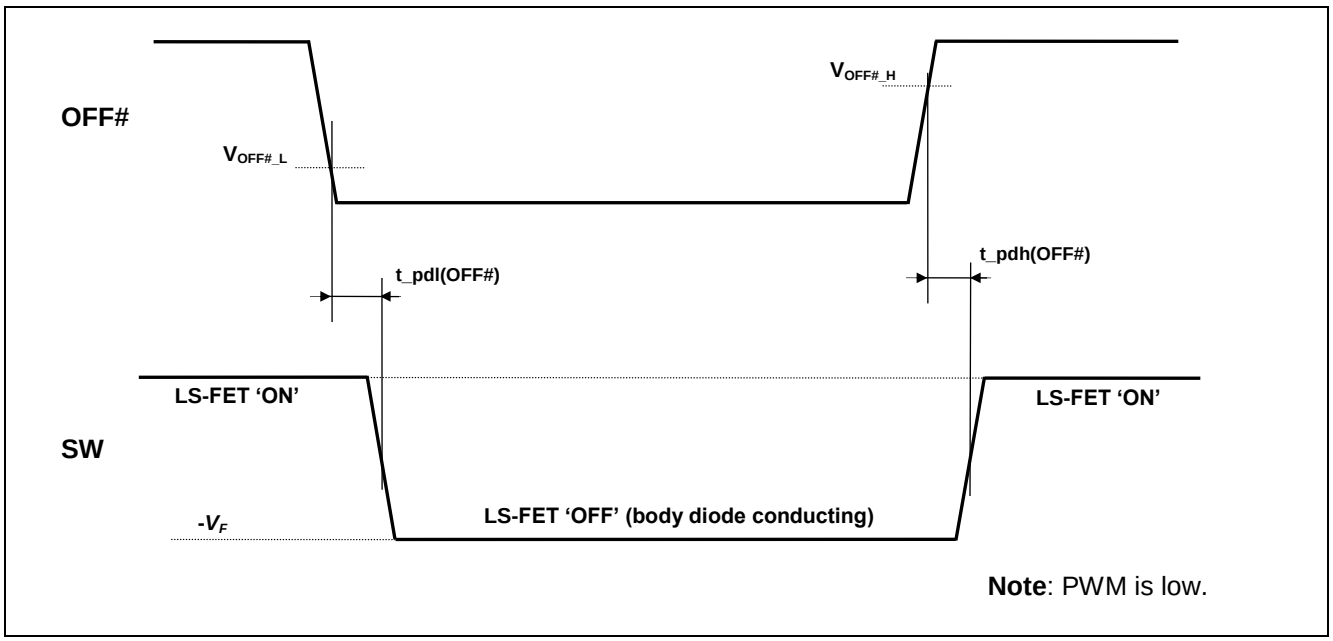


**Figure 10 OFF# Timing Diagram**

# 8 Performance Curves – Typical Data

Operating conditions (unless otherwise specified): VIN = +12 V, VCIN = VDRV = +5 V, VOUT = +1.8 V, $f_{SW}$ = 750 kHz, 180nH (Delta, HCB118080D-181, DCR = 0.19 mΩ) inductor, $T_A$ = 25 °C, airflow = 200 LFM, no heatsink. Efficiency and power loss reported herein include only TDA21321 losses.

## 8.1 Driver Current versus Switching Frequency

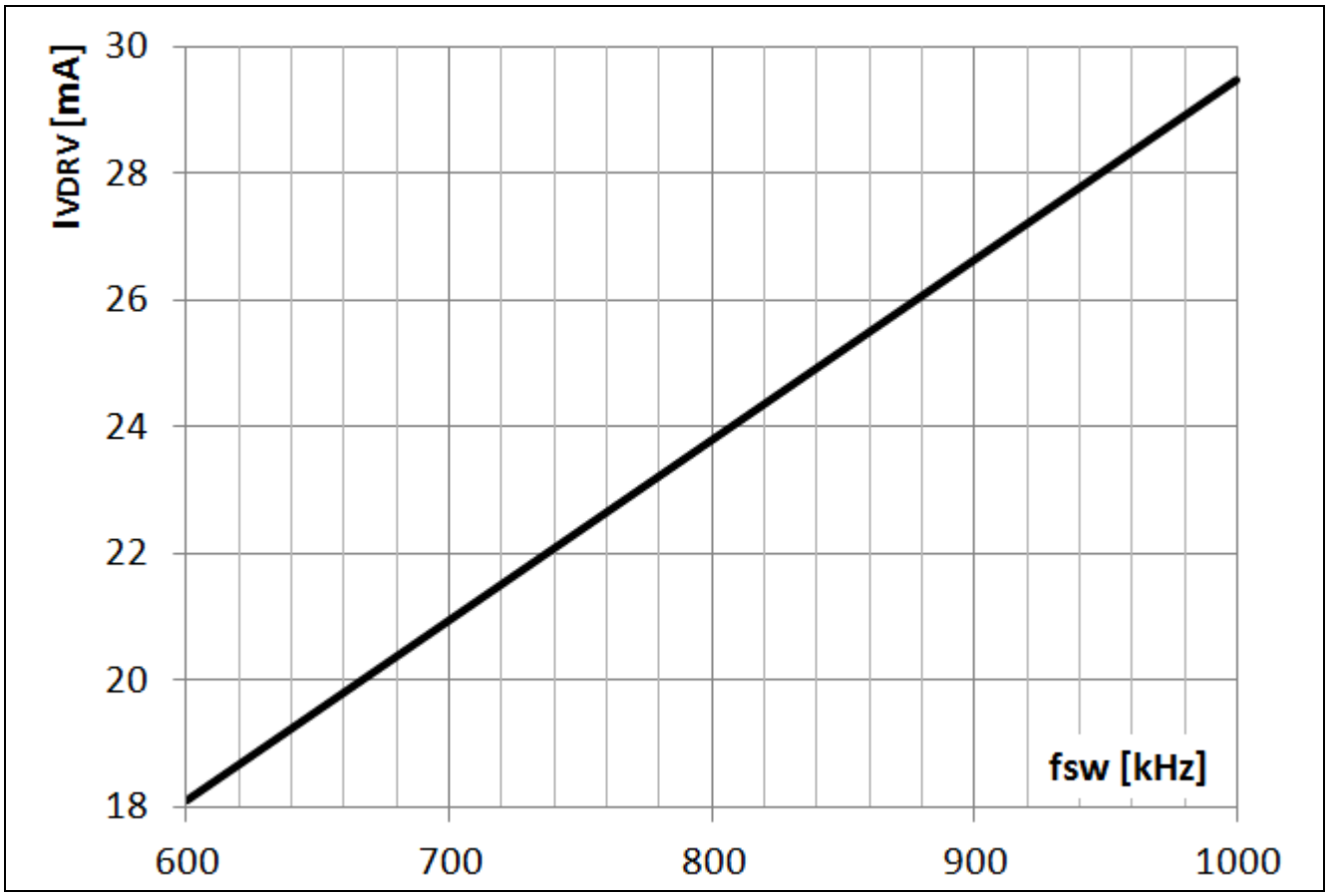


**Figure 11 Driver Current over Switching Frequency in CCM Operation**

## 8.2 Efficiency and Power Loss versus Output Voltage

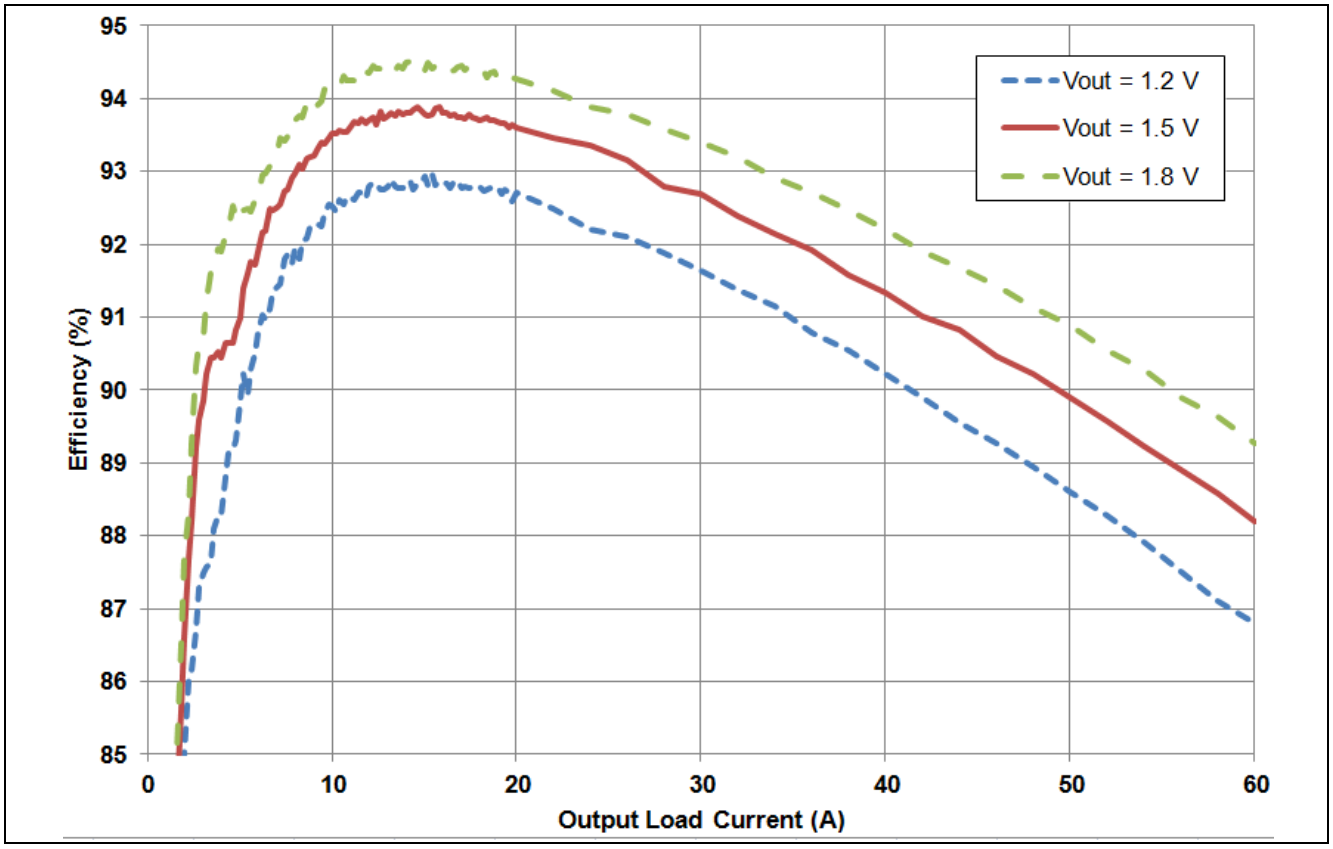


**Figure 12 Efficiency at VIN = 12 V, VCIN = VDRV = 5 V, $f_{sw}$ = 750 kHz, Parameter: VOUT**

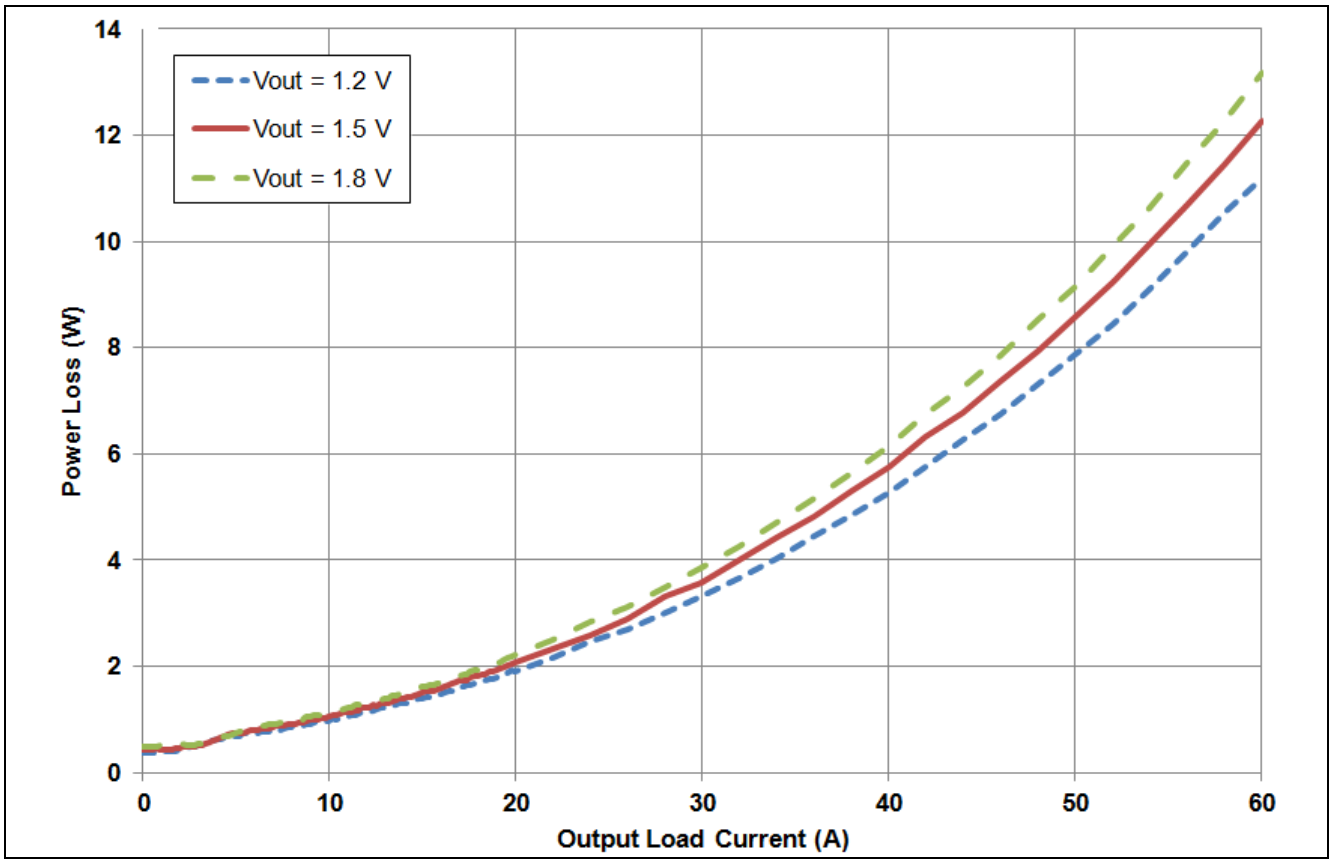


**Figure 13 Power Loss at VIN = 12 V, VCIN = VDRV = 5 V, $f_{sw}$ = 750 kHz, Parameter: VOUT**

## 8.3 Efficiency and Power Loss versus Input Voltage

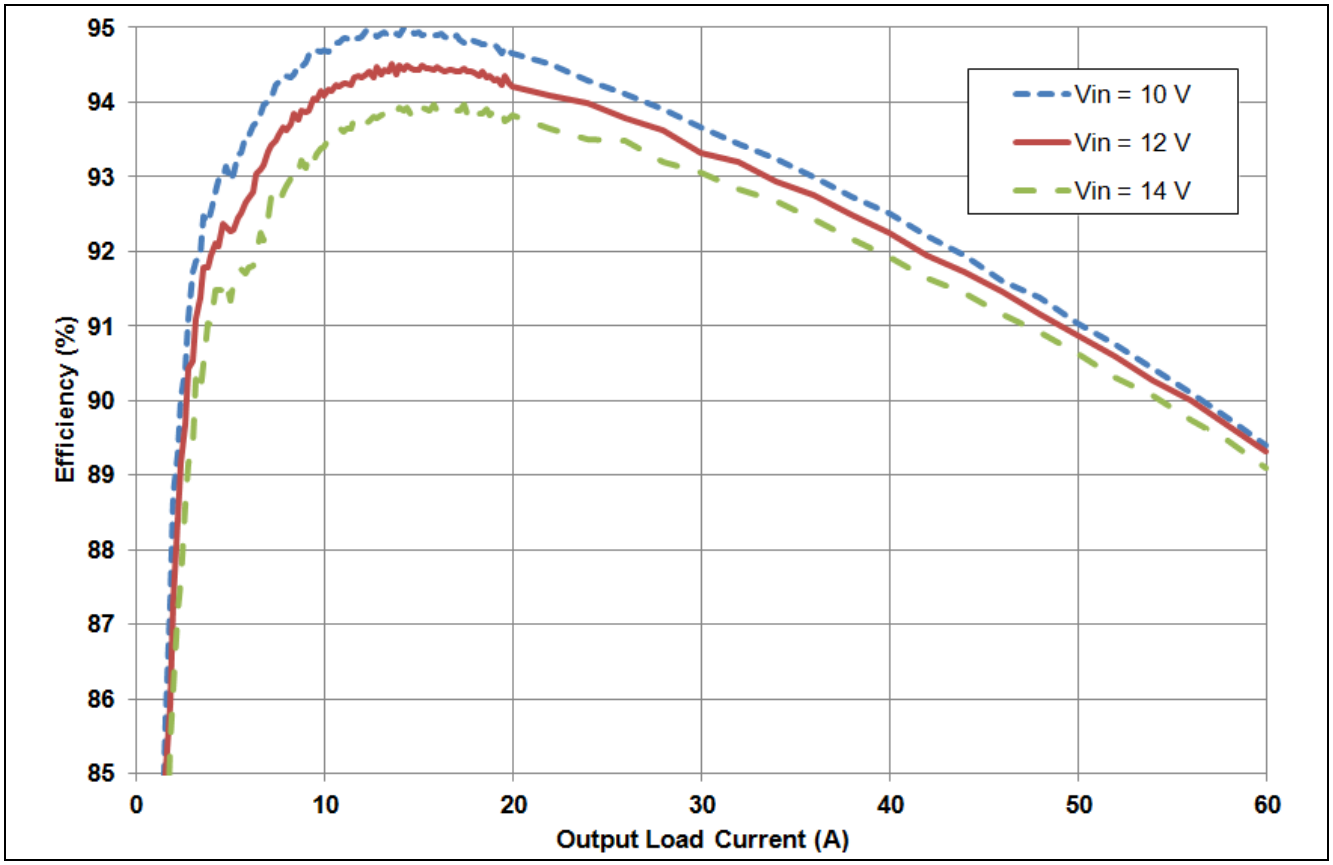


**Figure 14 Efficiency at $f_{sw}$ = 750 kHz, VCIN = VDRV = 5 V, VOUT = 1.8 V, Parameter: VIN**

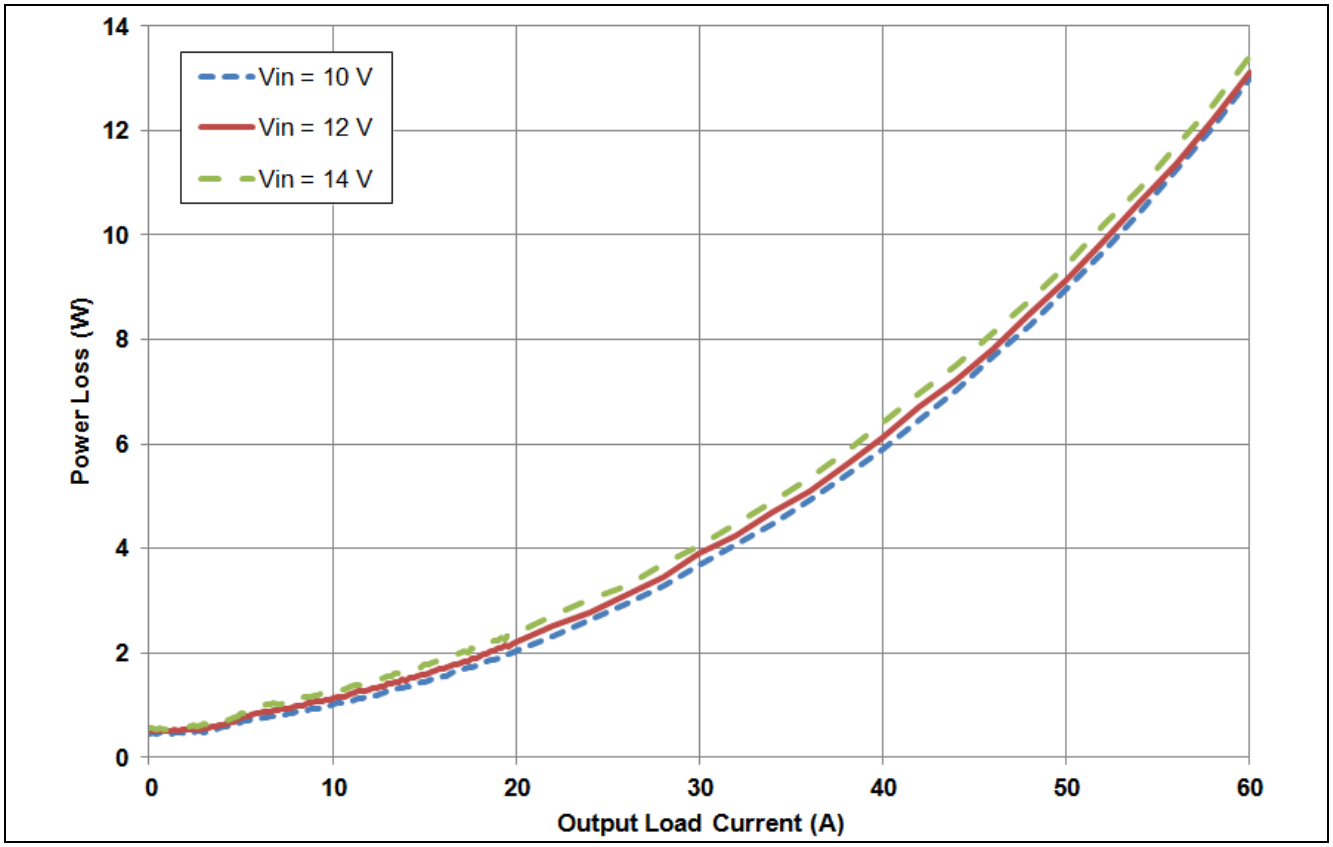


**Figure 15 Power Loss at $f_{sw}$ = 750 kHz, VCIN = VDRV = 5 V, VOUT = 1.8 V, Parameter: VIN**

## 8.4 Efficiency and Power Loss versus Switching Frequency

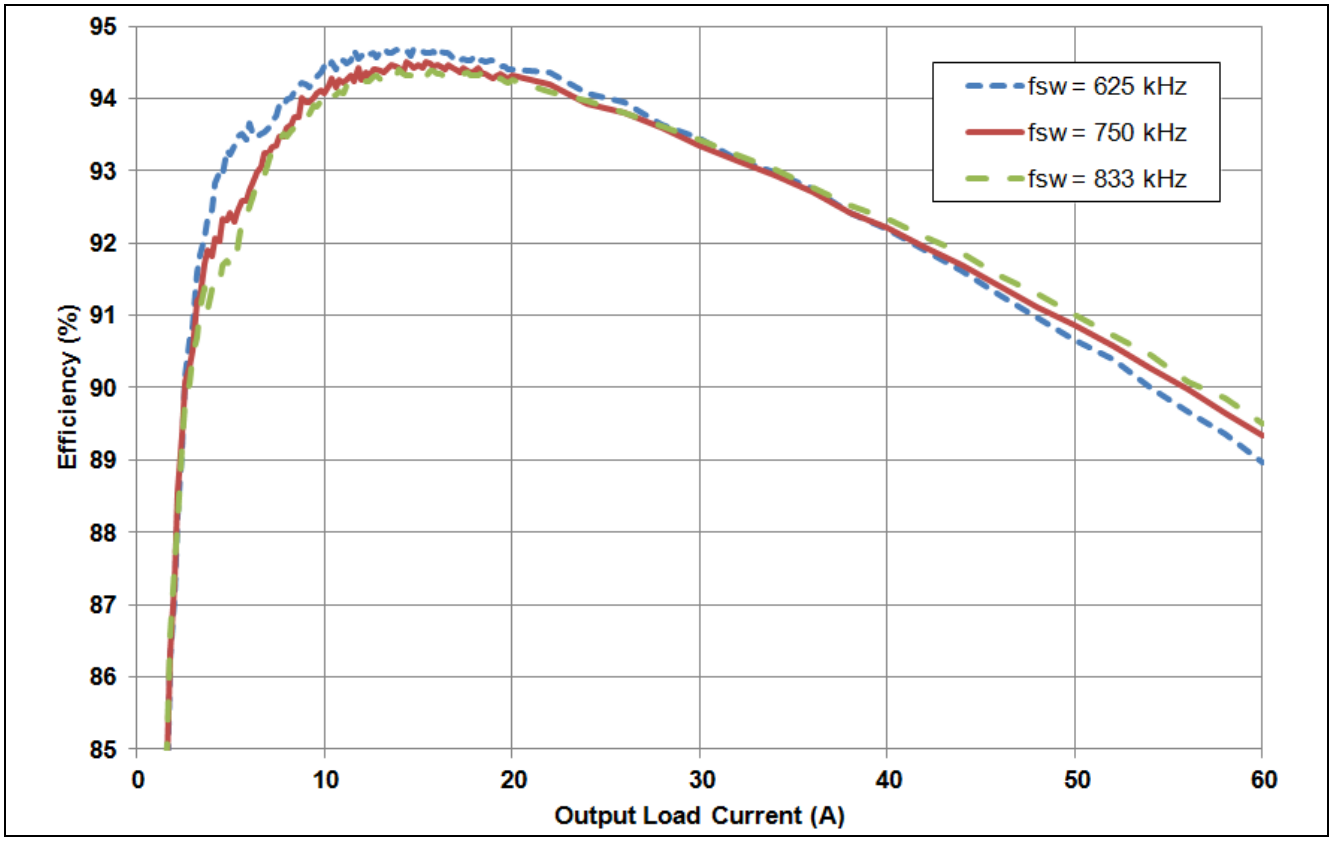


**Figure 16 Efficiency at VIN = 12 V, VCIN = VDRV = 5 V, VOUT = 1.8 V, Parameter: $f_{sw}$**

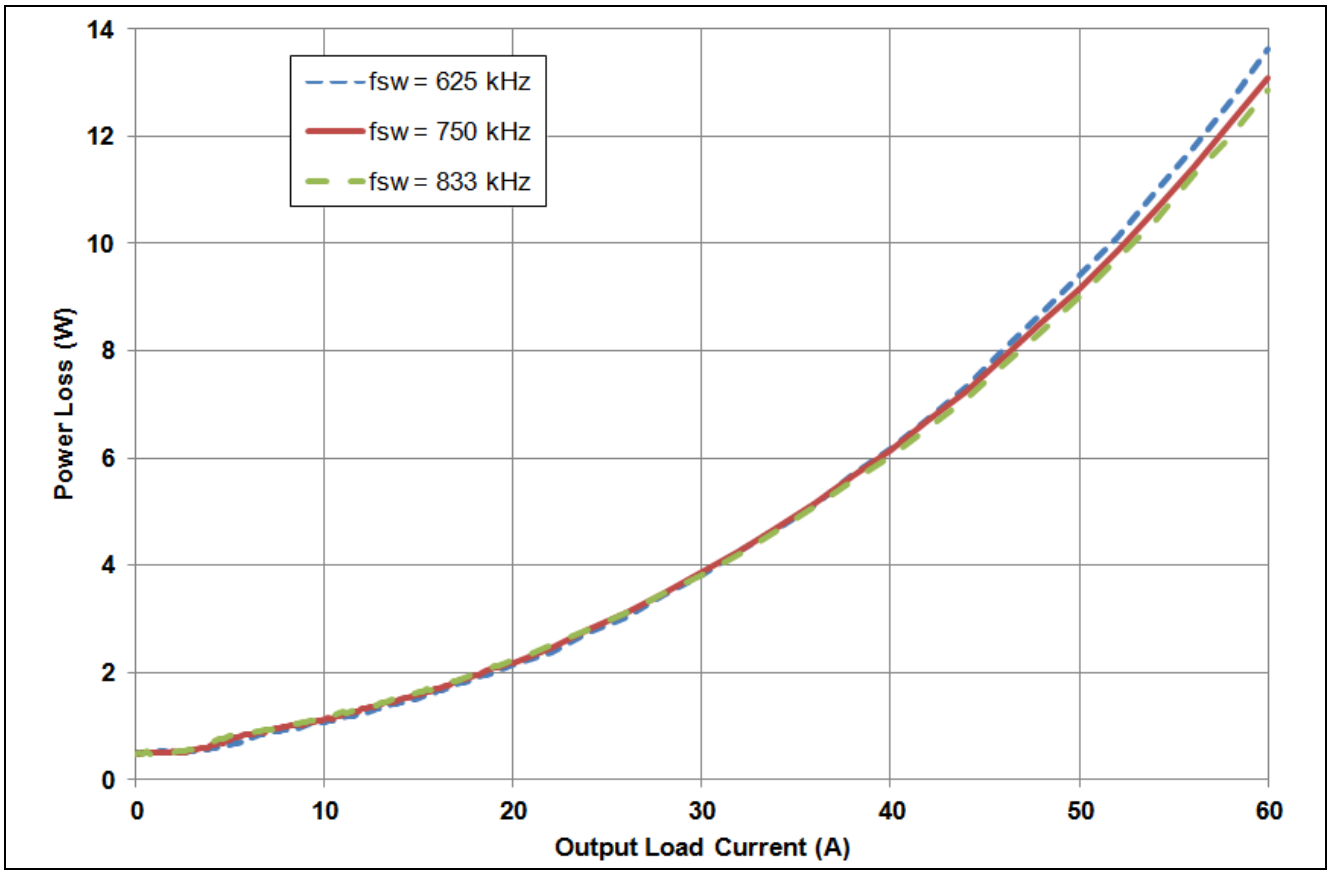


**Figure 17 Power Loss at VIN = 12 V, VCIN = VDRV = 5 V, VOUT = 1.8 V, Parameter: $f_{sw}$**

# 9 Mechanical Drawing LG-WIQFN-38-1 (6.6x4.5x0.6 mm³)

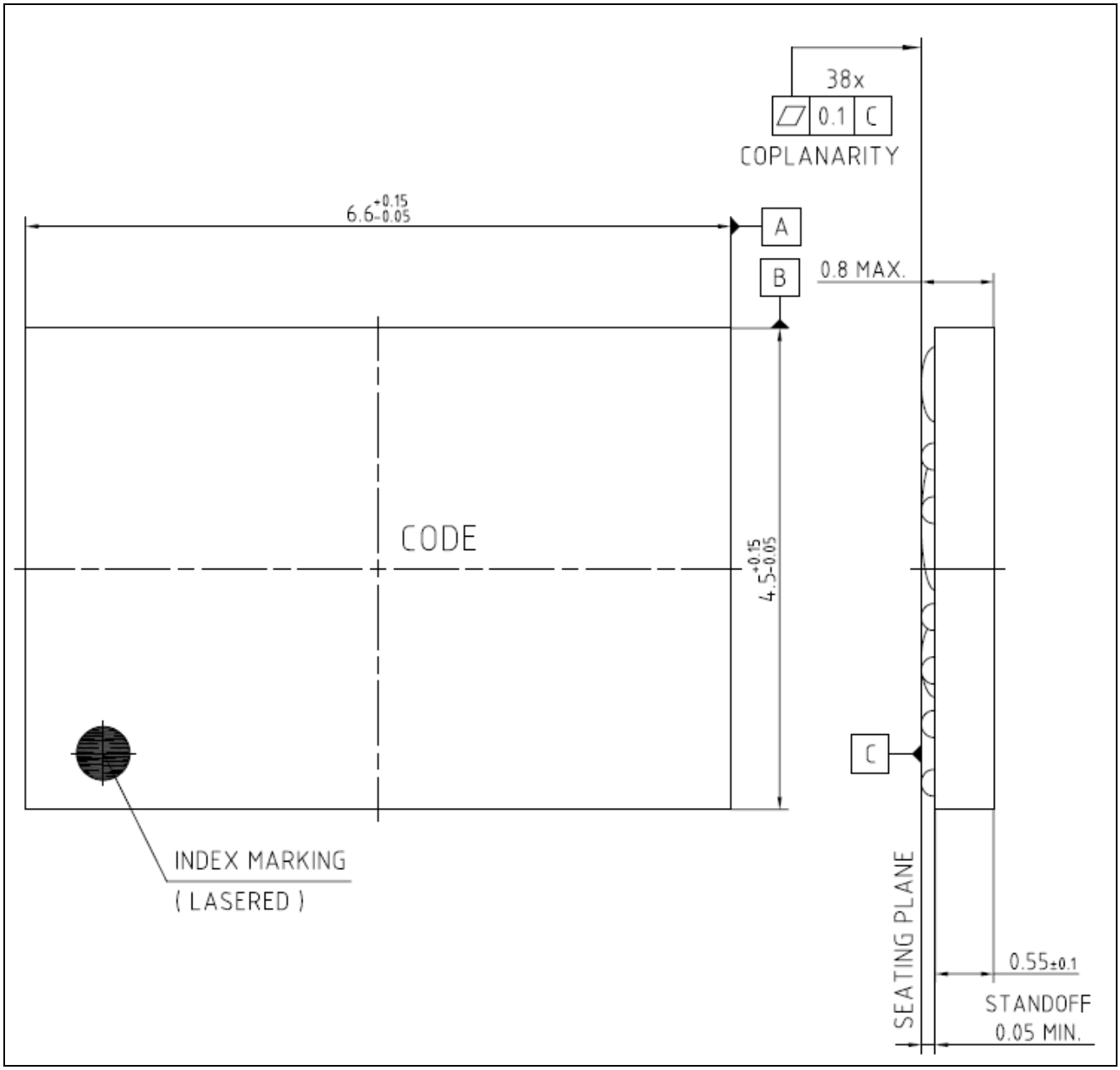


**Figure 18 Mechanical Dimensions of Package (Top and Side View) in mm**

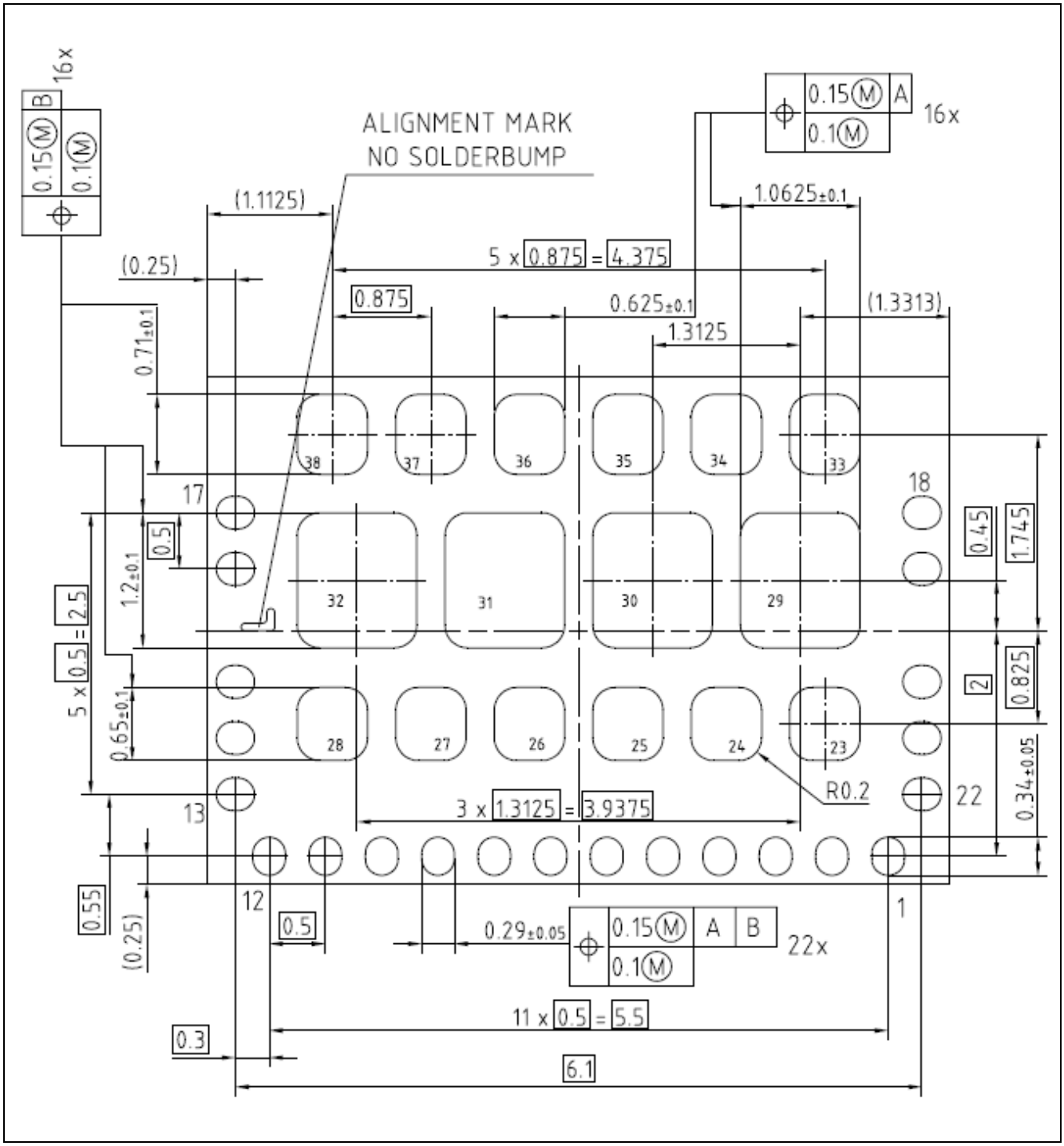


**Figure 19 Mechanical Dimensions of Package (Bottom View) in mm**

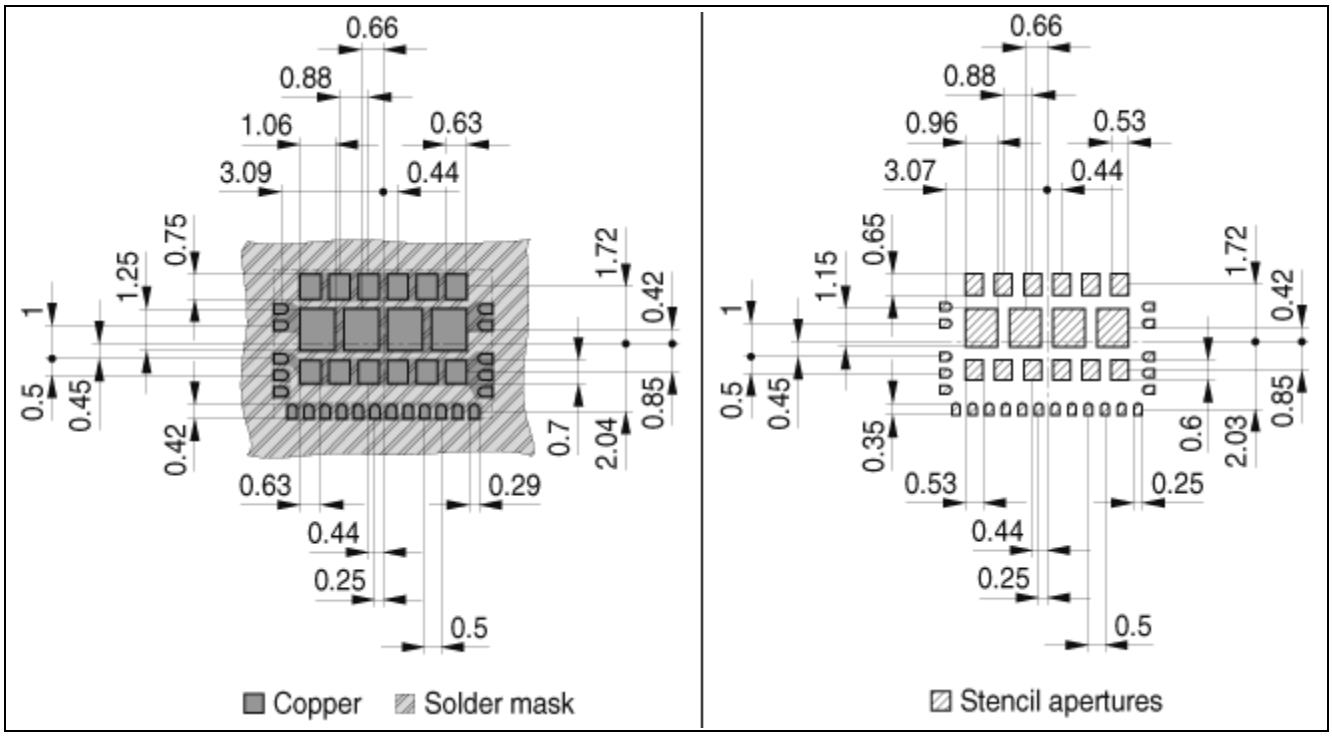


**Figure 20 Landing Pattern and Stencil Dimensions (SW on upper end) in mm**

# 10 Packaging Information

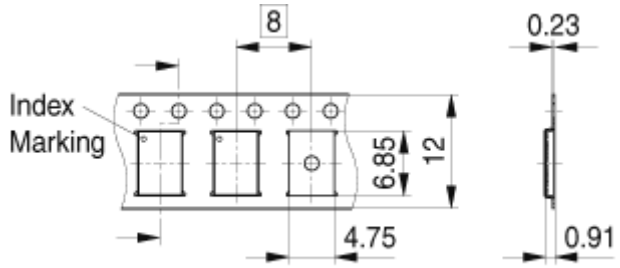


**Figure 21 Packaging Information in mm**

# 11 Board Layout Recommendations

The PCB (printed circuit board) layout design follows the listed industry standards:

- Recommended vias: 10 mil[10] hole with 20 mil via pad diameter, 12 mil hole with 24 mil via pad diameter
- Minimum (typical) via to via center distance: 25 mil (30 … 35 mil)
- Minimum feature width: 5 mil
- Minimum (typical) clearance: 5 mil (15 … 20 mil)

Commonly, 10 mil via drill diameters are used for PCBs up to 150 mil thicknesses (usually 22 layers). For thicker boards, 12 mil vias are recommended. To reduce voltage spikes caused by parasitic circuit inductance, all primary decoupling capacitors for VIN, VDRV, BOOT and VCIN should be of MLCC type, X6S or X7R rated and located at the same board side as the powerstage close to their respective pins. This is especially important for the VIN to PGND MLCCs.

Electrical and thermal connection of the powerstage to the PCB is crucial for achieving high efficiency. Therefore, vias in VIN and PGND pads are required in the pad areas to connect most effectively to other power and PGND layers. Bigger value MLCC input capacitors should be placed at the bottom side of the PCB close to the vias of the powerstage's VIN and PGND pads. To reduce the stray inductance in the current commutation loop it is strongly recommended to have the 2nd layers from the top and the bottom of the board to be monolithic ground planes. All logic and signal connections between powerstage and controller should be embedded between two ground layers. The routing of the current sense lines back to the controller has to be done differentially, for example with 5 mil spacing and 10 – 15 mil distances to other potentials. If the PCB features more than 10 layers, the passive components associated with the current sense lines should be located only at the top side of the board. All resistors and capacitors near the powerstage should be in 0402 case size. For minimizing distribution loss to the load and maintaining signal integrity, have multiple layers/planes in parallel and ensure that the copper cross section for PGND is at least as big as it is for Vout.

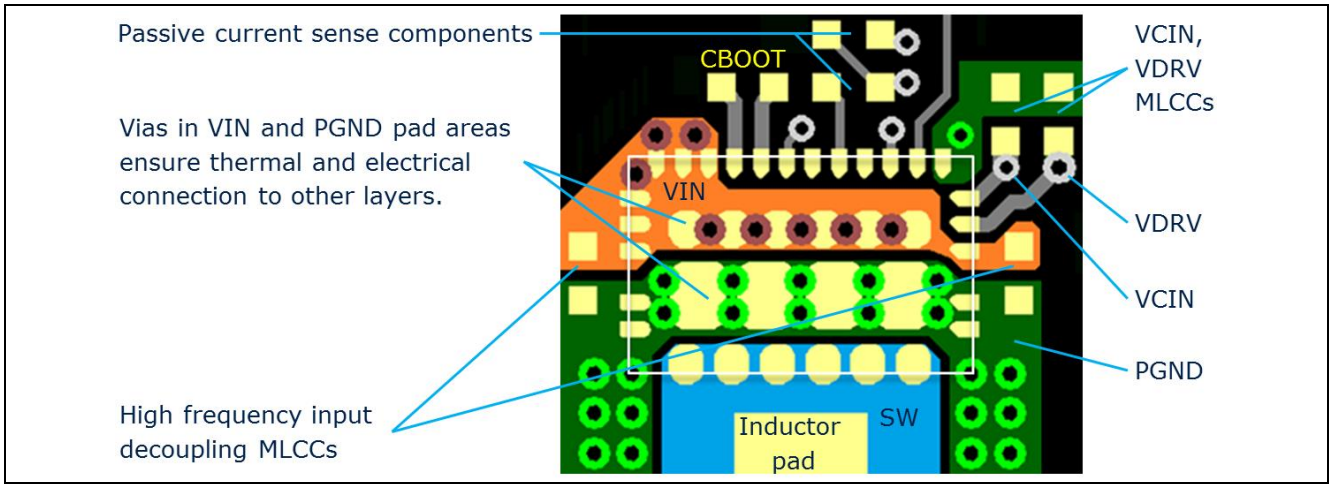


**Figure 22 Generic Board Design**

[10] Unit conversion: 1 mil = 25.4 µm

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