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S4E5B001B00A00
First Step Guide

SEIKO EPSON CORPORATION

Rev.1.0

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1. Description

This manual is a guide in the first step to do image display to the EPD panel by using S4E5B001B00A00. It explains the procedure for displaying the image of 16 levels in the EPD panel of resolution 800x600pixel. The connection with host CPU assumes the serial connection by SPI.

2. Connection

CPU is assumed mastering and it explains the SPI connection example.

Host CPU	S4E5B001B00A00	
Port input	HRDY	EPD module ready /wait signal
Port output	HD/C	EPD module command / parameter signal
Port output(SPI CS)	HCS_L	EPD module chip select signal
SPI Clock(output)	SHPICK(HDB2)	SPI clock signal
SPI data output	SHPIDI(HDB0)	SPI data (CPU output)
SPI data input	SHPIDO(HDB1)	SPI data (CPU input)

3. Setting

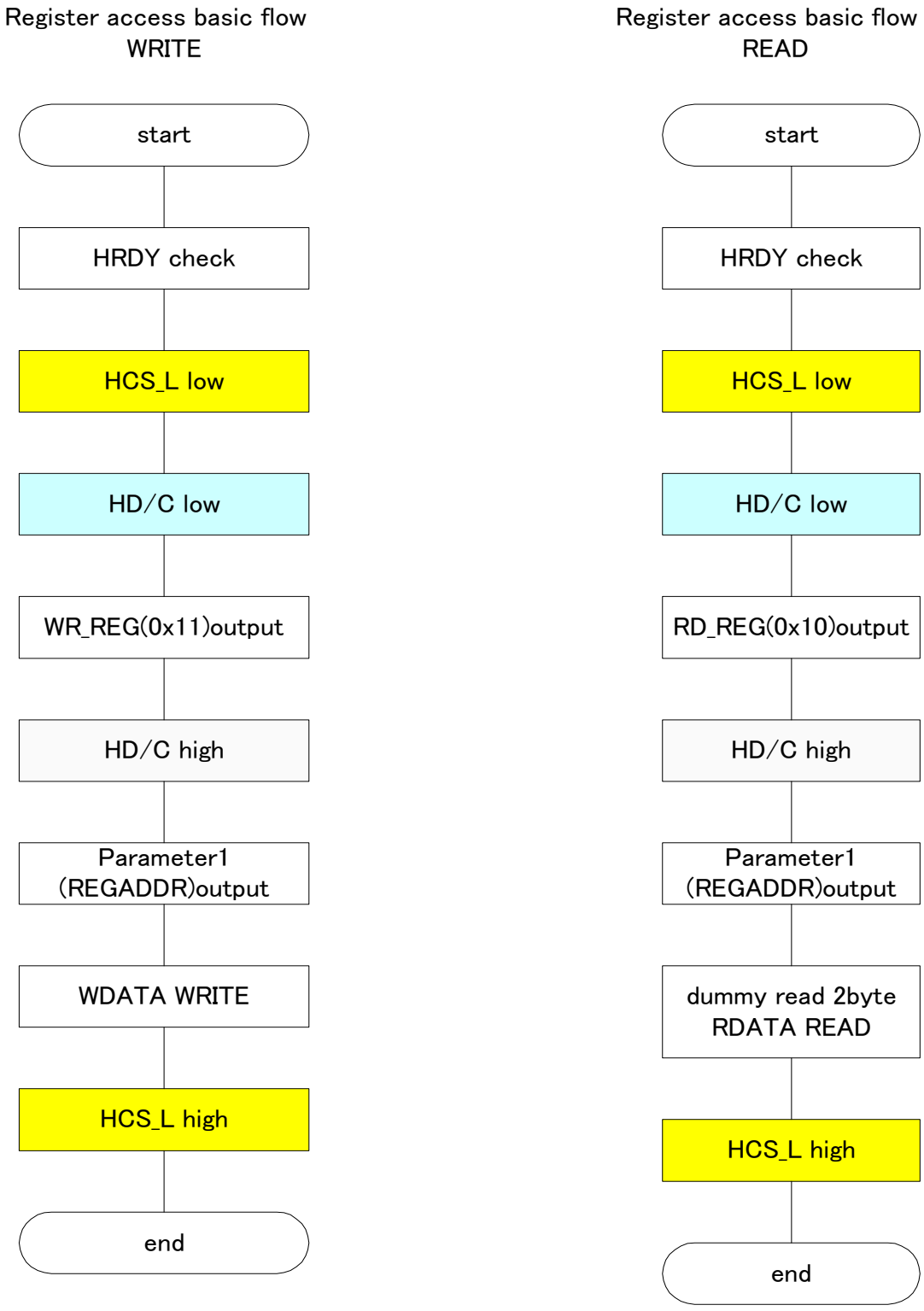
The setting of S4E5B001B00A00 is made a serial host. Serial Host type: HOSTCFG=1 and detailed HDB15=1

User Manual 4.4.1 Host Interface modes

4. Method of image display

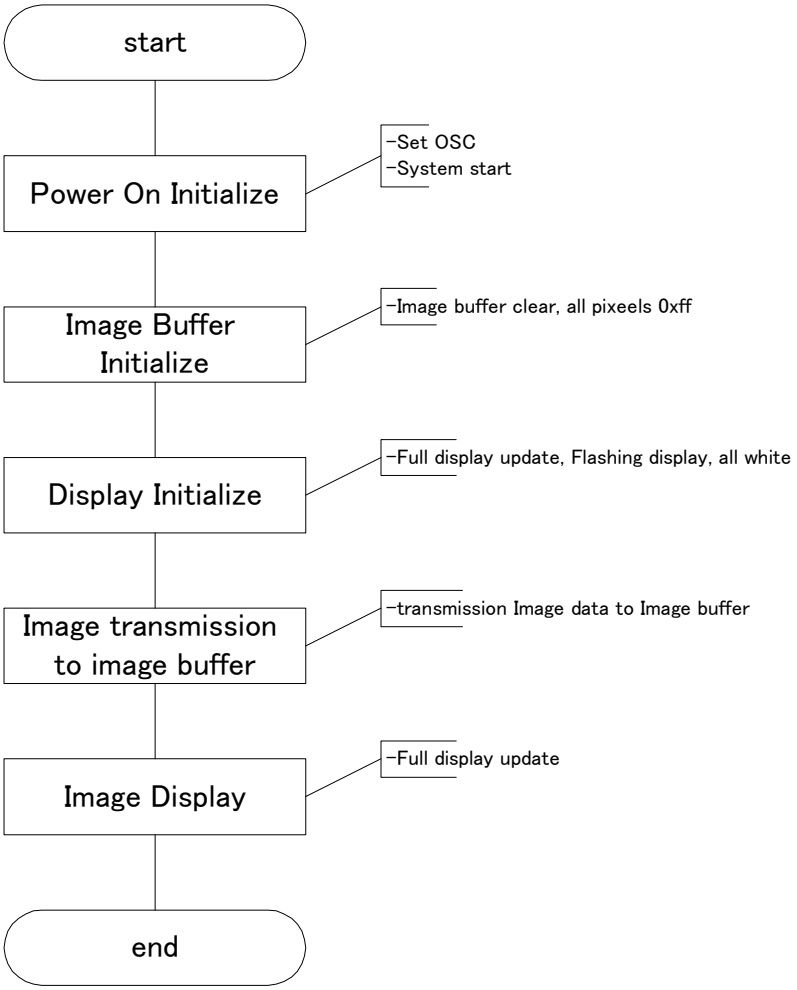
4.1 Register basis access

It explains basic flow of writing S4E5B001B00A00 in the register and reading.



4.2 Image display outline flow

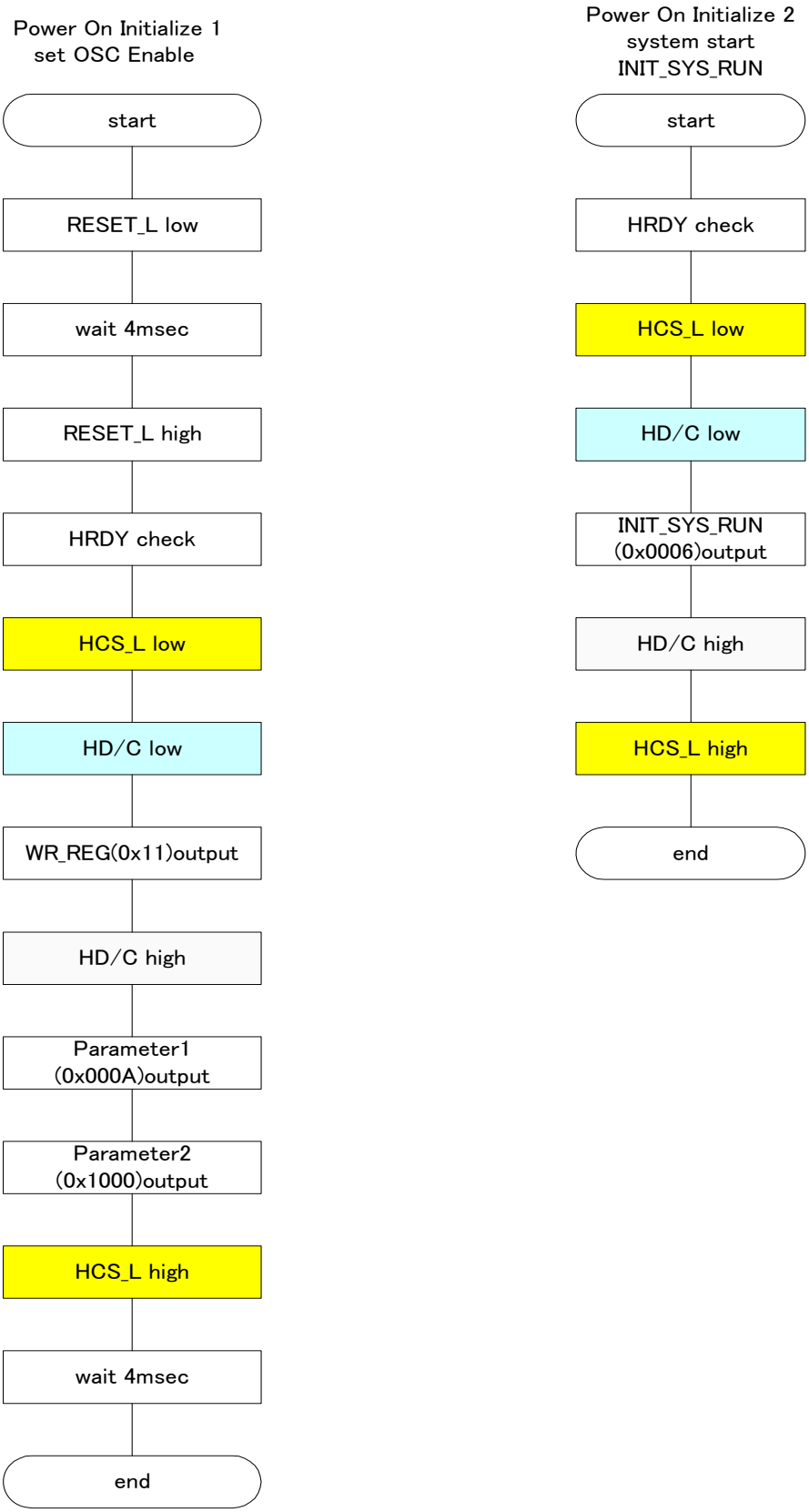
It explains the entire flow that displays the image from the initialization of S4E5B001B00A00.

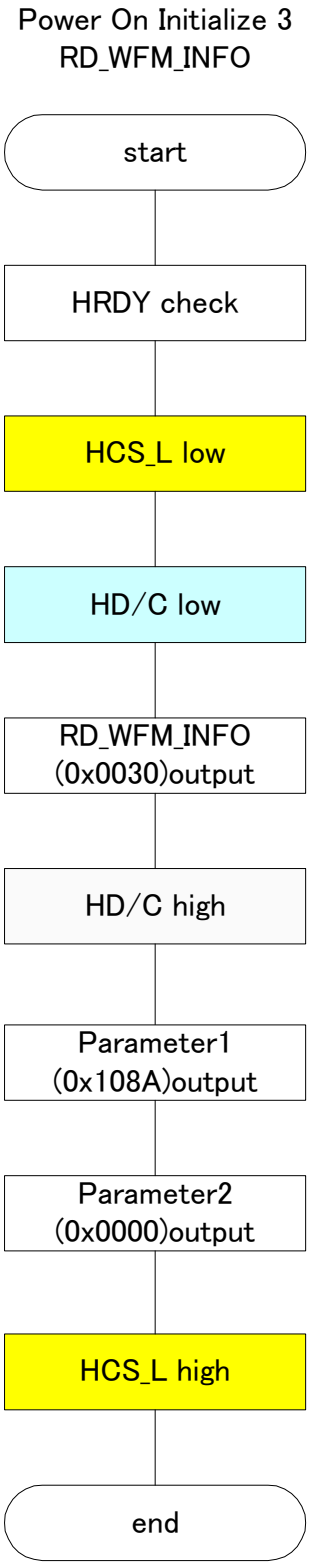


4.3 Power On Initialize

It explains the initialization flow of S4E5B001B00A00.

Refer to Fugyre 12-1: Power On Initialize Programming flow of User Manual P.107.




Power On Initialize 3
RD_WFM_INFO
start
HRDY check
HCS_L low
HD/C low
RD_WFM_INFO
(0x0030)output
HD/C high
Parameter1
(0x108A)output
Parameter2
(0x0000)output
HCS_L high
end

4.4 Image Buffer Initialize

It explains the initialization flow of Image Buffer of S4E5B001B00A00. White(0xFF) is written in Image Buffer, and white is displayed on the screen of EPD afterwards.

Refer to Fugyre 12-1: Power On Initialize Programming flow of User Manual P.108.

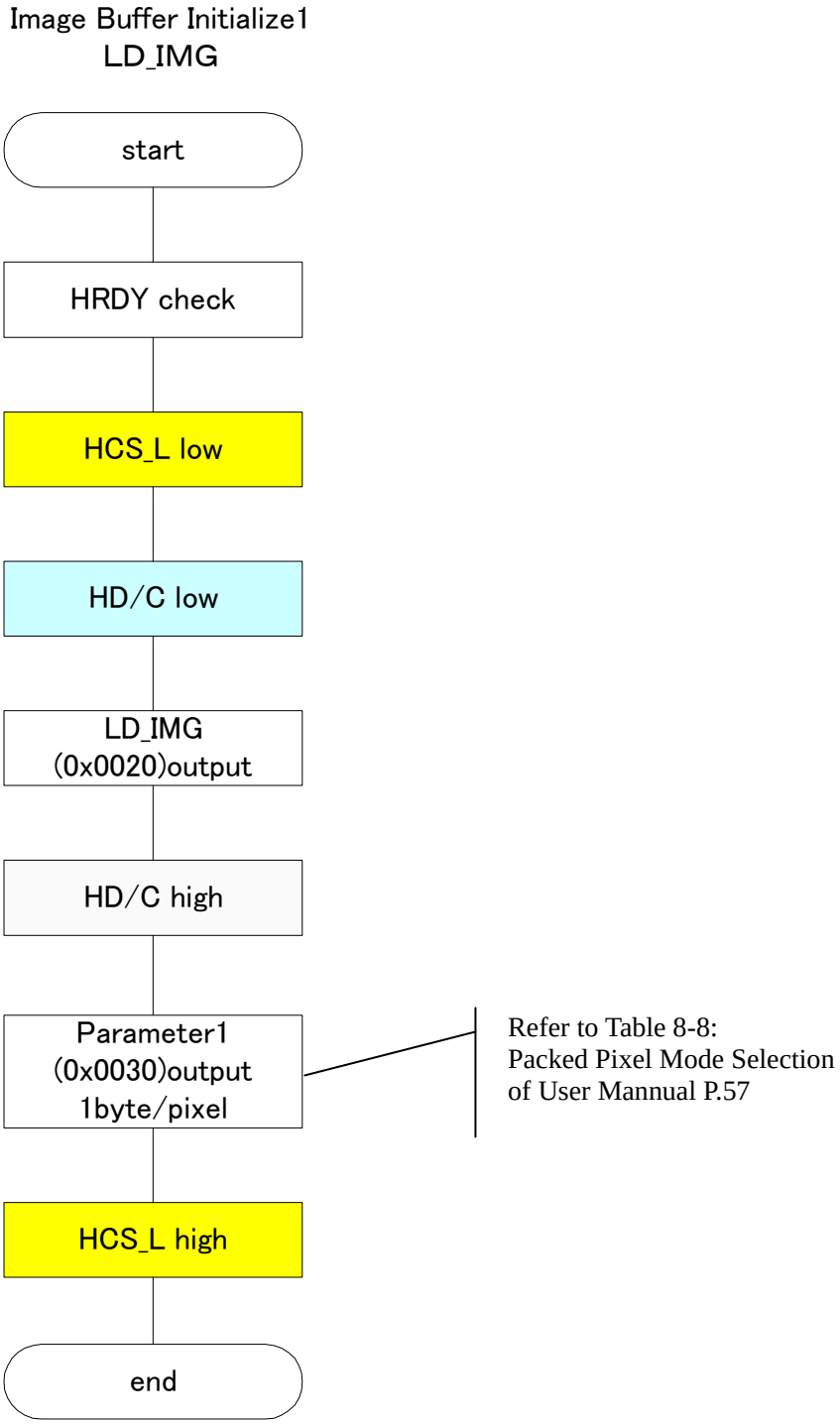


Image Buffer Initialize 2
Image data (0xff)
transmission

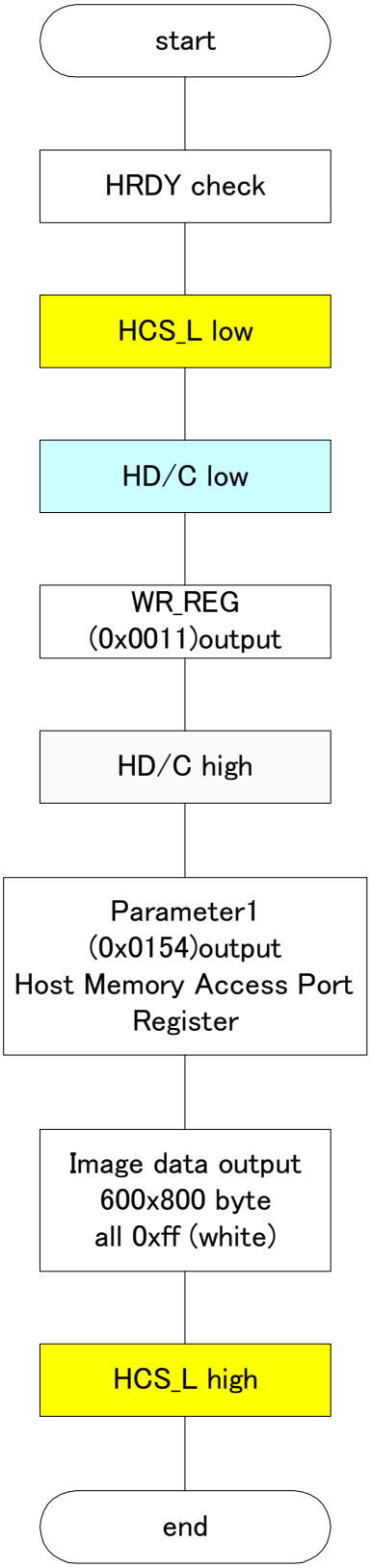
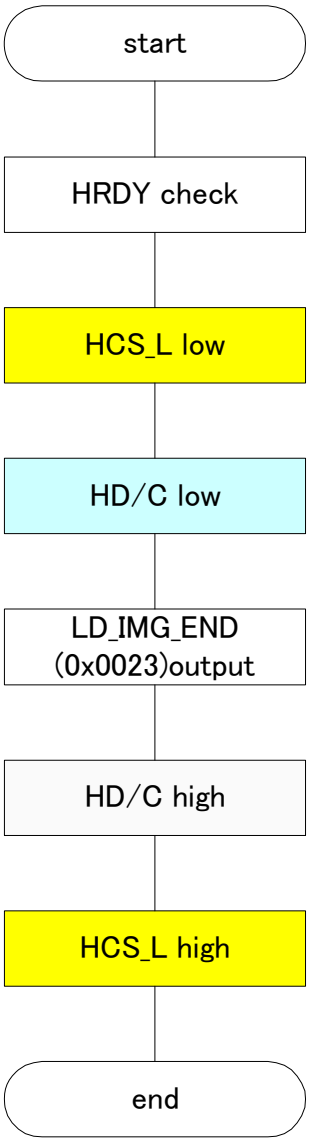


Image Buffer Initialize 3
transmission terminate



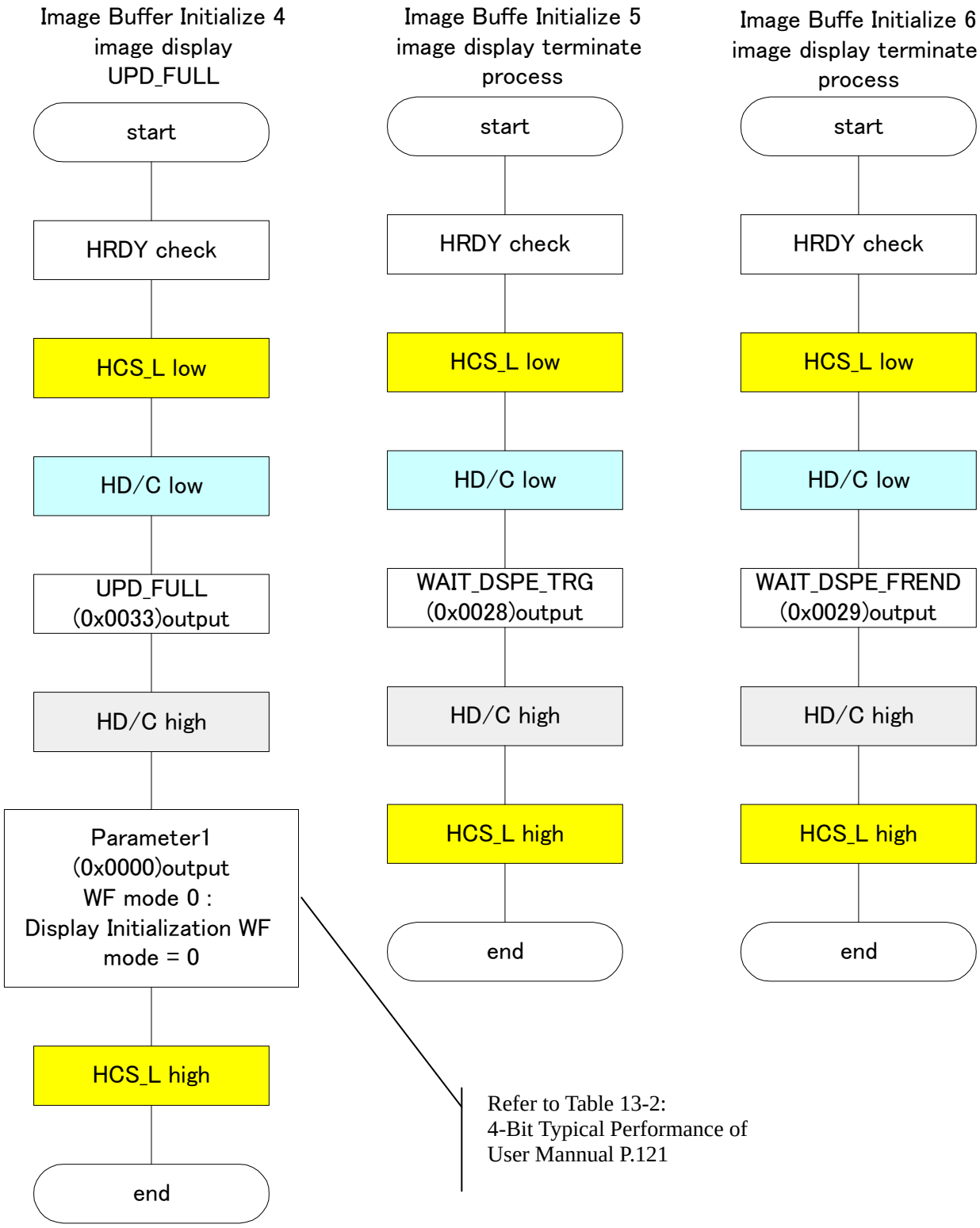
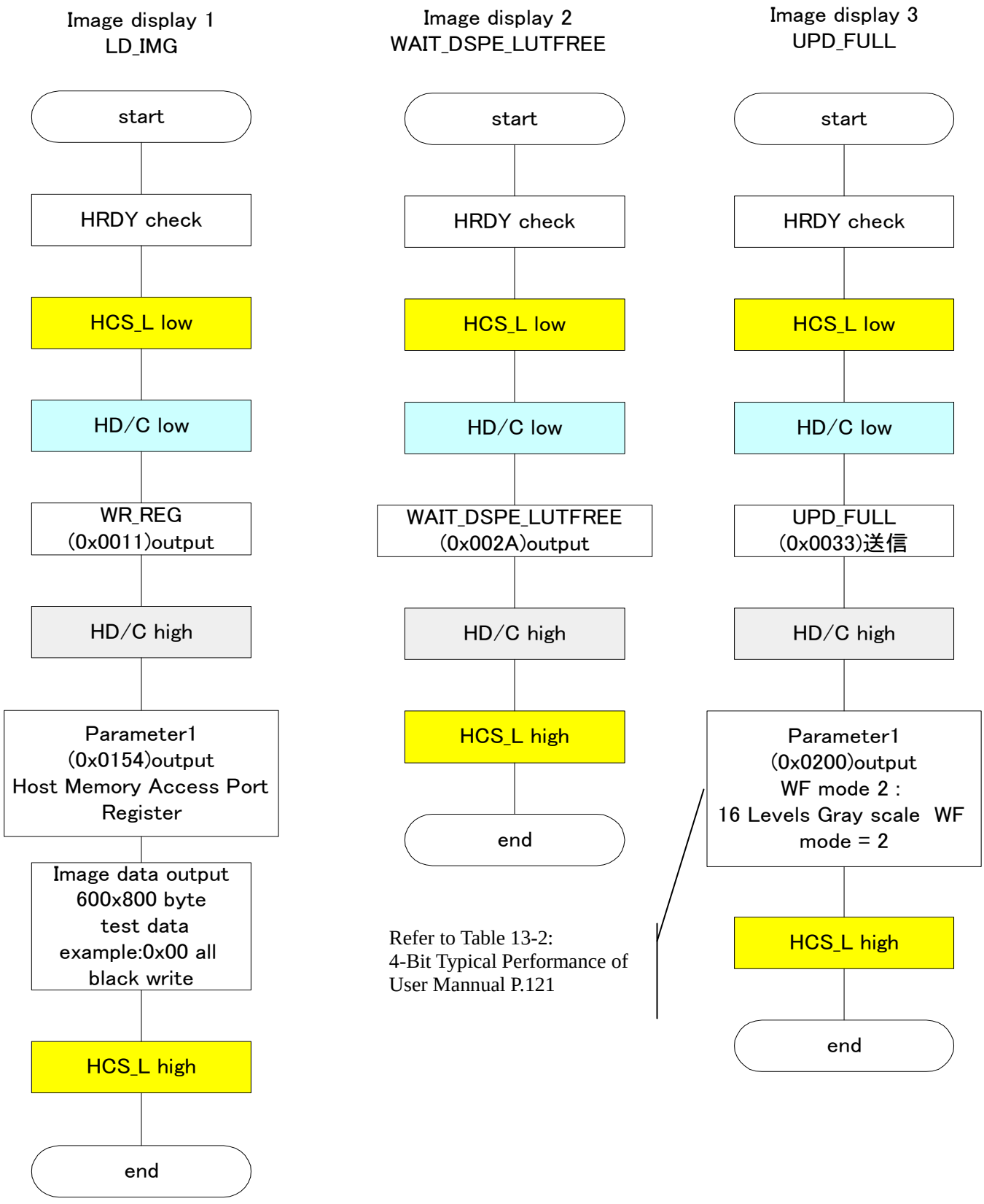


Image Buffer Initialize 4
image display
UPD_FULL
start
HRDY check
HCS_L low
HD/C low
UPD_FULL
(0x0033)output
HD/C high
Parameter1
(0x0000)output
WF mode 0 :
Display Initialization WF
mode = 0
HCS_L high
end
Image Buffe Initialize 5
image display terminate
process
start
HRDY check
HCS_L low
HD/C low
WAIT_DSPE_TRG
(0x0028)output
HD/C high
HCS_L high
end
Image Buffe Initialize 6
image display terminate
process
start
HRDY check
HCS_L low
HD/C low
WAIT_DSPE_FREND
(0x0029)output
HD/C high
HCS_L high
end
Refer to Table 13-2:
4-Bit Typical Performance of
User Mannual P.121

4.5 Image display

Data is written in Image Buffer of S4E5B001B00A00, and it explains the flow displayed on the EPD screen. The value of high 4bit is stored in Image Buffer by S4E5B001B00A00 when the data of 8bit for each 1pixel is written at 16 levels display and it displays it in the EPD panel.



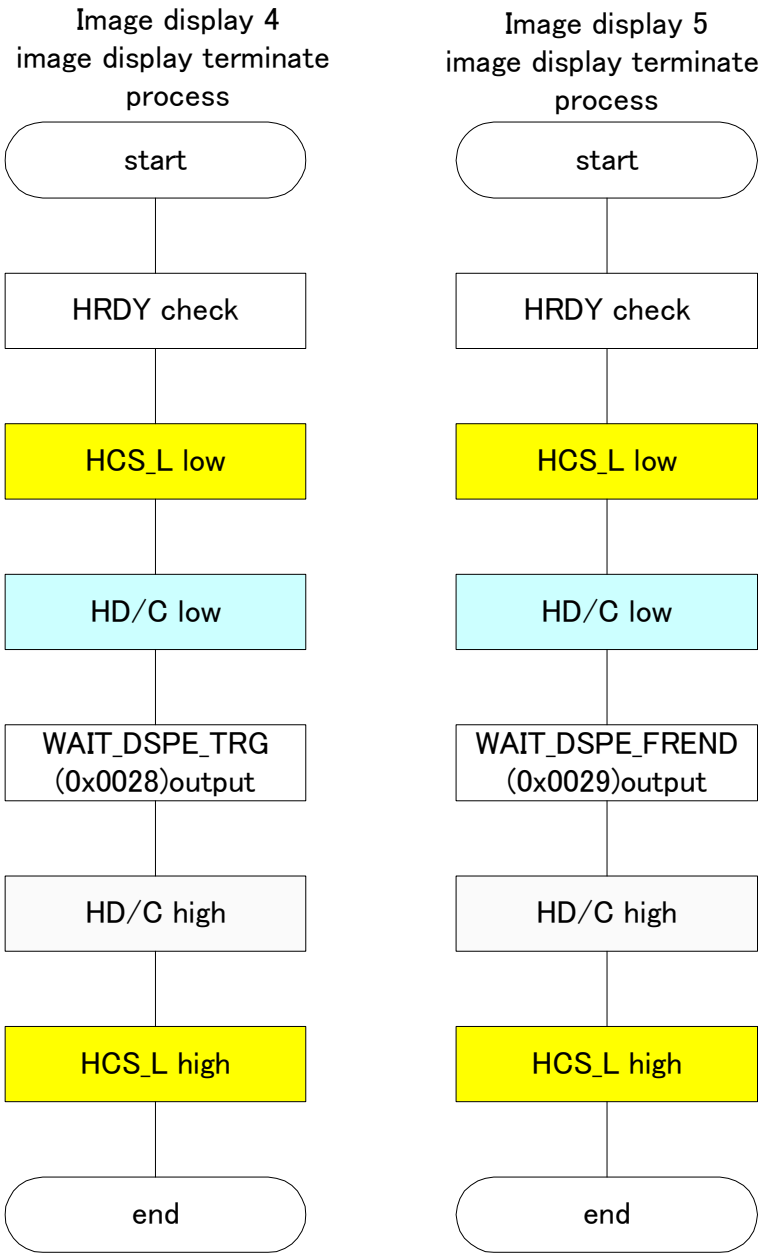


Image display 4
image display terminate process
start
HRDY check
HCS_L low
HD/C low
WAIT_DSPE_TRG (0x0028)output
HD/C high
HCS_L high
end
Image display 5
image display terminate process
start
HRDY check
HCS_L low
HD/C low
WAIT_DSPE_FREND (0x0029)output
HD/C high
HCS_L high
end

4.6 Picture file display

The image of the PG M format is prepared in the same pixel count as the EPD panel encoded by the binary. Data other than the header of the picture file are written in Image Buffer of S4E5B001B00A00 by host CPU. Writing data by the picture file and the display flow become the same flow as 4.5.

Revision History

Attachment-1

Rev. No.	Date	Page	Category	Contents
Rev 1.0	2012/01/18	All	new	

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