2 Port, USB 2.0 High Speed (480 Mbps) Switch, DPDT Analog Switch

DESCRIPTION

The DG2720 is 2 Port high speed analog switch optimized for USB 2.0 signal switching. The DG2720 switch is configured in DPDT. It handles bidirectional signal flow, achieving a 620 MHz - 3 dB bandwidth with 5 pF load, and a port to port Crosstalk and isolation at - 49 dB.

Processed with high density sub micron CMOS, the DG2720 provide low parasitic capacitance. Signals are routed with minimized phase distortion and attain a bit to bit skew is as low as 40 pS.

The DG2720 is designed for a wide range of operating voltages, from 2.7 V to 4.3 V that can be driven directly from one cell Li-ion battery. On-chip circuitry protects against conditions when either the D+/D- lines are shorted to the V_{BUS} at the USB port. Additionally, logic control pins (S and $\overline{OE}$) can tolerate the presence of voltages that are above the supply power rail (V+). The control logic threshold is guaranteed to be (V_{IH} = 1.3 V/min).

Latch up current is greater than 300 mA, as per JESD78, and its ESD tolerance exceeds 8 kV.

Packaged in ultra small miniQFN-10 (1.4 mm x 1.8 mm x 0.55 mm), it is ideal for portable high speed mix signal switching application.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device termination. The miniQFN-10 package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free "-E4" suffix to the ordering part number. The nickel-palladium-gold device terminations meet all JEDEC standards for reflow and MSL rating.

As a further sign of Vishay Siliconix's commitment, the DG2720 is fully RoHS complaint.

FEATURES

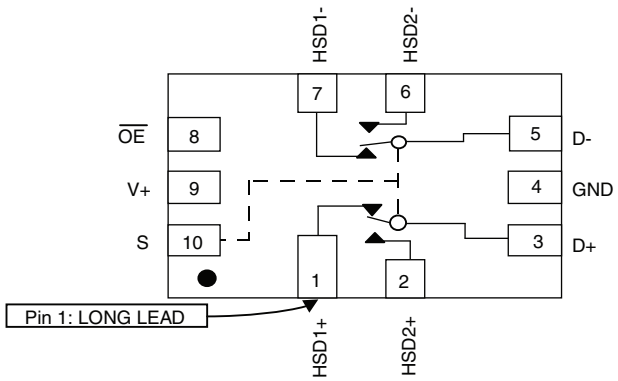
- Wide operation voltage range
- Low on-resistance, 5.7 Ω (typical at 3 V)
- Low capacitance, 5.6 pF (typical)
- 3 dB high bandwidth with 5 pF load: 620 MHz (typical)
- Low bit to bit skew: 40 pS (typical)
- Low power consumption
- Low logic threshold: V
- Power down protection: D+/D- pins can tolerate up to 5 V when V+ = 0 V
- Logic (S and $\overline{OE}$) above V+ tolerance
- Latch-up current greater than 300 mA per JESD78
- 8 kV ESD protection (HBM)
- Lead (Pb)-free low profile miniQFN-10 (1.4 mm x 1.8 mm x 0.55 mm)
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Cellular phones
- Portable media players
- PDA
- Digital camera
- GPS
- Notebook computer
- TV, monitor, and set top box

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

miniQFN-10L

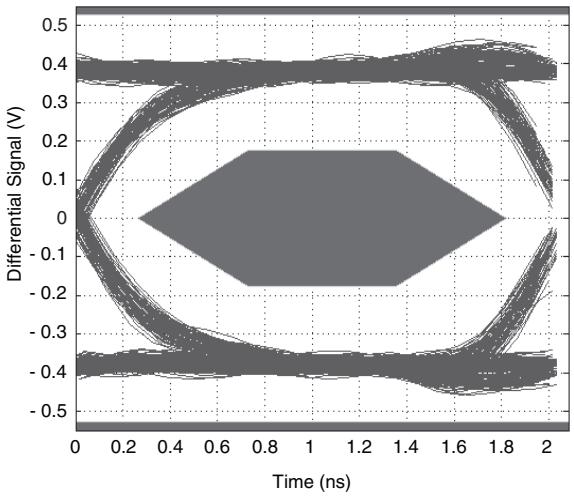


Top View

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
- 40 °C to 85 °C	miniQFN-10	DG2720DN-T1-E4

TRUTH TABLE		
$\overline{OE}$ (Pin 8)	**S (Pin 10)**	**Function**
0	0	D+ = HSD1+ and D- = HSD1-
0	1	D+ = HSD2+ and D- = HSD2-
1	X	Disconnect

PIN DESCRIPTIONS	
Pin Name	**Description**
$\overline{OE}$	Bus Switch Enable
S	Select Input
HSD1±, HSD2±, D±	Data Port



High Speed Signal Quality Eye Diagram Test with V+ = 3.3 V

SUMMARY OF THE USB 2.0 SIGNAL QUALITY TEST RESULTS	
Compliance Test	High Speed
Signal Eye Test	Pass
EOP Width	7.95 bits
Measured Signal Rate	480.0009 MHz
Consecutive Jitter Range	- 59.8 ps to 68.2 ps, RMS Jitter 26.8 ps
Paired JK Jitter Range	- 49.7 ps to 51.4 ps, RMS Jitter 25.3 ps
Paired KJ Jitter Range	- 61.3 ps to 58.5 ps, RMS Jitter 26.8 ps

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
Parameter		**Limit**	**Unit**
Reference to GND	V+	- 0.3 to 5	V
	S, $\overline{OE}$, D±, HSD1±, HSD2±[a]	- 0.3 to (V+ + 0.3)	
Current (Any Terminal except S, $\overline{OE}$, D±, HSD1±, HSD2±)		30	mA
Continuous Current (S, $\overline{OE}$, D±, HSD1±, HSD2±)		± 250	
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 500	
Storage Temperature (D Suffix)		- 65 to 150	°C
Power Dissipation (Packages)[b]	miniQFN-10[c]	208	mW
ESD (Human Body Model) I/O to GND		8	kV
Latch-up (Current Injection)		350	mA

Notes:
a. Signals on S, $\overline{OE}$, D±, HSD1±, HSD2± exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 2.6 mW/°C above 70 °C.

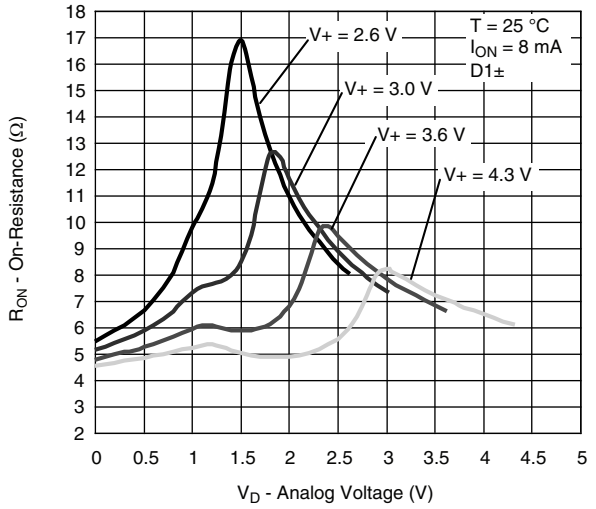
SPECIFICATIONS V+ = 3 V							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified**	**Temp.[a]**	**Limits - 40 to 85 °C**			**Unit**
				Min.	**Typ.**	**Max.**	
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}	$r_{DS(on)}$	Full	0		V+	V
On-Resistance	$R_{DS(on)}$	V+ = 3 V, $I_{D±}$ = 8 mA, $V_{HSD1/2±}$ = 0.4 V	Room		5.7	7	Ω
			Full			9	
On-Resistance Match[d]	ΔR_{ON}	V+ = 3 V, $I_{D±}$ = 8 mA, $V_{HSD1/2±}$ = 0.4 V	Room		0.35		
On-Resistance Resistance Flatness[d]	R_{ON} Flatness	V+ = 3 V, $I_{D±}$ = 8 mA, $V_{HSD1/2±}$ = 0 V, 1 V	Room		2		
Switch Off Leakage Current	$I_{(off)}$	V+ = 4.3 V, $V_{HSD1/2±}$ = 0.3 V, 3 V, $V_{D±}$ = 3 V, 0.3 V	Full	- 100		100	nA
Channel On Leakage Current	$I_{(on)}$	V+ = 4.3 V, $V_{HSD1/2±}$ = 0.3 V, 4 V, $V_{D±}$ = 4 V, 0.3 V	Full	- 200		200	
Digital Control							
Input Voltage High	V_{INH}	V+ = 3 V to 3.6 V	Full	1.3			V
		V+ = 4.3 V	Full	1.7			
Input Voltage Low	V_{INL}	V+ = 3 V to 4.3 V	Full			0.5	
Input Capacitance	C_{IN}		Full		5.6		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	- 1		1	µA

SPECIFICATIONS V+ = 3 V							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified**	**Temp.[a]**	**Limits - 40 to 85 °C**			**Unit**
				Min.[b]	**Typ.[c]**	**Max.[b]**	
Dynamic Characteristics							
Break-Before-Make Time[e, d]	t_{BBM}	V+ = 3 V, $V_{D1/2\pm}$ = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room		5		ns
			Full				
Enable Turn-On Time[e, d]	$t_{ON(EN)}$		Room			30	
			Full				
Enable Turn-Off Time[e, d]	$t_{OFF(EN)}$		Room			25	
			Full				
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 0 V	Room		0.5		pC
Off-Isolation[d]	OIRR	V+ = 3 V to 3.6 V, R_L = 50 Ω, C_L = 5 pF, f = 240 MHz			- 30		dB
Crosstalk[d]	X_{TALK}				- 49		
Bandwidth[d]	BW	V+ = 3 V to 3.6 V, R_L = 50 Ω, C_L = 5 pF, - 3 dB			620		MHz
Channel-Off Capacitance[d]	$C_{D1\pm\ (off)}$	V+ = 3.3 V, f = 1 MHz			4		pF
	$C_{D2\pm\ (off)}$				4		
Channel-On Capacitance[d]	$C_{D\pm\ (off)}$				5.6		
	$C_{D\pm\ (on)}$				11		
Channel-to-Channel Skew[d]	$t_{SK(O)}$	V+ = 3 V to 3.6 V, R_L = 50 Ω, C_L = 5 pF			50		ps
Skew Off Opposite Transitions of the Same Output[d]	$t_{SK(p)}$				20		
Total Jitter[d]	t_J				200		
Power Supply							
Power Supply Range	V+			2.6		4.3	V
Power Supply Current	I+	V_{IN} = 0 V, or V+	Full			2	µA

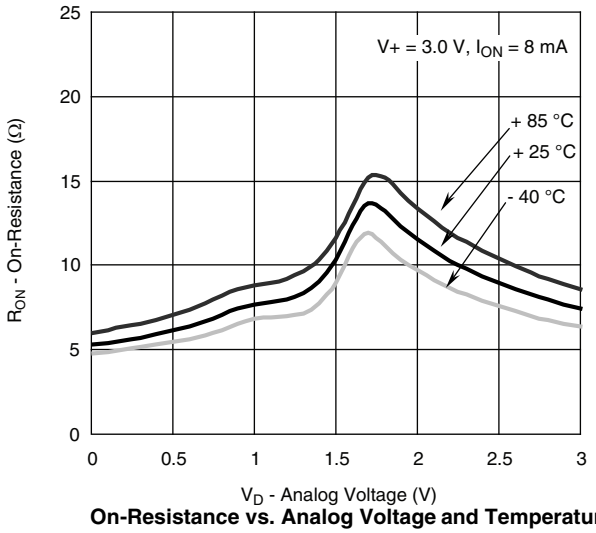
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, not subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Crosstalk measured between channels.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

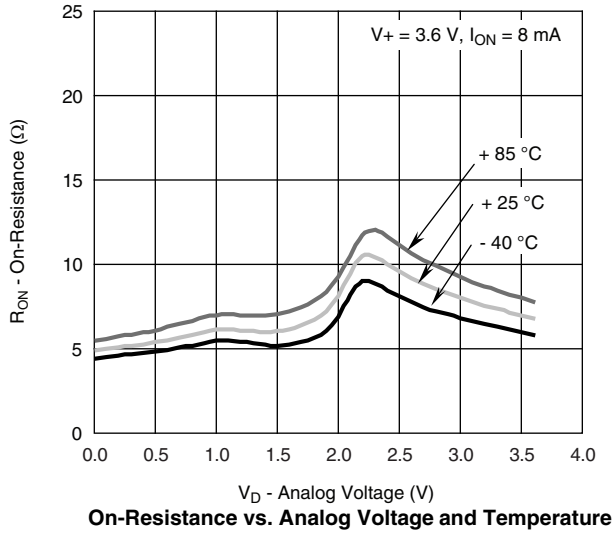
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



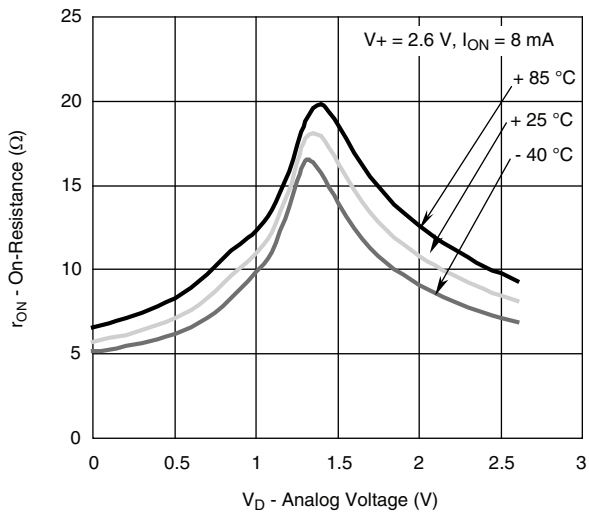
On-Resistance vs. V_D and Single Supply Voltage



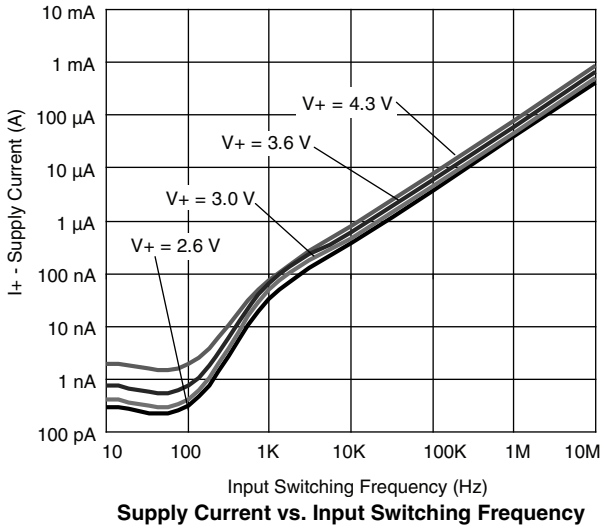
On-Resistance vs. Analog Voltage and Temperature



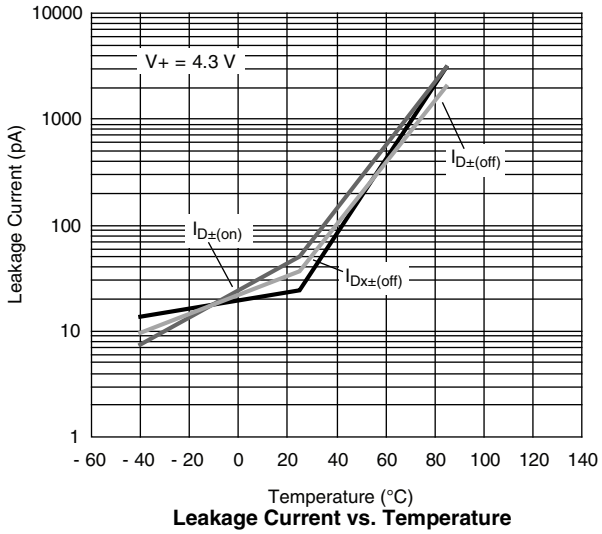
On-Resistance vs. Analog Voltage and Temperature



On-Resistance vs. Analog Voltage and Temperature

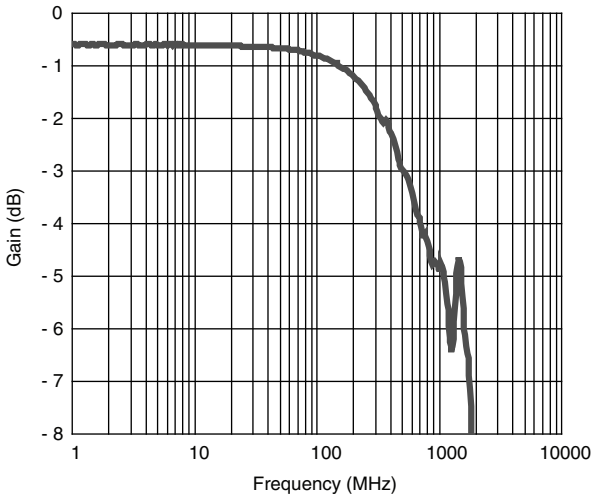


Supply Current vs. Input Switching Frequency

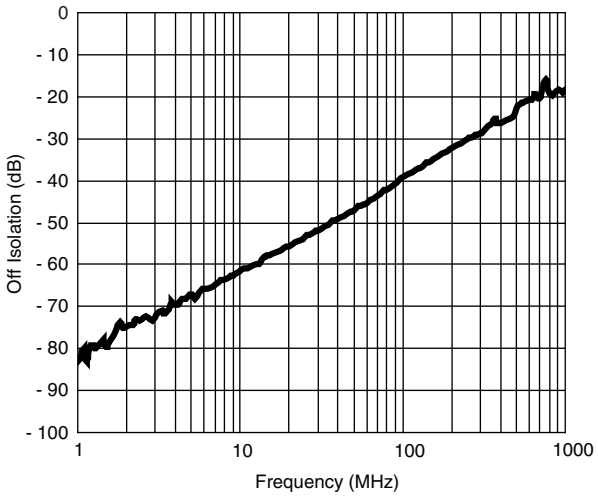


Leakage Current vs. Temperature

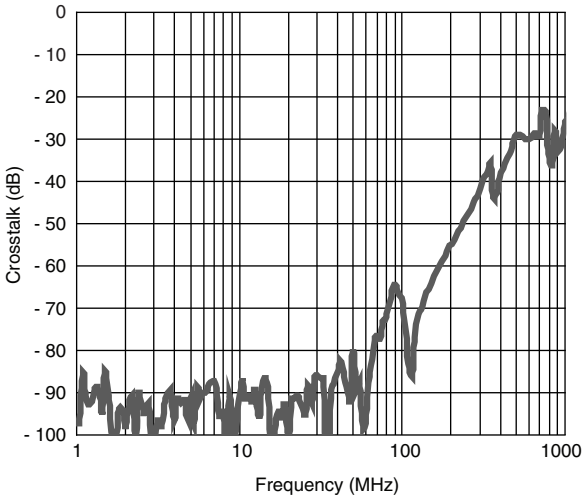
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



Gain vs. Frequency, C_L = 5 pF, V+ = 3.3 V

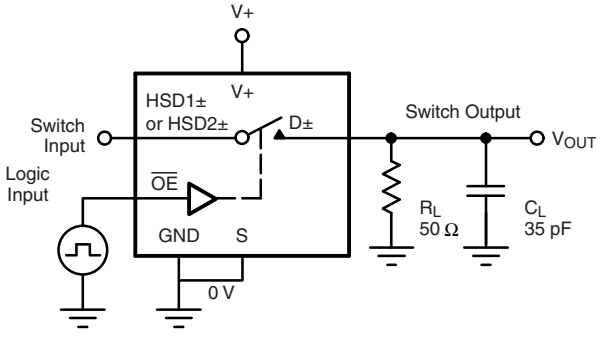


OFF Isolation, V+ = 3.3 V



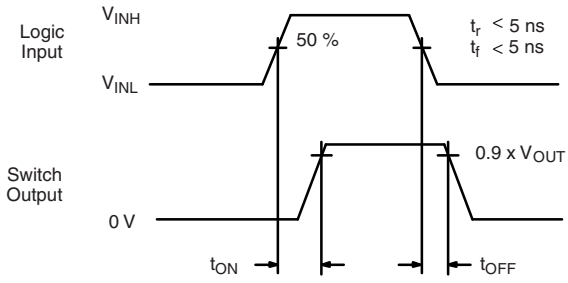
Crosstalk, V+ = 3.3 V

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

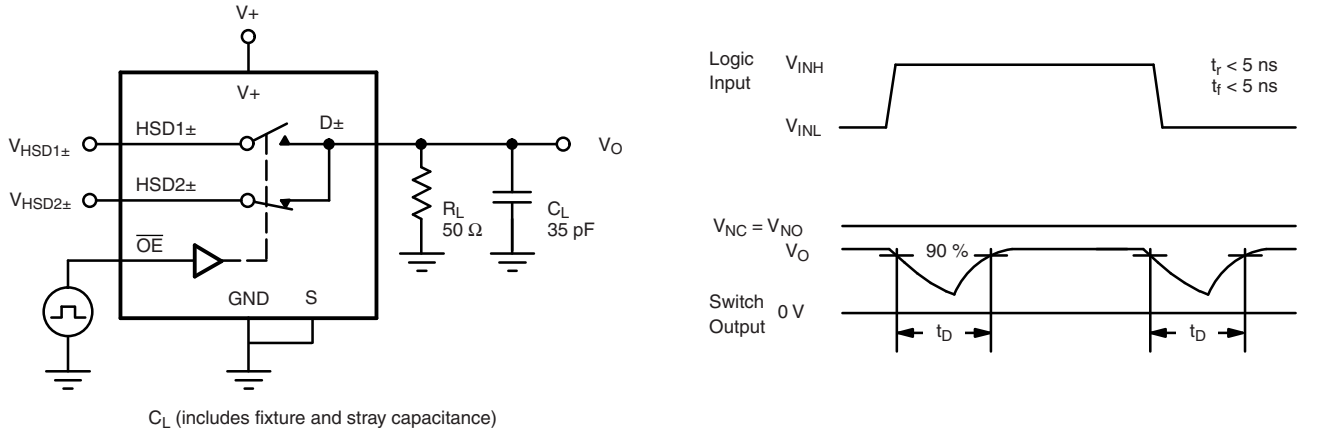
$$V_{OUT} = D\pm \left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

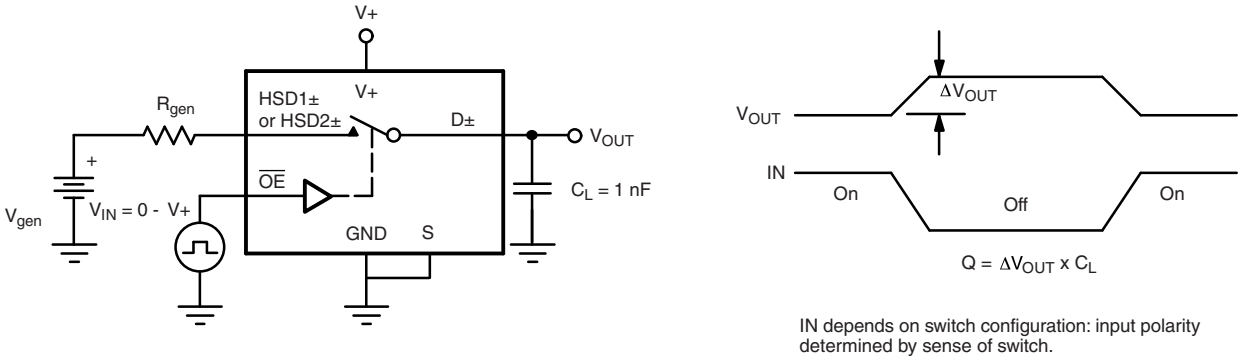
Figure 1. Switching Time

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

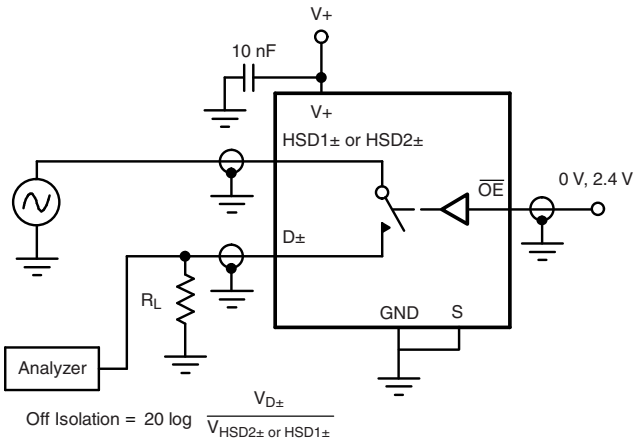


Figure 4. Off-Isolation

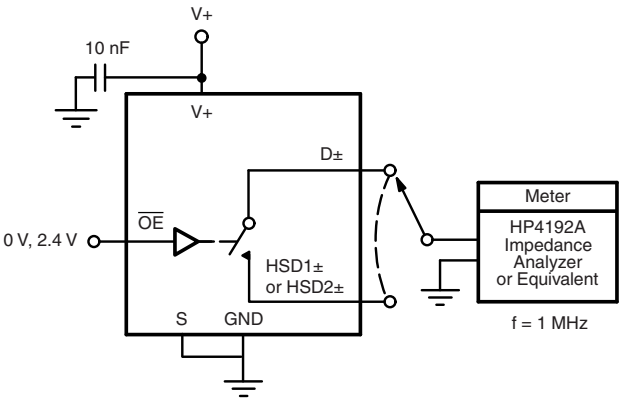
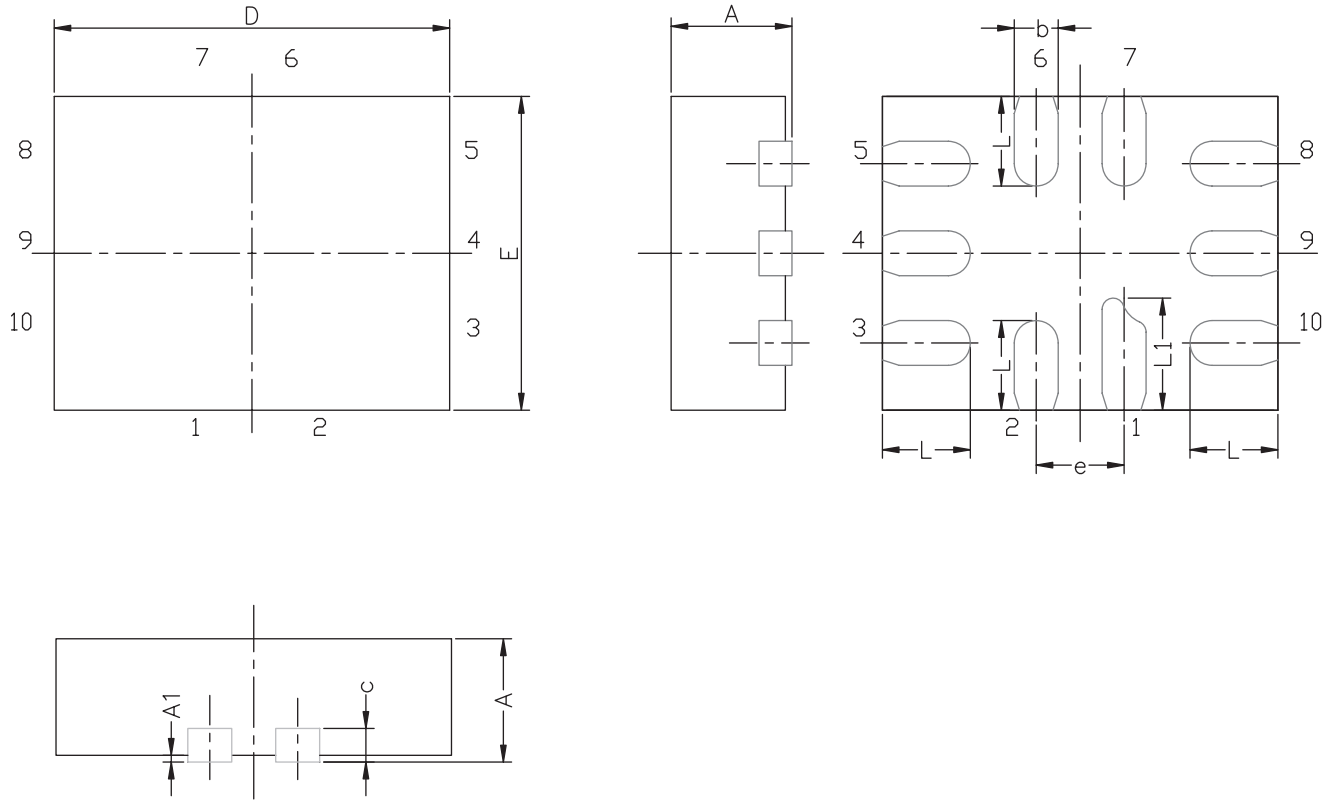


Figure 5. Channel Off/On Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?74593.

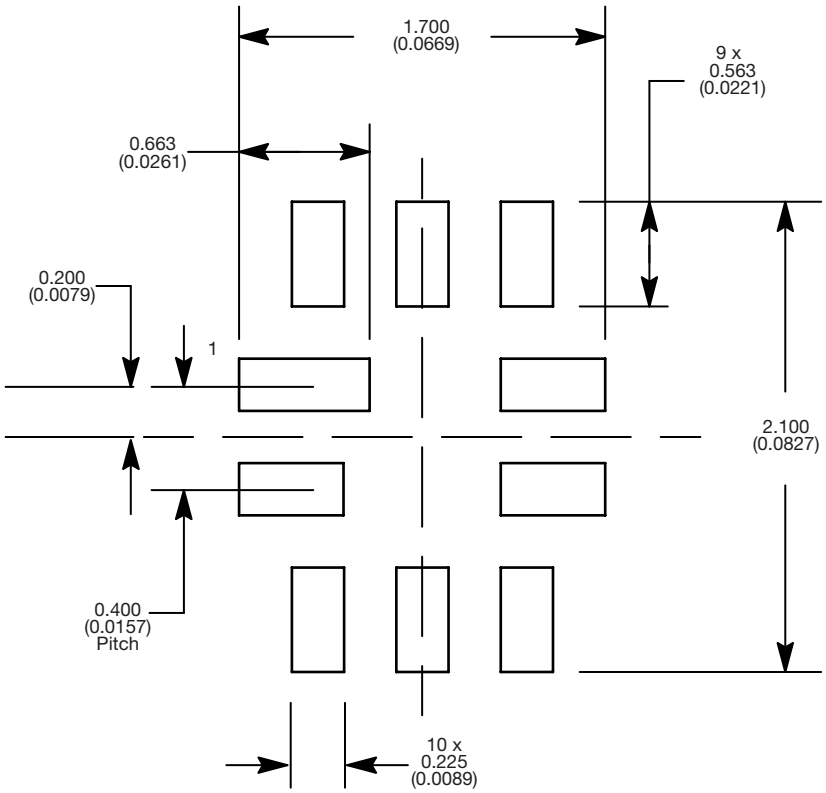
MINI QFN-10L CASE OUTLINE



DIM	MILLIMETERS			INCHES		
	MIN.	NAM.	MAX.	MIN.	NAM.	MAX.
A	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1	0.00	-	0.05	0.000	-	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.15 REF			0.006 REF		
D	1.75	1.80	1.85	0.069	0.071	0.073
E	1.35	1.40	1.45	0.053	0.055	0.057
e	0.40 BSC			0.016 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.0177	0.0197	0.0217

ECN T-07039-Rev. A, 12-Feb-07
DWG: 5957

RECOMMENDED MINIMUM PADS FOR MINI QFN 10L



Mounting Footprint
Dimensions in mm (inch)

Disclaimer

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