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FQA13N50C_F109

N-Channel QFET® MOSFET

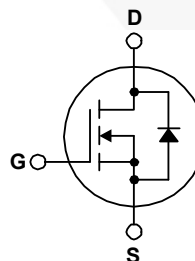
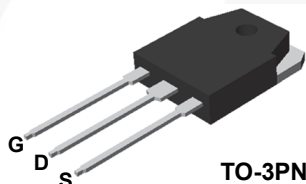
500 V, 13.5 A, 480 mΩ

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.

Features

- 13.5 A, 500 V, $R_{DS(on)} = 480 \text{ m}\Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = 6.75 \text{ A}$
- Low Gate Charge (Typ. 43 nC)
- Low Crss (Typ. 20 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQA13N50C_F109	Unit
V_{DSS}	Drain-Source Voltage	500	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	13.5	A
	- Continuous ($T_C = 100^\circ\text{C}$)	8.5	A
I_{DM}	Drain Current - Pulsed (Note 1)	54	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	860	mJ
I_{AR}	Avalanche Current (Note 1)	13.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	21.8	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	218	W
	- Derate above 25°C	1.56	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds.	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FQA13N50C_F109	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.58	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQA13N50C_F109	FQA13N50C	TO-3PN	Tube	N/A	N/A	30 units

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	--	0.5	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 400\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 6.75\text{ A}$	--	0.39	0.48	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 6.75\text{ A}$	--	15	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1580	2055	pF
C_{oss}	Output Capacitance		--	180	235	pF
C_{rss}	Reverse Transfer Capacitance		--	20	25	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 13.5\text{ A},$ $R_G = 25\ \Omega$	--	25	60	ns	
t_r	Turn-On Rise Time		--	100	210	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4)	--	130	270	ns
t_f	Turn-Off Fall Time		(Note 4)	--	100	210	ns
Q_g	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 13.5\text{ A},$ $V_{GS} = 10\text{ V}$	--	43	56	nC	
Q_{gs}	Gate-Source Charge		(Note 4)	--	7.5	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4)	--	18.5	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	13	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	52	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 13.5\text{ A}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 13.5\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$	--	410	--	ns
Q_{rr}	Reverse Recovery Charge		--	4.5	--	μC

Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. $L = 5.6\text{ mH}, I_{AS} = 13.5\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 13.5\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature

Typical Characteristics

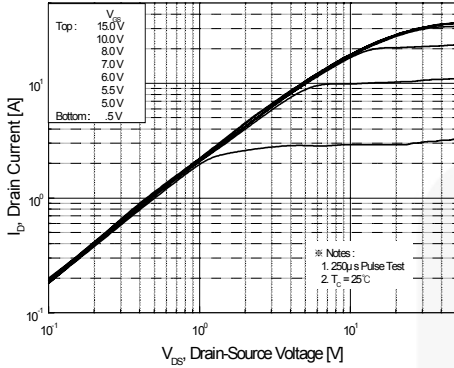


Figure 1. On-Region Characteristics

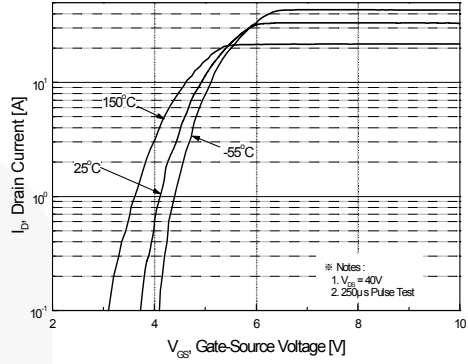


Figure 2. Transfer Characteristics

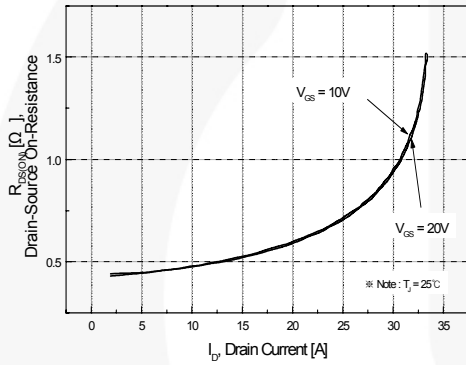


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

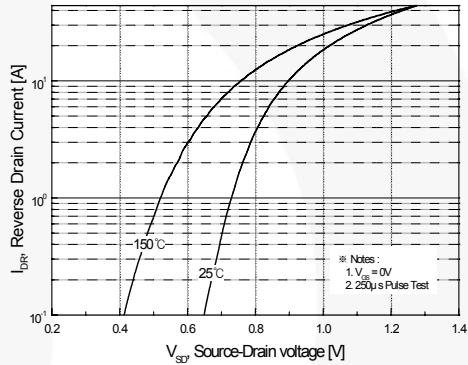


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

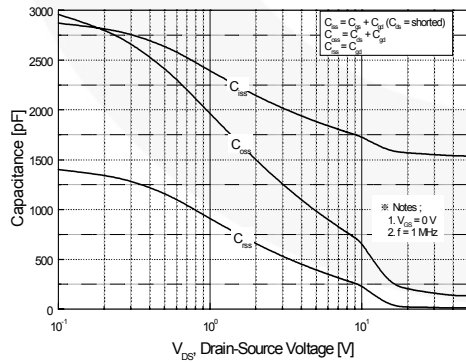


Figure 5. Capacitance Characteristics

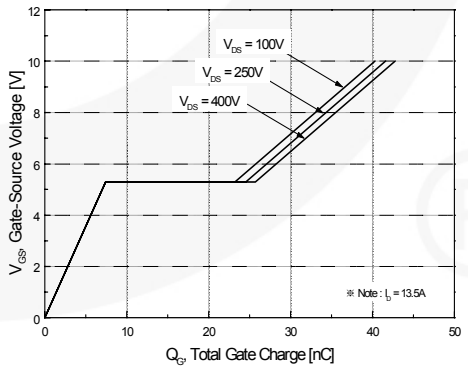


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

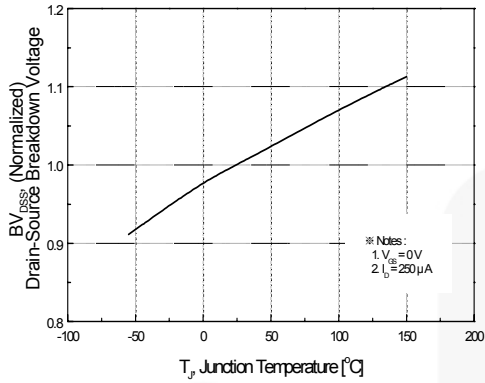


Figure 7. Breakdown Voltage Variation vs Temperature

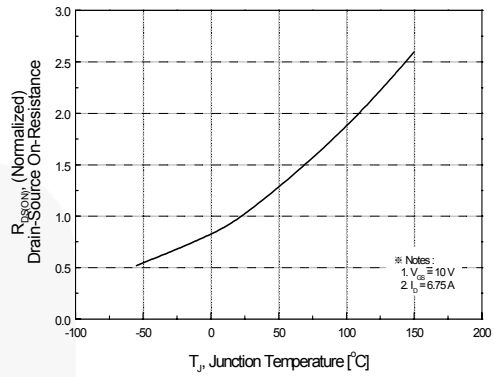


Figure 8. On-Resistance Variation vs Temperature

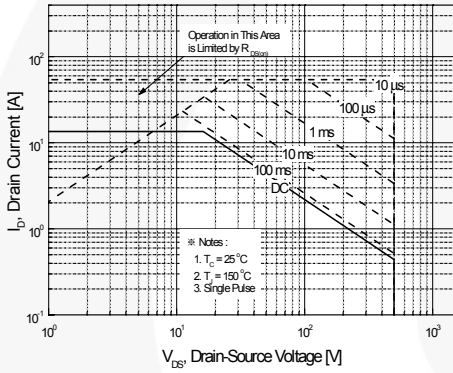


Figure 9. Maximum Safe Operating Area

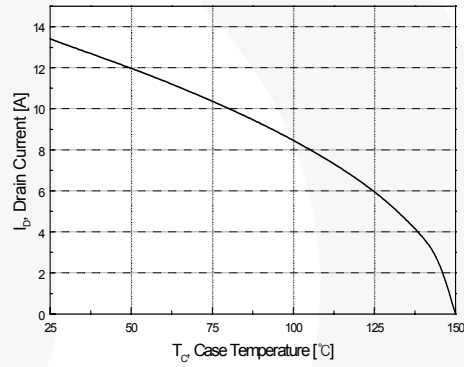


Figure 10. Maximum Drain Current vs Case Temperature

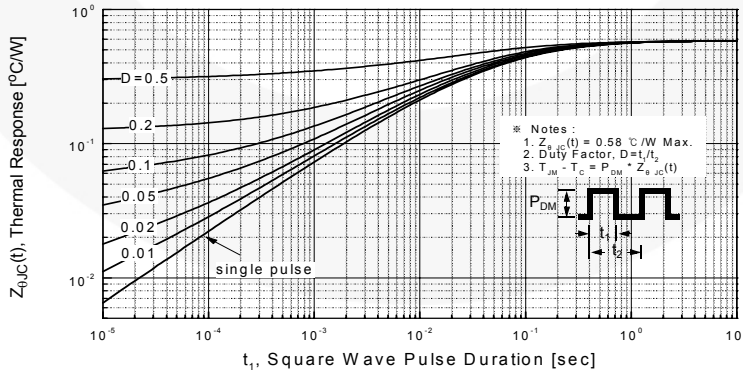


Figure 11. Transient Thermal Response Curve for FQA13N50C

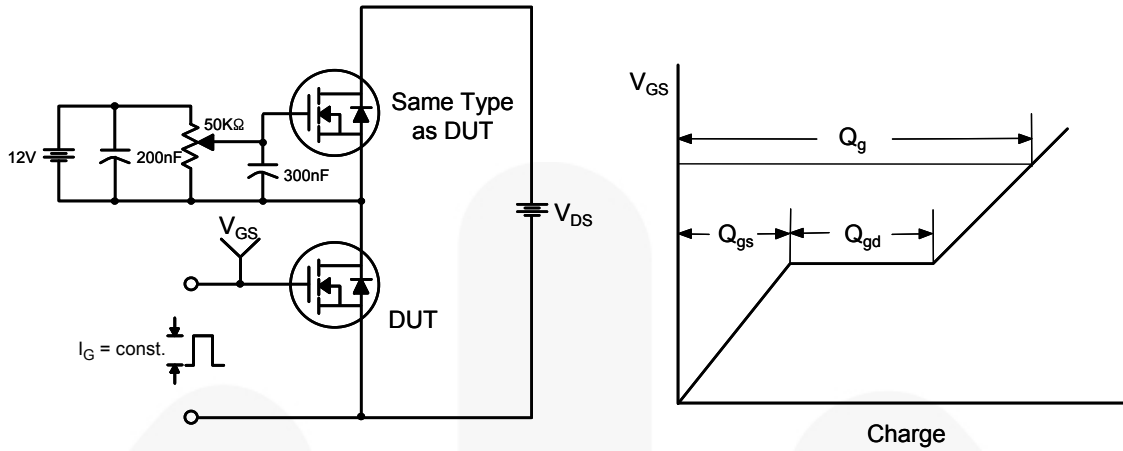


Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms

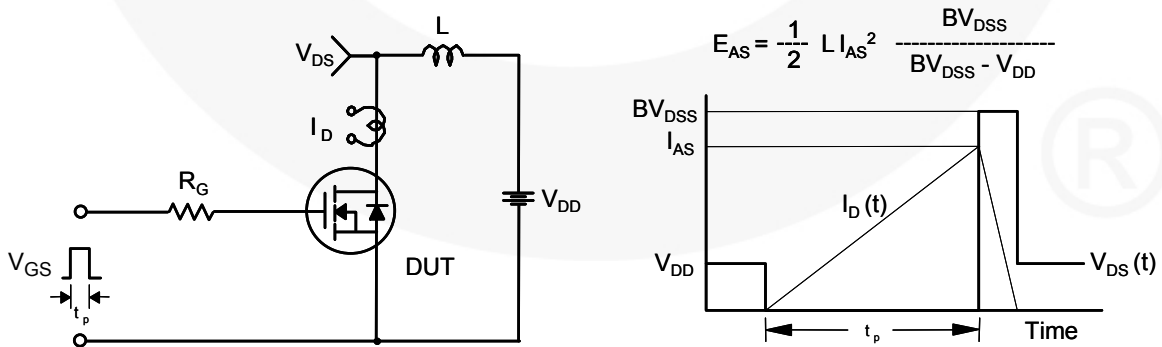
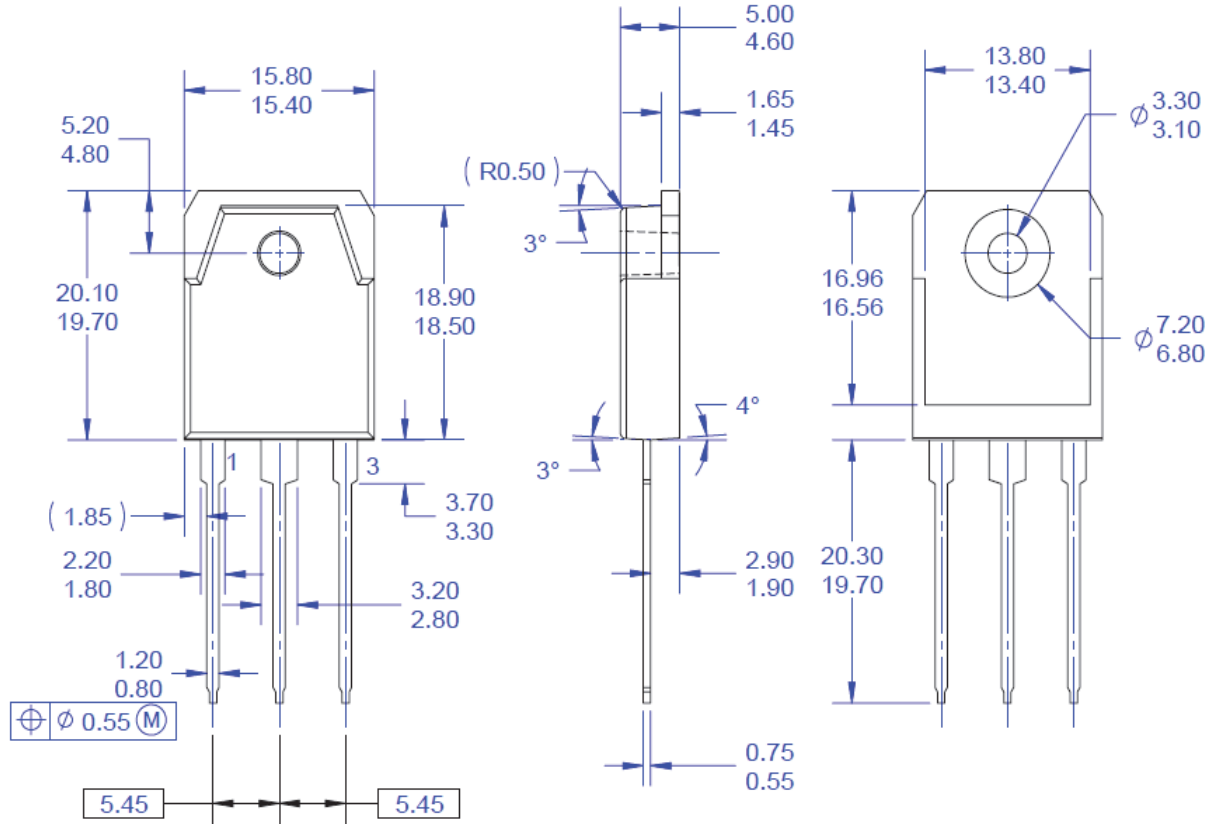


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

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- B) ALL DIMENSIONS ARE IN MILLIMETERS.
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Figure 16. TO3, 3-Lead, Plastic, EIAJ SC-65

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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