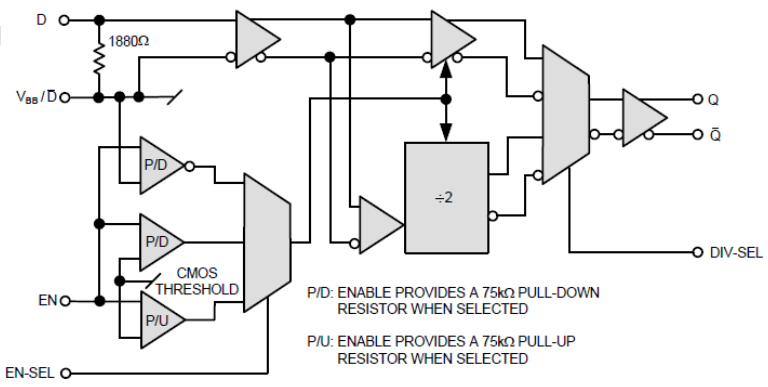
LVPECL Divide by 1, Divide by 2 Clock Generator w/ Selectable Enable

MLP8

FEATURES

- Selectable Divide Ratio
- Selectable Enable Priority and Threshold (CMOS or PECL)
- 3.0V to 5.5V Power Supply
- -145dBc/Hz (÷1) Typical Noise Floor
- -151dBc/Hz (÷2) Typical Noise Floor
- High BW [1.5GHz (÷1), 3.0GHz (÷2)]
- ROHS compliant Pb Free Packages

BLOCK DIAGRAM



DESCRIPTION

The CTSLV392 is a ÷1 or ÷2 clock generation part specifically designed to accommodate Colpitts or Pierce based oscillators. Features are incorporated to reduce board components. A voltage reference and input biasing allows for easy oscillator interface.

The CTSLV392 provides a ÷ 2 mode of operation for more frequency options and is selectable with a single connection. A selectable enable is also provided which doubles as a reset when the CTSLV392 is in ÷2 mode. With a single connection, the enable can be selected to operate as active high or active low.

ENGINEERING NOTES

The CTSLV392 is a specialized ÷1 or ÷2 clock generation part including an enable/reset function. The divide ratio is selected with the DIV-SEL pin/pad. When DIV-SEL is open (NC), the CTSLV392 functions as a standard receiver. If DIV-SEL is connected to V_{EE}, it functions as a ÷2 divider.

A selectable enable is provided which also functions as a reset when the ÷2 mode is selected. Enable (EN) functionality is selected with the EN-SEL pin/pad which has three valid states: open (NC), V_{EE}, or connected to V_{EE} via a 20kΩ resistor. Leaving EN-SEL open or connecting it to V_{EE} will select the EN pin/pad to function as an active high CMOS/TTL enable. When EN-SEL is open, an internal 75kΩ pull-up resistor is selected which enables the outputs whenever EN is left open. When EN-SEL is connected to V_{EE}, an internal 75kΩ pull-down resistor is selected which disables the outputs whenever EN is left open.

Connecting the EN-SEL to V_{EE} with a 20kΩ resistor will select the EN pin/pad to function as an active low PECL/ECL enable with an internal 75kΩ pull-down resistor. In this mode, outputs are enabled when EN is left open (NC). This default logic condition can be overridden by connecting the EN to V_{CC} with an external resistor of ≤20kΩ. Refer to the enable truth table on the next page for detailed operation.

The CTSLV392 provides a V_{BB} with an 1880Ω internal bias resistor from D to V_{BB}. This feature allows AC coupling with minimal external components. The V_{BB} pin supports 1.5mA sink/source current and should be bypassed to ground or V_{CC} with a 0.01 µF capacitor.

Divide Truth Table

DIV-SEL	÷Ratio
NC	÷1
V_{EE}[1]	÷2

[1] DIV-SEL connection must be ≤1Ω.

Enable Truth Table

EN-SEL	EN	Q	$\bar{Q}$
NC	CMOS Low or V_{EE}	Low	Low
	CMOS High, V_{CC} or NC	Data	Data
V_{EE}	CMOS Low, V_{EE} or NC	Low	Low
	CMOS High or V_{CC}	Data	Data
20kΩ to V_{EE}	PECL Low, V_{EE} or NC	Low	Low
	PECL High or V_{CC}	Data	Data

Figure 1 illustrates the timing sequences for the CTSLV392 in the ÷1 mode which is determined by leaving the DIV-SEL open (NC). It also illustrates the enable in the active High mode being controlled by a CMOS signal. This mode is determined by leaving the EN-SEL open (NC).

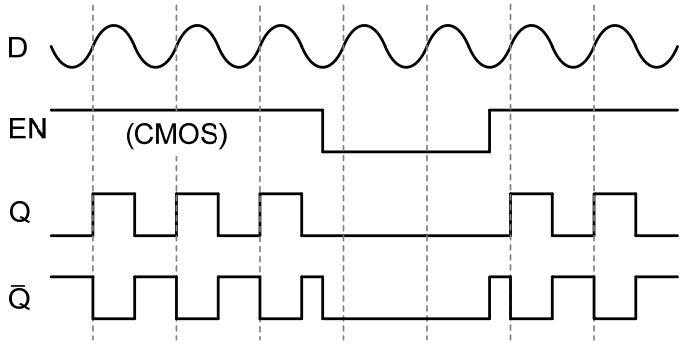


Figure 1

Figure 2 illustrates the timing sequences for the CTSLV392 in the ÷2 mode which is determined by connecting the DIV-SEL to V_{EE}. It also illustrates the enable in the active Low mode being controlled by a PECL signal. This mode is determined by connecting the EN-SEL to V_{EE} via 20kΩ resistor.

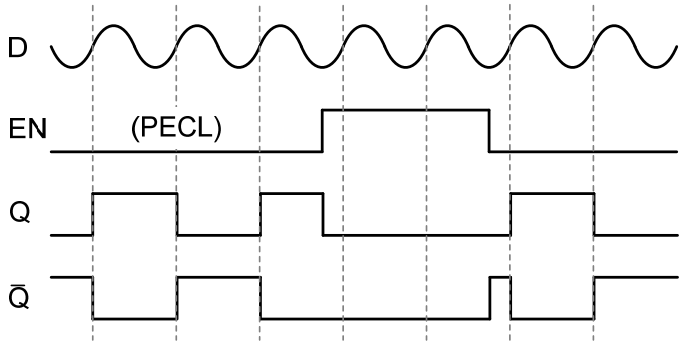


Figure 2

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V_{CC}	PECL Power Supply	V_{EE} = 0V	0 to + 6.0	V
V_{I_PECL}	PECL Input Voltage	V_{EE} = 0V	0 to + 6.0	V
V_{EE}	ECL Power Supply	V_{CC} = 0V	-6.0 to 0	V
V_{I_ECL}	ECL Input Supply	V_{CC} = 0V	-6.0 to 0	V
I_{HGOUT}	Output Current	Continuous	50	mA
		Surge	100	
T_A	Operating Temperature Range	-	-40 to +85	°C
T_{STG}	Storage Temperature Range	-	-65 to +150	°C
ESD_{HBM}	Human Body Model Electro Static Discharge	-	2500	V
ESD_{MM}	Machine Model Electro Static Discharge	-	200	V
ESD_{CDM}	Charged Device Model Electro Static Discharge	-	2000	V

100K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1]	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
V_{OL}	Output LOW Voltage[1]	-1900	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V_{IH}	Input HIGH Voltage D, EN (ECL)[2]	-1165	-390	-1165	-390	-1165	-390	-1165	-390	mV
	Input HIGH Voltage EN (CMOS)[3]	V_{EE} +2000	V_{CC}	V_{EE} +2000	V_{CC}	V_{EE} +2000	V_{CC}	V_{EE} +2000	V_{CC}	mV
V_{IL}	Input LOW Voltage D, EN (ECL)[2]	-2250	-1475	-2250	-1475	-2250	-1475	-2250	-1475	mV
	Input LOW Voltage EN (CMOS)[3]	V_{EE}	V_{EE} +800	V_{EE}	V_{EE} +800	V_{EE}	V_{EE} +800	V_{EE}	V_{EE} +800	mV
V_{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN (ECL)[2]	0.5		0.5		0.5		0.5		µA
	Input LOW Current EN (CMOS)[3]	-150		-150		-150		-150		
I_{EE}	Power Supply Current[4]		31		31		31		34	mA

1 Specified with each output terminated through 50Ω resistors to V_{CC} -2V.
2 EN-SEL connected to V_{EE} through a 20kΩ resistor.
3 EN-SEL connected to V_{EE} or left open (NC).
4 DIV-SEL left open (NC)

100K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	2215	2420	2275	2420	2275	2420	2275	2420	mV
V_{OL}	Output LOW Voltage[1,2]	1400	1745	1400	1680	1400	1680	1400	1680	mV
V_{IH}	Input HIGH Voltage D,EN (ECL)[3]	2135	2910	2135	2910	2135	2910	2135	2910	mV
	Input HIGH Voltage EN (CMOS)[4]	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	mV
V_{IL}	Input LOW Voltage D,EN (ECL)[3]	1050	1825	1050	1825	1050	1825	1050	1825	mV
	Input LOW Voltage EN (CMOS)[4]	GND	800	GND	800	GND	800	GND	800	mV
V_{BB}	Reference Voltage[1]	1910	2050	1910	2050	1910	2050	1910	2050	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN (ECL)[3]	0.5		0.5		0.5		0.5		µA
	Input LOW Current EN (CMOS)[4]	-150		-150		-150		-150		
I_{EE}	Power Supply Current[5]		31		31		31		34	mA

1 For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.
2 Specified with each output terminated through 50Ω resistors to V_{CC} -2V.
3 EN-SEL connected to V_{EE} through a 20kΩ resistor.
4 EN-SEL connected to V_{EE} or left open (NC)
5 DIV-SEL left open (NC)

100K PECL DC Characteristics (V_{EE} = GND, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	3915	4120	3975	4120	3975	4120	3975	4120	mV
V_{OL}	Output LOW Voltage[1,2]	3100	3445	3100	3380	3100	3380	3100	3380	mV
V_{IH}	Input HIGH Voltage D,EN (ECL)[3]	3835	4610	3835	4610	3835	4610	3835	4610	mV
	Input HIGH Voltage EN (CMOS)[4]	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	mV
V_{IL}	Input LOW Voltage D,EN (ECL)[3]	2750	3525	2750	3525	2750	3525	2750	3525	mV
	Input LOW Voltage EN (CMOS)[4]	GND	800	GND	800	GND	800	GND	800	mV
V_{BB}	Reference Voltage[1]	3610	3750	3610	3750	3610	3750	3610	3750	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN (ECL)[3]	0.5		0.5		0.5		0.5		µA
	Input LOW Current EN (CMOS)[4]	-150		-150		-150		-150		
I_{EE}	Power Supply Current[5]		31		31		31		34	mA

1 For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.
2 Specified with each output terminated through 50Ω resistors to V_{CC} -2V.
3 EN-SEL connected to V_{EE} through a 20kΩ resistor.
4 EN-SEL connected to V_{EE} or left open (NC).
5 DIV-SEL left open (NC).

AC Characteristics (V_{EE} = -3.0V to -5.5V; V_{CC}=GND or V_{EE}=GND; V_{CC} = +3.0V to +5.5V)

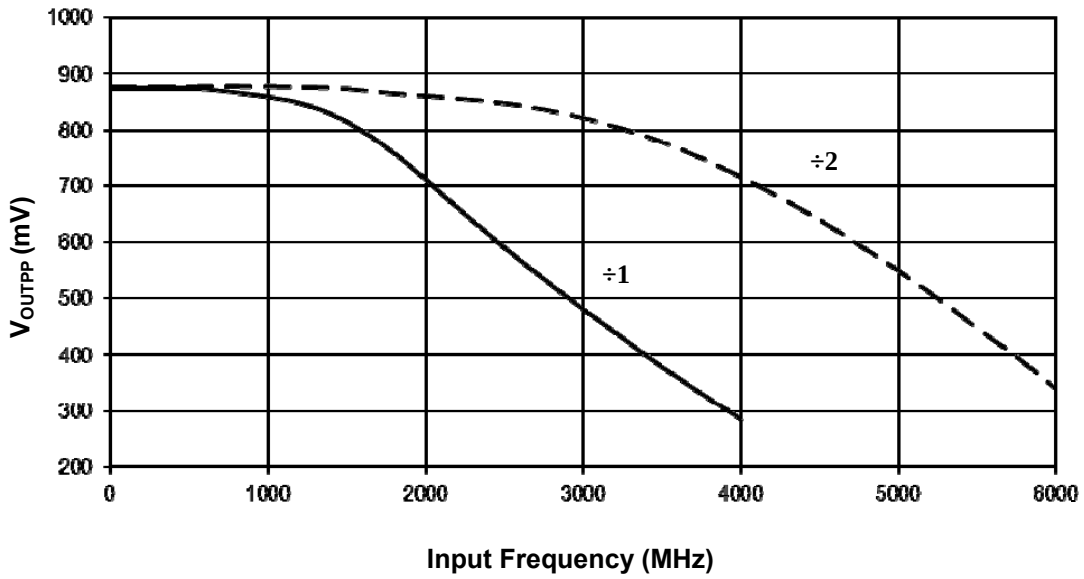
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}/t_{PHL}	D to Q/Qb[1]			450			450			450			450	ps
	D to Q_{HG}/Qb_{HG}[1]			600			600			600			600	ps
t_{SKEW}	Duty Cycle Skew[2]		5	20		5	20		5	20		5	20	ps
V_{PP} (AC)	Input Swing[3] Differential	150		1000	150		1000	150		1000	150		1000	mV
	Input Swing[3] Single Ended	300		2000	300		2000	300		2000	300		2000	
t_R/t_F	Output Rise/Fall[1] (20% - 80%)	80		200	80		200	80		200	80		200	ps

1 Specified with each output terminated through 50Ω resistors to V_{CC} -2V.

2 Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

3 V_{PP} is the peak-to-peak differential input swing for which AC parameters are guaranteed.

4 Range valid for AC coupled signals only.

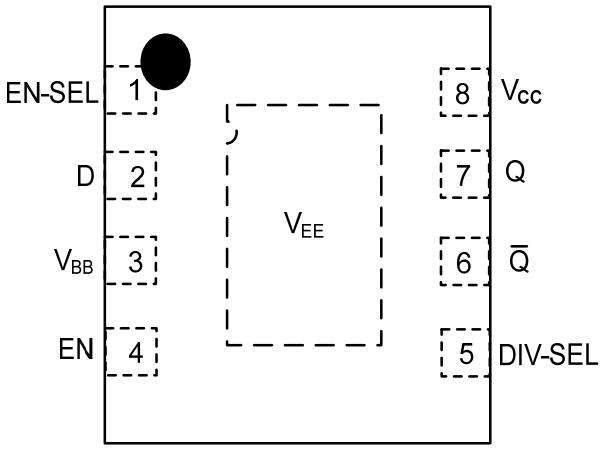


Typical Large Signal Output Swing
Measured with 750mV D input, Q/$\overline{Q}$ each terminated to V_{CC}-2V via 50Ω resistors.

Pin Description and Configuration

Pin Assignments

Pin	Name	Type	Function
1	EN-SEL	Input	Enable Polarity Select
2	D	Input	Data Input
3	V_{BB}	Input	Reference Voltage
4	EN	Input	Output Enable
5	DIV-SEL	Input	Divide Select
6	$\overline{Q}$	Output	Inverted PECL Output
7	Q	Output	PECL Output
8	V_{CC}	Power	Positive Supply
9	V_{EE}	Power	Negative Supply



PART ORDERING INFORMATION

Part Number	Package	Marking
CTSLV392NG	MLP8	P1G / YWW