

PES1600-12-080ND

DC-DC Front-End Power Supply

The PES1600-12-080ND is a 1600 Watt DC to DC power supply that converts -40 to -75 VDC voltage into an insulated main output of +12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches. The PES1600-12-080ND utilizes full digital control architecture for greater efficiency, control, and functionality.

This power supply meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).



Key Features & Benefits

- Designed to meet Intel CPRS compatibility
- Wide input voltage range: -40 to -75 VDC
- 1600 W continuous output power capability
- Always-on 12 VSB / 3.5 A standby output
- Hot-plug capable
- Parallel operation with active current sharing
- Full digital controls for improved performance
- High power density design: 42 W/in³
- Small form factor: 80 x 40 x 195 in mm
- Hot-plug capable
- PMBus® communication interface for control, programming and monitoring
- Status LED with fault signaling

Applications

- Networking Switches
- Servers & Routers
- Telecommunications

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1. ORDERING INFORMATION

PES	1600	-	12	-	080	N	D
Product Family	Power Level	Dash	V1 Output	Dash	Width	Airflow	Input
PES Front-Ends	1600 W		12 V		80 mm	N: Normal	D: DC

2. OVERVIEW

The PES1600-12-080ND DC/DC power supply is a DSP controlled, highly efficient front-end power supply. It incorporates state of the art technology and uses an interleaved forward converter topology with active clamp and synchronous rectification to reduce component stresses, thus providing increased system reliability and very high efficiency.

With a wide input DC voltage range the PES1600-12-080ND maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow path.

An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.

The always-on standby output provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.

Status information is provided with a front-panel LED. In addition, the power supply can be controlled and the fan speed set via the I2C bus. The I2C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C bus.

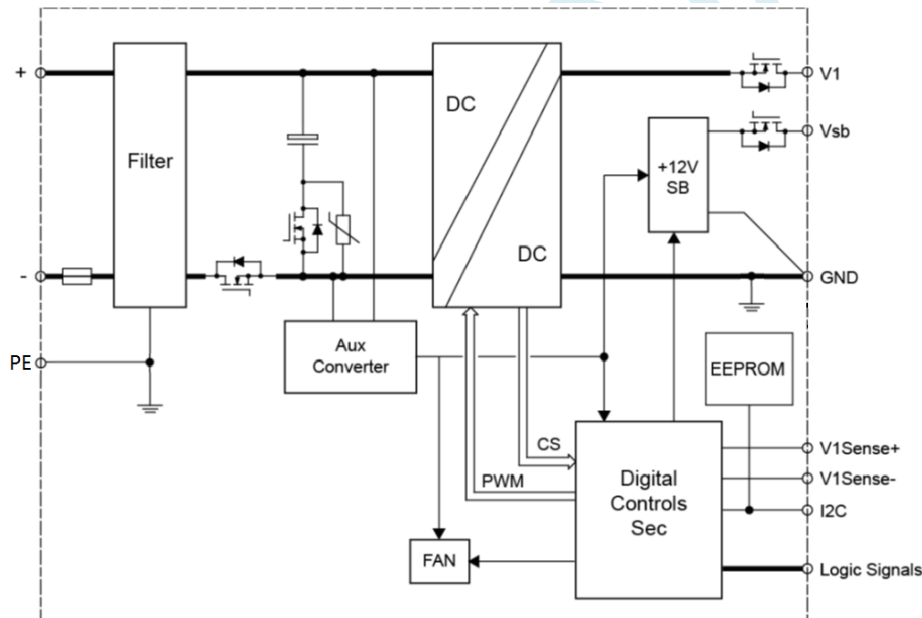


Figure 1. PES1600-12-080ND Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER	CONDITIONS / DESCRIPTION	MIN	MAX	UNITS
$V_i \text{ maxc}$	Maximum Input Continuous		-78	VDC

4. INPUT

General Condition: $T_A = 0 \dots 55 \text{ }^\circ\text{C}$, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_i \text{ start}$	Minimum operating input voltage	-30			VDC
$V_i \text{ nom}$	Nominal input voltage	-48		-60	VDC
V_i	Input voltage	-40		-75	VDC
I_i	Input current			46	A
$I_i \text{ pk}$	Inrush current limitation			50	A
$V_i \text{ vsb_on}$	Turn-on standby input voltage	-30		-32	VDC
$V_i \text{ vsb_off}$	Turn-off standby input voltage	-28		-30	VDC
$V_i \text{ v1_on}$	Turn-on V1 input voltage	-38		-40	VDC
$V_i \text{ v1_off}$	Turn-off V1 input voltage	-37		-39	VDC
η	Efficiency ¹	$V_i = -48 \text{ VDC}; -60 \text{ VDC}; 10\% \text{ load}$		82	%
		$V_i = -48 \text{ VDC}; -60 \text{ VDC}; 20\% \text{ load}$		90	%
		$V_i = -48 \text{ VDC}; -60 \text{ VDC}; 50\% \text{ load}$		94	%
		$V_i = -48 \text{ VDC}; -60 \text{ VDC}; 100\% \text{ load}$		91	%
T_{V1_holdup}	Hold-up time V1	133 A on I1, 3.5 A on Vsb		2.5	ms
T_{VSB_holdup}	Hold-up time Vsb	Vsb full load		15	ms

4.1 INPUT FUSE

A fast-acting 60 A input fuse in the negative voltage path inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

4.2 INRUSH CURRENT

Internal bulk capacitors will be charged through resistors connected from bulk cap minus pin to the DC rail minus, thus limiting the inrush current. After the inrush phase, NTC resistors are then shorted with MOSFETs connected in parallel. The Inrush control is managed by the digital controller (DSP).

4.3 INPUT UNDER-VOLTAGE

If the input voltage stays below the input under voltage lockout threshold $V_i \text{ on}$, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

4.4 EFFICIENCY

High efficiency (see [Figure 2](#)) is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

¹ Efficiency measured without fan power per EPA server guidelines.

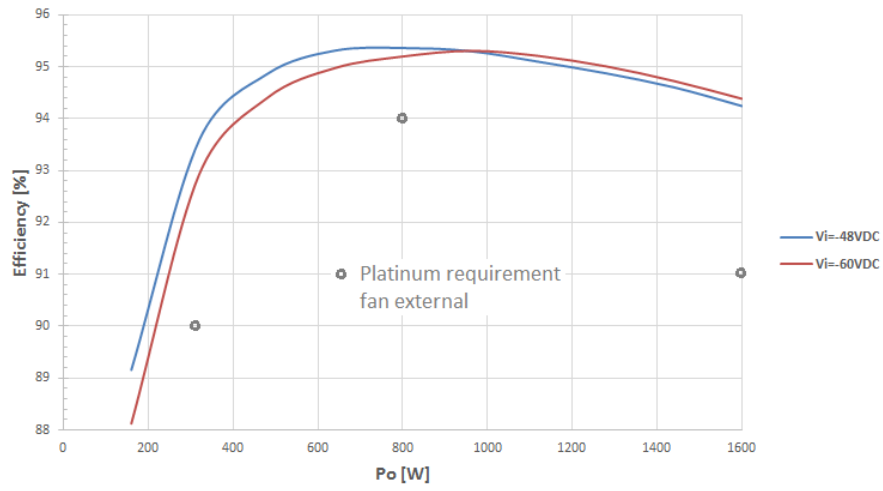


Figure 2. Efficiency vs. Load current (ratio metric loading)

PRELIMINARY

4.5 DC LINE TRANSIENT TEST

MINUS 75 VDC LINE TRANSIENT TEST

A standard line voltage momentary transient test is shown below. This test simulates a momentary voltage overshoot. This should not affect the operation of the PSU, the output voltage should remain in regulation. This test shall be conducted every 10 sec for 30 min (180 times total).

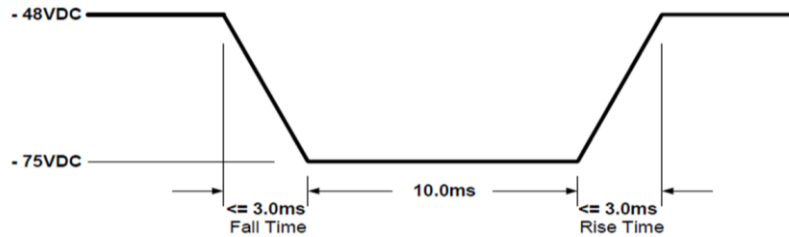


Figure 3. Minus 75 VDC Line Transient Test

0 V LINE TRANSIENT TEST

A standard line voltage momentary blackout test is shown below. This test simulates a momentary switch throw off-on, see graph below. The power supply should restart, not latch. This test shall be conducted 3 times in 10 min intervals. Practically a blackout of any duration should not damage the power supply in any way and not cause a latch off condition.

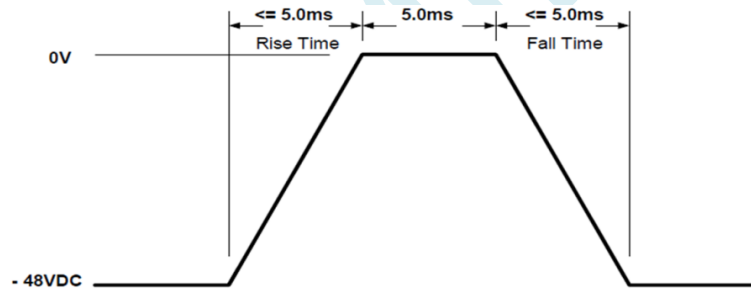


Figure 4. 0 V Line Transient Test

The power supply shall also be able to withstand the following transients:

DURATION	SLOPE / RATE	OUTPUT	PERFORMANCE CRITERIA
200 μs max	-48 V \rightarrow 30 V W / + 2 V / μs	Rated DC Voltages	No loss of function or performance
	-30 V \rightarrow 48 V W / -2 V / μs	Rated DC Voltages	No loss of function or performance

Table 1. Line Voltage Transient Limits

5. OUTPUT

General condition: $T_A = 0 \dots 55 \text{ }^\circ\text{C}$, $V_I = -48 \text{ VDC}$ unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V_I					
$V_{I \text{ nom}}$	Nominal Output Voltage		12.0		VDC
$V_{I \text{ set}}$	Output Set Point Accuracy	$0.5 \cdot I_{I \text{ nom}}$, $T_A = 25^\circ\text{C}$	-1	+1	$\%V_{I \text{ nom}}$
$dV_I \text{ load}$	Load Regulation	0 to 100% $I_{I \text{ nom}}$		480	mV
$dV_I \text{ line}$	Line Regulation	$V_{I \text{ min}}$ to $V_{I \text{ max}}$		120	mV
$dV_I \text{ tot}$	Total Regulation	$V_{I \text{ min}}$ to $V_{I \text{ max}}$, 0 to 100% $I_{I \text{ nom}}$	-5	+5	$\%V_{I \text{ nom}}$
$P_{I \text{ nom}}$	Nominal Output Power	$V_{I \text{ min}}$ to $V_{I \text{ max}}$		1600	W
$I_{I \text{ peak}}$	Peak Output Loading	$V_{I \text{ min}}$ to $V_{I \text{ max}}$ (max 20 s)		150	ADC
		$V_{I \text{ min}}$ to $V_{I \text{ max}}$ (max 100 μs)		205	ADC
$I_{I \text{ nom}}$	Output Current	$V_{I \text{ min}}$ to $V_{I \text{ max}}$	0	133	ADC
$V_{I \text{ pp}}$	Output Ripple Voltage ²	$V_{I \text{ min}}$ to $V_{I \text{ max}}$, 0 to 100% $I_{I \text{ nom}}$, 20MHz Bandwidth		120	mVpp
$dI_{I \text{ share}}$	Current Sharing	Deviation from $I_{I \text{ tot}} / N$, $I > 20\%$	-5	+5	$\% I_{I \text{ nom}}$
$V_{I \text{ SHARE}}$	Current Share Bus Voltage	$I_{I \text{ nom}}$		8	VDC
$dV_I \text{ dyn}$	Dynamic Load Regulation	Test frequency between 50Hz and 5KHz at duty cycles from 10% to 90%, $\Delta I_1 = 60\% I_{I \text{ nom}}$, $I_1 = 3A \dots 100\% I_{I \text{ nom}}$, 2000 μF capacitive loading	11.40	12.60	VDC
t_{rec}	Recovery Time	$dI_1/dt = 0.25A/\mu\text{s}$, recovery within 1% of $V_{I \text{ nom}}$		2	ms
$t_{V_I \text{ rise}}$	Output Voltage Rise Time	$V_I = 10 \dots 90\% V_{I \text{ nom}}$, $C_{\text{ext}} < 10 \text{ mF}$	1	70	ms
$t_{V_I \text{ ovr sh}}$	Output Turn-on Overshoot	$V_{I \text{ nom}}$, 0 to 100% $I_{I \text{ nom}}$		0.6	V
$dV_I \text{ sense}$	Remote Sense	Compensation for cable drop, 0 to 100% $I_{I \text{ nom}}$		0.25	V
$C_{V_I \text{ load}}$	Capacitive Loading			22	mF
Standby Output V_{SB}					
$V_{SB \text{ nom}}$	Nominal Output Voltage		12.0		VDC
$V_{SB \text{ set}}$	Output Set point Accuracy	$0.5 \cdot I_{SB \text{ nom}}$, $T_A = 25^\circ\text{C}$	-1	+1	$\%V_{SB \text{ nom}}$
$dV_{SB \text{ load}}$	Load Regulation	0 to 100% $I_{SB \text{ nom}}$		480	mV
$dV_{SB \text{ line}}$	Line Regulation	$V_{I \text{ min}}$ to $V_{I \text{ max}}$		120	mV
$dV_{SB \text{ tot}}$	Total Regulation	$V_{I \text{ min}}$ to $V_{I \text{ max}}$, 0 to 100% $I_{SB \text{ nom}}$	-5	+5	$\%V_{SB \text{ nom}}$
$P_{SB \text{ nom}}$	Nominal Output Power	$V_{I \text{ min}}$ to $V_{I \text{ max}}$		42	W
$I_{SB \text{ peak}}$	Peak Output Loading	$V_{I \text{ min}}$ to $V_{I \text{ max}}$		4	ADC
$I_{SB \text{ nom}}$	Output Current	$V_{I \text{ min}}$ to $V_{I \text{ max}}$	0	3.5	ADC
$V_{SB \text{ pp}}$	Output Ripple Voltage ¹	$V_{I \text{ min}}$ to $V_{I \text{ max}}$, 0 to 100% $I_{SB \text{ nom}}$, 20 MHz bandwidth		120	mVpp
$dV_{SB \text{ dyn}}$	Dynamic Load Regulation	$\Delta I_{SB} = 50\% I_{SB \text{ nom}}$, $I_{SB} = 0 \dots 100\% I_{SB \text{ nom}}$, $dI_{SB}/dt = 0.25 A/\mu\text{s}$, recovery within 1% of $V_{SB \text{ nom}}$	11.40	12.60	VDC
t_{rec}	Recovery Time			2	ms
$t_{V_{SB} \text{ rise}}$	Output Voltage Rise Time	$V_{SB} = 10 \dots 90\% V_{SB \text{ nom}}$	5	10	ms
$t_{V_{SB} \text{ ovr sh}}$	Output Turn-on Overshoot	$V_{I \text{ nom HL}}$, 0 to 100% $I_{SB \text{ nom}}$		0.6	V
$C_{V_{SB} \text{ load}}$	Capacitive Loading			1000	μF

² Ripple noise and dynamic load measured with a 10 μF low ESR capacitor in parallel with a 0.1 μF ceramic capacitor at the point of measurement.

5.1 OUTPUT GROUND / CHASSIS CONNECTION

The output return path serves as power and signal ground. All output voltages and signals are referenced to these pins. To prevent a shift in signal and voltage levels due to ground wiring voltage drop a low impedance ground plane should be used as shown in *Figure 5*. Alternatively, separated ground signals can be used as shown in *Figure 6*. In this case the two ground planes should be connected together at the power supplies ground pins.

NOTE: Within the power supply the output GND pins are connected to the Chassis, which in turn is connected to the Protective Earth terminal. Therefore, it is not possible to set the potential of the output return (GND) to any other than Protective Earth potential.

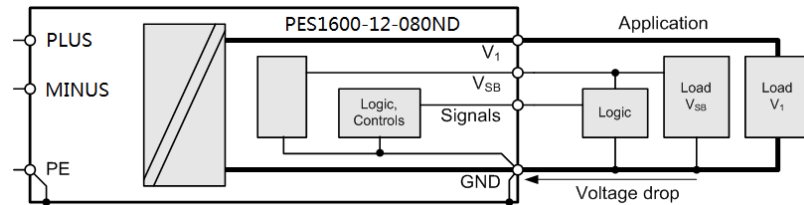


Figure 5. Common Low Impedance Ground Plane

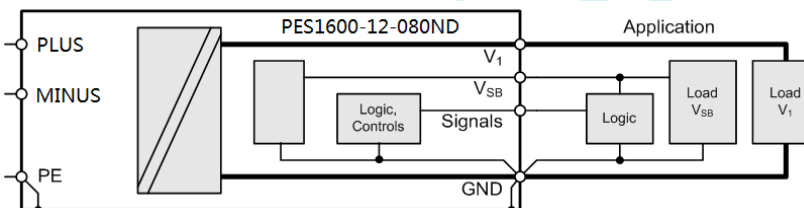


Figure 6. Separated Power and Signal Ground

5.2 CLOSED LOOP STABILITY

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges. A minimum of: 45 degrees phase margin and -10dB-gain margin is required. The power supply manufacturer shall provide proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at 10%, 20%, 50% and 100% loads as applicable, 0% is just for reference.

5.3 RESIDUAL VOLTAGE IMMUNITY IN STANDBY MODE

The power supply should be immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to 500mV. There shall be no additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when DC voltage is applied and the PSON_L signal is de-asserted.

5.4 COMMON MODE NOISE

The common mode noise on any output shall not exceed 350mV pk-pk over the frequency band of 10Hz to 20MHz.

The measurement shall be made across a 100Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure), the test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

5.5 SOFT STARTING

The Power Supply shall contain control circuit which provides monotonic soft start for its outputs without overstress of the DC line or any power supply components at any specified DC line or load conditions.

5.6 ZERO LOAD STABILITY REQUIREMENTS

When the power subsystem operates in a no load condition, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault.

5.7 HOT SWAP REQUIREMENTS

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply shall use a latching mechanism to prevent insertion and extraction of the power supply when the DC power cord is inserted into the power supply.

5.8 FORCED LOAD SHARING

The PES front-ends have an active current share scheme implemented for V1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses an analog bus to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV. The output will share within 10% at full load.

The 12 V_{SB} output is not required to actively share current between power supplies (passive sharing).

5.9 RIPPLE / NOISE

The test set-up shall be following *Figure 7*.

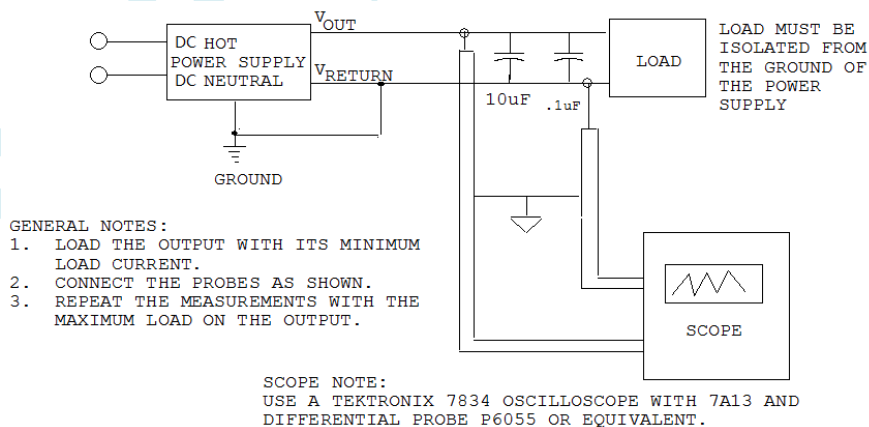


Figure 7. Differential Noise Test Setup

NOTES: Load must be isolated from the safety ground to *Figure 7*.

When performing this test, the probe clips and capacitors should be located close to the load.

6. PROTECTION

General Condition: $T_A = 0 \dots 55 \text{ }^\circ\text{C}$, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input fuse (L)		60		A
V_{1OV}	OV Threshold V_1	13.0	13.9	14.5	VDC
$V_{SB OV}$	OV Threshold V_{SB}	13.0	13.9	14.5	VDC
V_{1UV}	UV Threshold V_1		11.2		VDC
$V_{SB UV}$	UV Threshold V_{SB}		11.2		VDC
I_{V1OC}	OC Limit V_1				Refer to section 6.5
$I_{VSB OC}$	OC Limit V_{SB}	4.5		5.5	A
T_{SD}	Over Temperature on Critical Points				Refer to Table 17
					$^\circ\text{C}$

6.1 PROTECTION CIRCUITS

Protection circuits inside the power supply shall cause only the power supply's main output to shut down. If the power supply latches off due to a protection circuit tripping, a DC OFF for 15sec and a PSON_L cycle HIGH for 1sec shall be able to reset the power supply.

6.2 OVER TEMPERATURE PROTECTION (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature.

In an OTP condition the PSU will shut down, when the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on, the OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition, the OTP trip temperature level shall be at least 5°C higher than over temperature warning threshold level.

6.3 OVER VOLTAGE PROTECTION

The PES1600-12-080ND front-end provides a fixed threshold overvoltage (OV) protection implemented with a HW comparator for both the main and the standby output. Once an OV condition has been triggered on the main output, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the DC mains or by toggling the PSON_L input. 12VSB will be auto-recovered after removing OVP limit.

6.4 UNDER VOLTAGE DETECTION

Both main and standby outputs are monitored. PWOK_H pin signal if the output voltage exceeds $\pm 5\%$ of its nominal voltage.

The main output will latch off if the main output voltage when V_1 falls below 11.2 V (typically in an overload condition), the latch can be unlocked by disconnecting the supply from the DC mains or by toggling the PSON_L input.

If the standby output leaves its regulation bandwidth for more than 10ms then the main output is disabled to protect the system.

6.5 OVER CURRENT LIMIT & OVER POWER PROTECTION (OCP & OPP)

The power supply shall have current limit to prevent the outputs from exceeding the values shown in *Table 2*. If the current limits are exceeded the power supply shall shutdown and latch off. The latch will be cleared only by a DC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. 12VSB will be auto-recovered after removing OCP limit.

NORM	DESCRIPTION	CURRENT THRESHOLD (A)		TRIP TIMING		TESTING RANGE	COMMENTS
		MIN	MAX	MIN	MAX		
OCP1	Fast over current protection (shutdown, latch)	210	225	10 μ s	100 μ s	OCP1 to Short Circuit	
OPP	Over power protection (voltage foldback)	195	210	5 ms	20 ms	OPP to V fold back to 8 V	
OCW1	Fast over current warning (SMB_ALERT_L)	180	195	5 μ s	20 μ s		SMB_ALERT_L Latch and hold for 50-150 ms
OCP2	Slow over current protection (shutdown, latch)	150	180	50 ms	100 ms		
OCW2	Slow over current warning (SMB_ALERT_L)	150	180	15 ms	50 ms		
OCPstby	Standby over current protection (shutdown, hiccup mode)	4.5	5.5				10 ms minimum delay

Table 2. OCP & OPP

The power supply shall have a circuit to quickly assert the SMB_ALERT_L signal when the output current exceeds the over power protection threshold in the PSU, The SMB_ALERT_L signal must always assert before the over power protection threshold is exceeded. SMB_ALERT_L must always latch for about 100msec before being released.

6.6 PEAK LOAD WITH ADDED SYSTEM BUFFER CAPACITANCE

The power supply shall be able to support higher peak power levels with added system buffer capacitance for up to 100 μ sec. *Table 3* are PMAX testing conditions.

PEAK POWER	PEAK CURRENT	SYSTEM CAPACITANCE	PEAK LOAD DURATION	VOLTAGE UNDERSHOOT
2460 W	205 A	6,150 μ F	100 μ s	5%

Table 3. PMAX Testing Conditions

7. MONITORING

The power supply operating parameters can be accessed through I²C interface. For more details refer to chapter I²C / PMBus® COMMUNICATION and document PES1600-12-080ND PMBus® Communication Manual.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ mon}$	Input Voltage $V_{i\ min\ LL} \leq V_i \leq V_{i\ max}$	-2		+2	VDC
$I_{i\ mon}$	Input Current	-0.35		+0.35	A
$P_{i\ mon}$	True Input Power	$I_1 < 10\% I_{1\ nom}$		+15	W
		10% $I_{1\ nom} < I_1 < 20\% I_{1\ nom}$	-4	+4	%
		$I_1 > 20\% I_{1\ nom}$	-2	+2	%
$E_{i\ mon}$	Total Input Energy	$I_1 < 10\% I_{1\ nom}$		+15	W
		10% $I_{1\ nom} < I_1 < 20\% I_{1\ nom}$	-4	+4	%
		$I_1 > 20\% I_{1\ nom}$	-2	+2	%
$V_{i\ mon}$	V_i Voltage	-1		+1	%
$I_{i\ mon}$	V_i Current	$I_1 < 10\% I_{1\ nom}$	-1	+1	ADC
		10% $I_{1\ nom} < I_1 < 20\% I_{1\ nom}$	-5	+5	%
		$I_1 > 20\% I_{1\ nom}$	-2	+2	%
P_{nom}	V_i Output Power	$I_1 < 10\% I_{1\ nom}$		+15	W
		10% $I_{1\ nom} < I_1 < 20\% I_{1\ nom}$	-6	+6	%
		$I_1 > 20\% I_{1\ nom}$	-3	+3	%
E_{nom}	V_i Output Energy	$I_1 < 10\% I_{1\ nom}$		+15	W
		10% $I_{1\ nom} < I_1 < 20\% I_{1\ nom}$	-6	+6	%
		$I_1 > 20\% I_{1\ nom}$	-3	+3	%
$T_{amb\ mon}$	Ambient Temperature	0°C		55°C	°C
F_s	Fan speed	-500		+500	RPM

8. SIGNALING AND CONTROL

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
PSON_L					
V_{iL}	Input Low Level Voltage			0.8	V
V_{iH}	Input High Level Voltage			5.25	V
$I_{iL,H}$	Maximum Source Current			4	mA
$R_{pull\ up}$	Pull-up to 3V3 Located in Power Supply		10		kΩ
PWOK_H					
V_{oL}	Output Low Level Voltage			0.4	V
V_{oH}	Output High Level Voltage		2.4	3.46	V
I_s	Maximum Sink Current			400	μA
	Maximum Source Current			2	mA
SMB_ALERT_L					
V_{ext}	Maximum External Pull up Voltage			3.46	V
V_{oL}	Output Low Level Voltage			0.4	V
$R_{pull\ up}$	Pull-up to 3V3 Located in Power Supply		None		
I_s	Sink Current			4	mA
				50	μA
VIN_OK_H					
V_{ext}	Maximum External Pull up Voltage			3.46	V
V_{oL}	Output Low Level Voltage			0.4	V
$R_{pull\ up}$	Pull-up to 3V3 Located in Power Supply		1		kΩ
I_s	Sink Current			4	mA

8.2 SENSE INPUTS

The main output has sense lines implemented to compensate for voltage drop on load wires in both positive and negative path. The maximum allowed voltage drop is 200 mV on the positive rail and 50 mV on the GND rail.

With open sense inputs the main output voltage will rise by 250 mV. Therefore, if not used, these inputs should be connected to the power output and GND at the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.3 PRESENT_L OUTPUT

The PRESENT_L pin is wired through a 100Ω resistor to internal GND within the power supply. This pin does indicate that there is a power supply present in this system slot. An external pull-up resistor has to be added within the application. Current into PRESENT_L should not exceed 5mA to guarantee a low level voltage if power supply is seated.

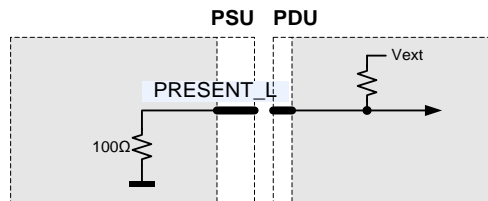


Figure 8. PRESENT_L Connection

8.4 PSON_L INPUT

The PSON_L is an internally pulled-up (3.3 V) input signal to enable/disable the main output V1 of the front-end. With low level input the main output is enabled. This active-low pin is also used to clear any latched fault condition. The PSON_L can be either controlled by an open collector device or by a voltage source.

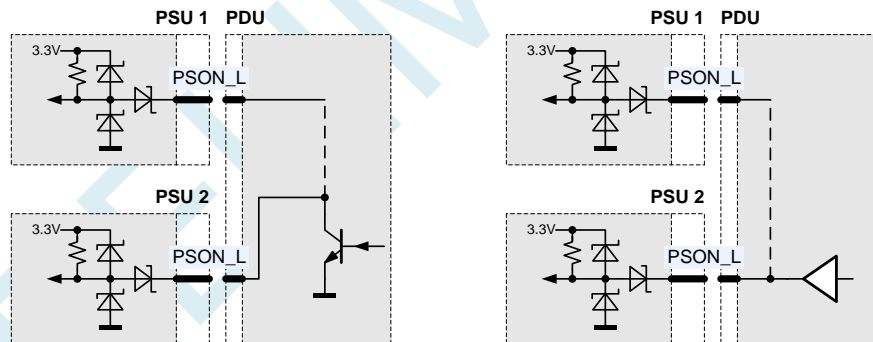


Figure 9. PSON_L connection

8.5 PWOK_H OUTPUT

PWOK_H is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK_H will be de-asserted to a LOW state. The start of the PWOK_H delay time shall be inhibited as long as any power supply output is in current limit.

The PWOK_H and I2C bus of PSU are connected together on the redundant system. The below block diagram was shown the wiring on the system. The internal PWOK_H circuit of power supply is designed so that the PWOK_H bus is the wire-ORed function of the individual PWOK_H signals of all the power supply in parallel. Suggest system Pull-up to 3V3 and pull-up resistance is 10K. The PWOK_H signal also can be separated for each PSU design in system side to indicate each PSU output state.

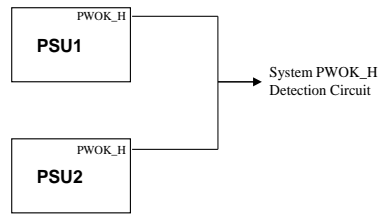


Figure 10. PWOK_H connection

8.6 SMB_ALERT_L OUTPUT

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. It is asserted (pulled Low) at Shutdown or Warning events such as reaching temperature warning/shutdown threshold of critical component, general failure, over-current, over-voltage, under voltage or low-speed of failed fan. This signal may also indicate the power supply is operating in an environment exceeding the specified limits. This signal is to be asserted in parallel with LED turning solid Yellow.

The inlet temperature warning threshold must be set at 63C, preventing exhaust air and cord temperatures temperature exceeding safety ratings. The warning gets de-asserted once inlet air temperature returns into specified operating temperature range. Fan speed control algorithm shall ramp up the fan speed to the maximum prior to the OT_WARNING bit set in STATUS_TEMPERATURE (7Dh) register.

In case exhaust air temperature exceeds 70C higher temp rating cord must be used.

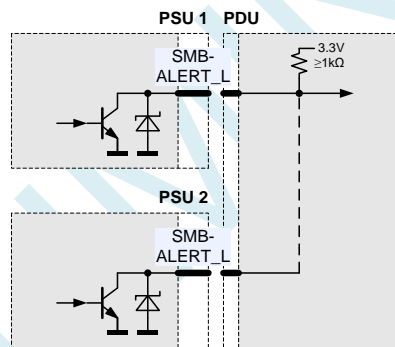


Figure 11. SMB_ALERT_L Connection

8.7 VIN_OK_H OUTPUT

This signal will be asserted, driven high, by the power supply to indicate that the input voltage meets the minimum requirements of the parametric PSU specification.

The PSU shall de-assert (drive low) under input over-voltage condition.

DC LINE AND DC LOSS DETECTION ALGORITHM

DC line voltage detection for power on:

The power supply will use Vrms to determine if the input voltage is within the specified requirements for turning on the power supply unit as called out by the individual power supply specification for DC input voltage range. The Vrms of the input must be determined within 100 ms after the application of DC & Standby has reached regulation. Assertion requirements for VIN_OK_H remain the same.

DC line voltage detection for a DC brownout and dropout:

PSU shall detect both DC brown out and dropout conditions and issue a power down warning to the end system. The PSU shall de-assert (drive low) VIN_OK_H at least 1mS (T1) prior to the de-assertion of PWOK_H upon input conditions that fall below the Vin (turn-off) specification of the PSU parametric specification. Under such conditions. After VIN_OK_H de-assertion, the PSU shall be capable of delivering all outputs within the regulation limits for at least 1mS before de-asserting PWOK_H (T1). In a similar manner the PSU shall de-assert PWOK_H a minimum of 1ms prior to the main rail voltage degrading to 95% of the set point voltage value. Upon a VIN_OK_H de-assertion, the PSU shall derive an average RMS input voltage, measured

over a moving average window equal to T2, to establish if conditions meet the requirements for assertion of VIN_OK_H. Refer to Figure 12.

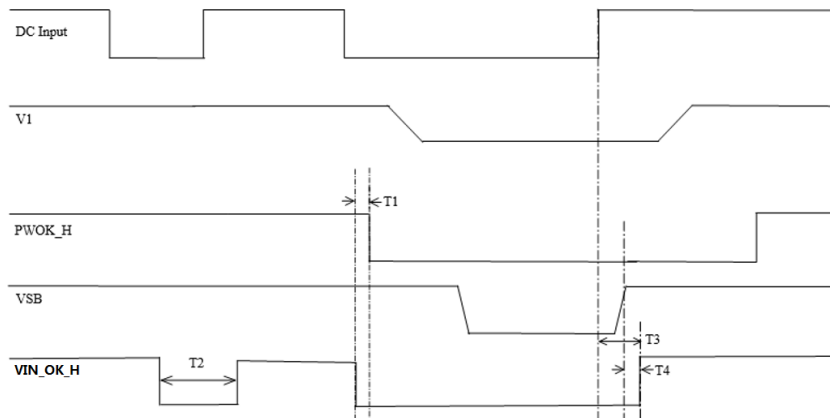


Figure 12. VIN_OK_H Timing

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T1	VIN_OK_H & PWOK_H	1			ms
T2	VIN_OK_H Dwell Time	75		120	ms
T3	VIN_OK_H delay to AC			1700	ms
T4	VIN_OK_H to 12VSB			20	ms

NOTE: T2 is the minimum VIN_OK_H de-assertion dwell time that is initiated when the PSU has declared a loss of input voltage.

Table 4. VIN_OK_H Timing Requirements

8.8 TIMING REQUIREMENTS

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 1 to 70ms. For 12VSB, it is allowed to rise from 5.0 between 10ms. All outputs must rise monotonically. Table 5 shows the timing requirements for the power supply being turned on and off two ways; 1) via the DC input with PSON_L held low; 2) via the PSON_L signal with the DC input applied. The PSU needs to remain off for 1 second minimum after PWOK_H is de-asserted.

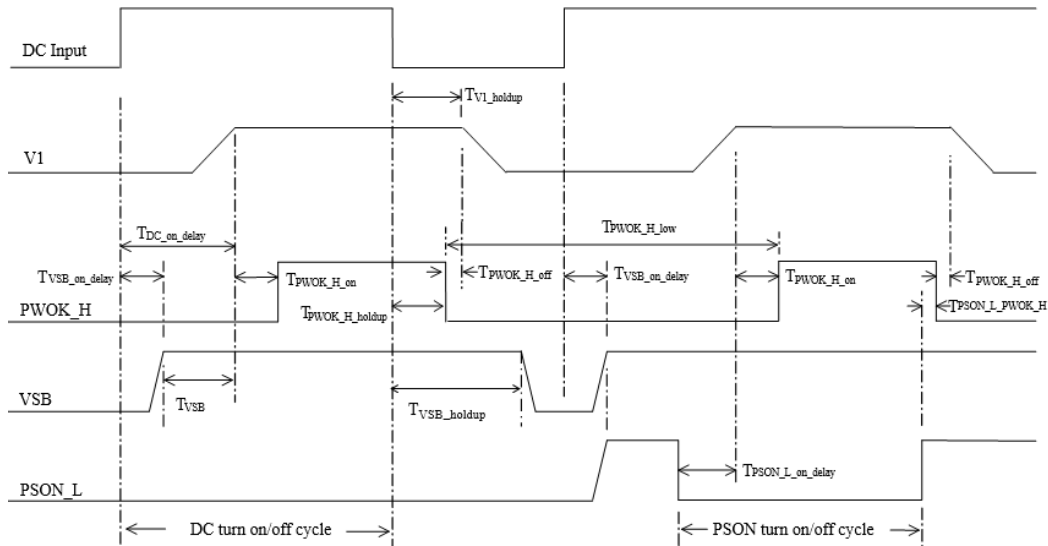


Figure 13. Turn On/Off Timing

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
TV1_rise	Output voltage rise time	1.0 *		70 *	ms
TVSB_on_delay	Delay from DC being applied to 12 VSB being within regulation.			1500	ms
TDC_on_delay	Delay from DC being applied to all output voltages being within regulation.			3000	ms
TV1_holdup	Time 12 V output voltage stay within regulation after loss of DC.	2.5			ms
TPWOK_H_holdup	Delay from loss of DC to de-assertion of PWOK_H	1			ms
TPSON_L_on_delay	Delay from PSON_L active to output voltages within regulation limits.	5		400	ms
TPSON_L_PWOK_H	Delay from PSON_L deactivate to PWOK_H being de-asserted.			5	ms
TPWOK_H_on	Delay from output voltages within regulation limits to PWOK_H asserted at turn on.	100		500	ms
TPWOK_H_off	Delay from PWOK_H de-asserted to output voltages dropping out of regulation limits.	1			ms
TPWOK_H_low	Duration of PWOK_H being in the de-asserted state during an off/on cycle using DC or the PSON_L signal.	100			ms
TVSB	Delay from 12 VSB being in regulation to O/Ps being in regulation at DC turn on.	50		1000	ms
TVSB_holdup	Time the 12VSB output voltage stays within regulation after loss of DC.	15			ms
TDC_off_SMB_ALERT_L	The power supply shall assert the SMB_ALERT_L signal quickly after a loss of DC input voltage.			2	ms

* The 12VSB output voltage rise time shall be from 5.0 ms between 10 ms.

Table 5. Timing Requirements

8.9 HOT_STANDBY

The hot-standby operation is an operating mode allowing to further increase efficiency at light load conditions in a redundant power supply system. Under specific conditions one of the power supplies is allowed to disable Oring gate, to make sure into hot standby mode. This will save the power losses associated with this power supply and at the same time the other power supply will operate in a load range having a better efficiency.



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8.10 LED INDICATOR

The front-end has one front LED showing the status of the supply. The LED is bi-colored: green and amber, and indicates DC and DC power presence and warning or fault conditions. [Table 7](#) lists the different LED status.

	MIN λ_d WAVELENGTH	NOMINAL λ_d WAVELENGTH	MAX λ_d WAVELENGTH	UNITS
Green		570		nm
Yellow		590		nm

Table 6. LED Characteristics

OPERATING CONDITION	LED STATE
Output ON and OK	Solid GREEN
No AC power to all power supplies	OFF
AC present / Only 12 VSB on (PS off) or PS in Hot standby state	1Hz Blink GREEN
AC cord unplugged; with a second power supply in parallel still with AC input power.	Solid AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink AMBER
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	Solid AMBER
Power supply in FW upload mode	2Hz Blink GREEN

Table 7. LED Status

9. I²C / PMBus® COMMUNICATION

The PES front-end is a communication Slave device only; it never initiates messages on the I²C/SMBus by itself. The communication bus voltage and timing is defined in [Table 8](#) further characterized through:

- The SDA/SCL IOs use 3V3 logic levels
- External pull-up resistors on SDA/SCL required for correct signal edges
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

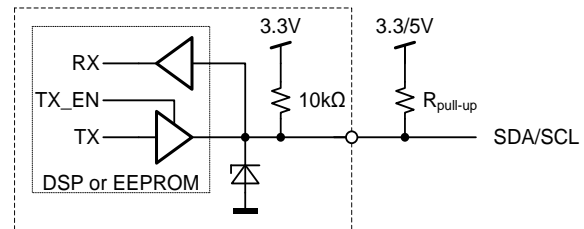


Figure 14. Physical layer of communication interface

Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible as long as it is connected to a life V_{SB} output or V_I output (provided e.g. by the redundant unit).

PARAMETER	DESCRIPTION	CONDITION	MIN	MAX	UNIT
SCL / SDA					
V_L	Input low voltage		-0.5	1.0	V
V_H	Input high voltage		2.3	3.5	V
V_{hys}	Input hysteresis		0.15		V
V_{oL}	Output low voltage	3 mA sink current	0	0.4	V
t_r	Rise time for SDA and SCL		$20+0.1C_b^1$	300	ns
t_{of}	Output fall time $V_{IHmin} \rightarrow V_{ILmax}$	$10 \text{ pF} < C_b^1 < 400 \text{ pF}$	$20+0.1C_b^1$	250	ns
I	Input current SCL/SDA	$0.1 \text{ VDD} < V_i < 0.9 \text{ VDD}$	-10	10	μA
C_i	Internal Capacitance for each SCL/SDA			50	pF
f_{SCL}	SCL clock frequency		0	100	kHz
$R_{pull-up}$	External pull-up resistor	$f_{SCL} \leq 100 \text{ kHz}$		$1000 \text{ ns} / C_b^1$	Ω
t_{HDSTA}	Hold time (repeated) START	$f_{SCL} \leq 100 \text{ kHz}$	4.0		μs
t_{LOW}	Low period of the SCL clock	$f_{SCL} \leq 100 \text{ kHz}$	4.7		μs
t_{HIGH}	High period of the SCL clock	$f_{SCL} \leq 100 \text{ kHz}$	4.0		μs
t_{SUSTA}	Setup time for a repeated START	$f_{SCL} \leq 100 \text{ kHz}$	4.7		μs
t_{HDDAT}	Data hold time	$f_{SCL} \leq 100 \text{ kHz}$	0	3.45	μs
t_{SUDAT}	Data setup time	$f_{SCL} \leq 100 \text{ kHz}$	250		ns
t_{SUSTO}	Setup time for STOP condition	$f_{SCL} \leq 100 \text{ kHz}$	4.0		μs
t_{BUF}	Bus free time between STOP and START	$f_{SCL} \leq 100 \text{ kHz}$	5		ms

¹ C_b = Capacitance of bus line in pF, typically in the range of 10...400 pF

Table 8. I²C / SMBus Specification

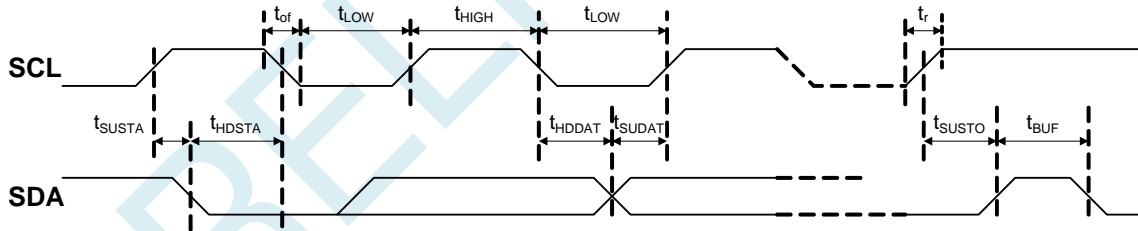


Figure 15. I²C / SMBus Timing

ADDRESS SELECTION

The address for I²C communication can be configured by pulling address input pins A2, A1 and A0 either to GND (Logic Low) or leave them open (Logic High). An internal pull up resistor will cause the A2 / A1 / A0 pin to be in High Level if left open.

A fixed addressing offset exists between the Controller and the EEPROM.



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A2	A1	A0	I2C Address *	
			Controller	EEPROM
0	0	0	0xB0	0xA0
0	0	1	0xB2	0xA2
0	1	0	0xB4	0xA4
0	1	1	0xB6	0xA6
1	0	0	0xB8	0xA8
1	0	1	0xBA	0xAA
1	1	0	0xBC	0xAC
1	1	1	0xBE	0xAE

* The LSB of the address byte is the R/W bit

Table 9. Address and Protocol Encoding

9.1 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I²C bus physical layer (see *Figure 16*) and can be accessed under different addresses, see ADDRESS SELECTION. The SDA/SCL lines are connected directly to the controller and EEPROM which are supplied by internal 3V3. The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

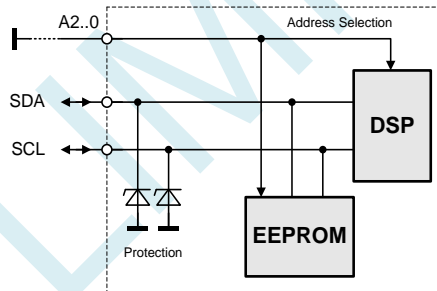


Figure 16. I2C Bus to DSP and EEPROM

9.2 EEPROM PROTOCOL

The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.



READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



9.3 PMBus® PROTOCOL

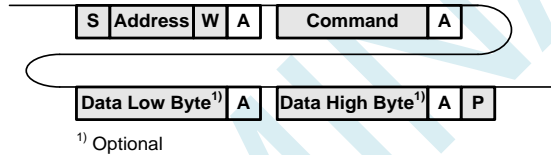
The Power Management Bus (PMBus®) is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org.

PMBus® command codes are not register addresses. They describe a specific command to be executed. The PES1600-12-080ND supply supports the following basic command structures:

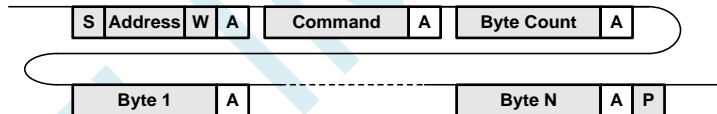
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).

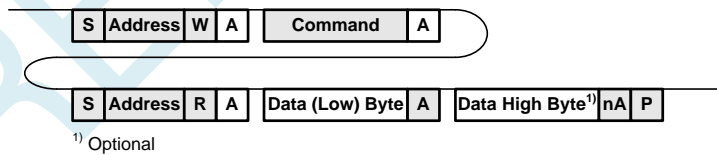


In addition, Block write commands are supported with a total maximum length of 255 bytes. See PES1600-12-080ND PMBus Communication Manual URP.00XXX for further information.

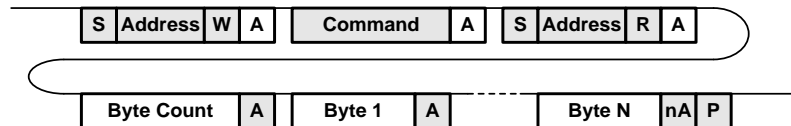


READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



In addition, Block read commands are supported with a total maximum length of 255 bytes. See PES1600-12-080ND PMBus Communication Manual URP.00XXX for further information.



9.4 POWER SUPPLY DIAGNOSTIC “EVENT RECORDER”

The power supply shall save the latest PMBus data and other pertinent data into nonvolatile memory when a critical event shuts down the power supply. This data shall be accessible via the PMBus® interface with an external source providing power to the 12 VSB output.

Critical Events to trigger an update to the Event Recorder includes:

- Output OVP
- Output OCP
- Input OV/UV Fault
- Fan fault
- OTP
- Other faults to cause output shutdown.

Refer to BCA_XXXXX_xx_PES1600-12-080ND PMBus® Communication Application Note for further information about the PMBus commands to support this function.

9.5 FIRMWARE UPDATE

The power supply shall have the capability to update its firmware via the PMBus interface while it is in standby mode. This FW can be updated when in the system and in standby mode and outside the system with power applied to the 12Vstby pins. BPS standard GUI supports the firmware upgrade function.

9.6 GRAPHICAL USER INTERFACE

Bel Power Solutions provides with its “f2C Utility” a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PES1600-12-080ND Front-End. The utility can be downloaded on:

<https://belfuse.com/power-solutions> and supports both the PSMI and PMBus® protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

If the GUI is used in conjunction with the YTM.00103 Evaluation Board it is also possible to control the PSON_L pin(s) of the power supply.

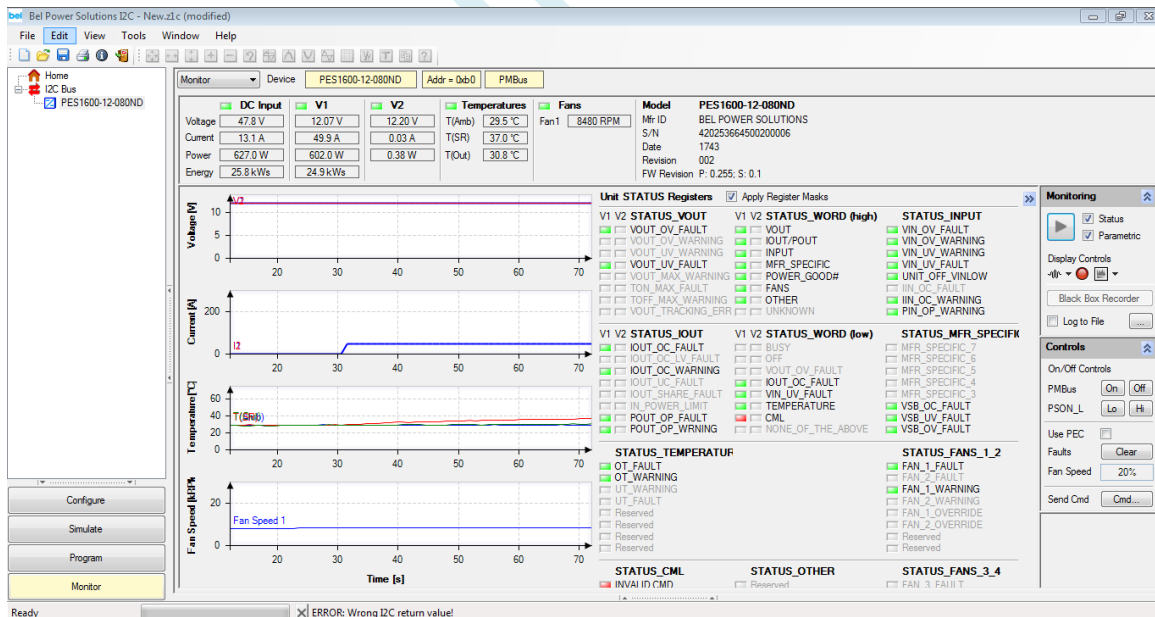


Figure 17. Monitoring dialog of the f2C Utility

10. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the air-flow at the rear of the supply by placing large objects directly at the output connector. The PES1600-12-080ND is provided with a rear to front airflow, which means the air enters through the DC-output of the supply and leaves at the DC-inlet. The PES1600-12-080ND supply has been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

The fan oscillation shall be controlled such that associated sound power level variation falls within a band of 2.0 dBA (roughly 10% mean speed). This condition may be treated as steady state fan speed condition.

After the new load and/or cooling condition steady state is established, transition to the steady state fan speed shall take place within 60s.

The PES1600-12-080ND provides access via I²C to the measured temperatures of in total 3 sensors within the power supply, see [Table 10](#). The microprocessor is monitoring these temperatures and if warning threshold of one of these sensors is reached it will set fan to maximum speed. If temperatures continue to rise above shut down threshold the main output V1 (or VSB if auxiliary converter is affected) will be disabled. At the same time the warning or fault condition is signalized accordingly through LED, PWOK_H and SMB_ALERT_L.

TEMPERATURE SENSOR	DESCRIPTION / CONDITION	PMBUS® REGISTER	WARNING THRESHOLD	SHUT DOWN THRESHOLD
Inlet air temperature	Sensor located on control board close to DC end of power supply	8Dh	63°C	68°C
Syn rectifier Mosfet 1	Sensor located close to Syn rectifier Mosfet group 1	8Eh	108°C	113°C
Syn rectifier Mosfet 2	Sensor located close to Syn rectifier Mosfet group 2	EAh	108°C	113°C

Table 10. Temperature Sensor Location and Thresholds

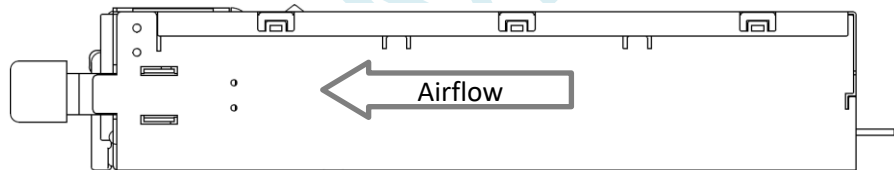


Figure 18. Airflow Direction

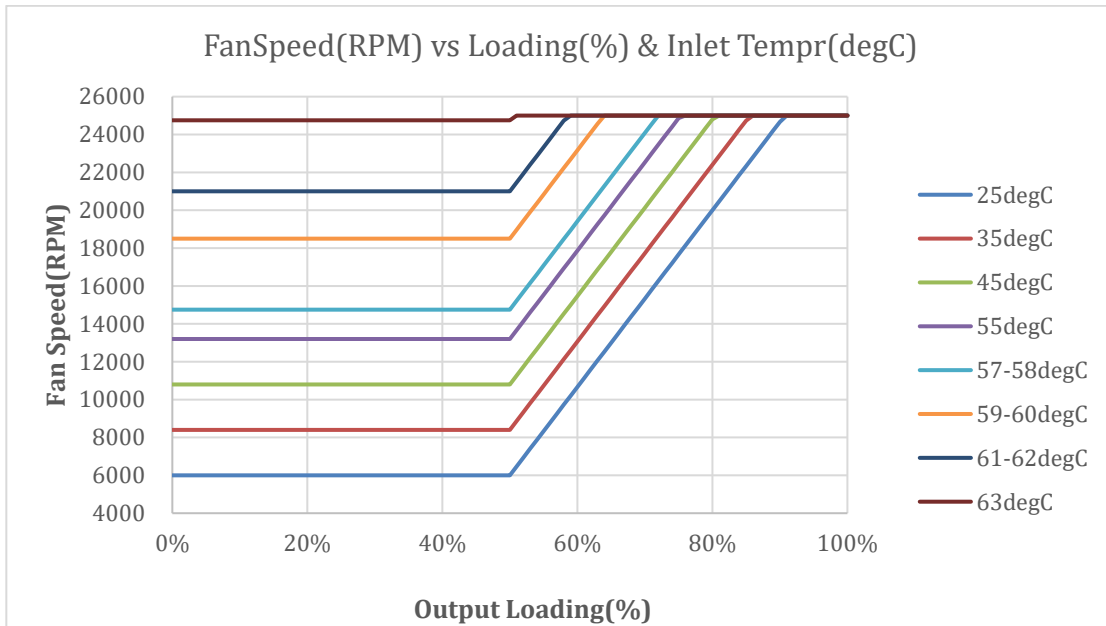


Figure 19. Fan Speed vs. Main Output Load

Comment: The fan minimum speed is 6000 RPM.

11. ELECTROMAGNETIC COMPATIBILITY

11.1 IMMUNITY

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	EN 55024: 2010/A1: 2015 using the IEC 61000-4-2: 2001-04 test standard and performance criteria B defined in Annex B of CISPR 24.	B
Radiated Electromagnetics Filled	EN 55024: 2010/A1: 2015 using the IEC 61000-4-3: 2002-09 test standard and performance criteria A defined in Annex B of CISPR 24	A
Burst	EN 55024: 2010/A1: 2015 using the IEC 61000-4-4: 2004-07 test standard and performance criteria B defined in Annex B of CISPR 24	B
Surge*	EN 55024: 2010/A1: 2015: 2001-04 the power supply shall be tested with the system for immunity to AC Unidirectional wave; 1kV line to ground and 1kV line to line.	B
RF Conducted Immunity	IEC / EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 ... 80 MHz	A

* The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.

The power supply shall be tested in accordance with IEC 61000-4-5: 2005 per EN55024: 2010/A1: 2015 and meet criterial B defined in session 7 of EN55024: 2010/A1: 2015, more criteria details refer to Table 18.

LEVEL	DESCRIPTION
A	During and after the test, the EUT shall continue to operate as intended without operator intervention.
B	Degradation of performance is allowed during test and the EUT shall continue to operate as intended without operator intervention after the test. And EUT can recover without operator intervention when test condition removed.
C	Temporary loss of function is allowed, provided the function is self-recoverable or can be restored by the operation of the controls or cycling of the power to the EUT by the user in accordance with the manufacturer's instructions.

Table 11. Performance Criteria

11.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN 55032:2015 / CISPR 32:2015: 0.15 ... 30 MHz, QP and AVG, single power supply	Class A
	EN 55032:2015 / CISPR 32:2015: 0.15 ... 30 MHz, QP and AVG, 2 power supplies in a system	Class A
Radiated Emission	EN 55032:2015 / CISPR 32:2015: 30 MHz ... 1 GHz, QP, single power supply	Class A
	EN 55032:2015 / CISPR 32:2015: 30 MHz ... 1 GHz, QP, 2 power supplies in a system	Class A

12. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	NOTE
Agency Approvals	Approved to latest edition of the following standards: UL60950-1/CSA 60950-1 (USA / Canada) EN60950-1 (Europe) IEC60950-1 (International)	Pending
	CB Certificate & Report, IEC60950-1 (report to include all country national deviations) Nordics – EMKO-TSE (74-SEC) 207/94 CE - Low Voltage Directive 2014/35/EC (Europe) GB4943.1- CNCA Certification (China)	
Isolation Strength	Input (L/N) to chassis (PE)	Basic
	Input (L/N) to output	Basic
	Output to chassis	None (Direct connection)
Electrical Strength Test	Input to output	1500 VDC
	Input to chassis	1500 VDC

Comment: All printed wiring boards and all connectors meet UL94V-0 level.

13. ENVIRONMENTAL

Power supply shall meet the thermal requirements under the load and environmental condition identified in each table. Even though the table addresses only the exhaust air temperature, all other components in the power supply shall also meet their temperature specifications and lifetime requirements.

The power supply must meet UL enclosure requirements for temperature rise limits. All sides of the power supply with exception to the air exhaust side must be classified as “Handle, knobs, grips, etc. held for short periods of time only”.

In case the exit air temperature requirement cannot be met, the power supply must have a warning label for high touch temperature that is in compliance with IEC/UL 60950-1 and additionally 85C rated power cords must also be used with this power supply.



ITEM	DESCRIPTION	MIN	MAX	UNITS
Load	Maximum typical load under redundant configurations		890	W
Top1	Operating temperature range; 900 m	0	55	°C
Top2	Operating temperature range; 3050 m	0	50	°C
Textit	Maximum exit air temperature		68	°C
Tnon-op	Non-operating temperature range	-40	70	°C
Altitude1	Maximum operating altitude; 50°C inlet		3050	meters
Altitude2	Maximum operating altitude; 55°C inlet		900	meters
Acoustical Noise	A-weighted sound power, 25°C, 50% Load		49	dB

Table 12. Requirements for Redundant Power Supply Configuration

TEM	DESCRIPTION	MIN	MAX	UNITS
Load	Maximum rated output load		1600	W
Top1	Operating temperature range; 900 m	0	45	°C
Top2	Operating temperature range; 3050 m	0	40	°C
Textit	Maximum exit air temperature		68	°C
Tnon-op	Non-operating temperature range	-40	70	°C
Altitude1	Maximum operating altitude; 40°C inlet		3050	meters
Altitude2	Maximum operating altitude; 45°C inlet		900	meters
Acoustical Noise	A-weighted sound power, 25°C, 50% Load		49	dB

Table 13. Requirements for Non-Redundant Power Supply Configuration (Typical System Ambient)

ITEM	DESCRIPTION	MIN	MAX	UNITS
Load	Maximum rated output load		1600	W
Top1	Operating temperature range; 900 m	0	55	°C
Top2	Operating temperature range; 3050 m	0	50	°C
Textit	Maximum exit air temperature		68	°C
Tnon-op	Non-operating temperature range	-40	70	°C
Altitude1	Maximum operating altitude; 50°C inlet		3050	meters
Altitude2	Maximum operating altitude; 55°C inlet		900	meters
Acoustical Noise	A-weighted sound power, 25°C, 50% Load		49	dB

Table 14. Requirements for Non-Redundant Power Supply Configuration (High System Ambient)

13.1 HUMIDITY

Operating: To 85% relative humidity (non-condensing)

Non-Operating: To 95% relative humidity (non-condensing)

NOTE: 95% relative humidity is achieved with a dry bulb temperature of 55°C and a wet bulb temperature of 54°C.

13.2 ALTITUDE

Operating: To 3050 m (Maximum operating altitude 5000 meters and the Maximum operating temperature to 40°C.)

Non-operating: To 15200 m

13.3 SHOCK AND VIBRATION

13.3.1 RANDOM VIBRATION – OPERATING

Sample Size: For all product classes and categories, the minimum number of samples shall be 3 devices.

Test Method: The devices shall be tested per the methods described in IEC 60068-2-64, Environmental testing - Part 2: Test methods - Test Fh: Vibration, broad-band random (digital control) and guidance. Each device shall be tested in three axes for a minimum of 30 minutes per axis. The device shall be powered for the duration of the test at nominal input voltage and no load. For operating vibration testing, see [Figure 20](#).

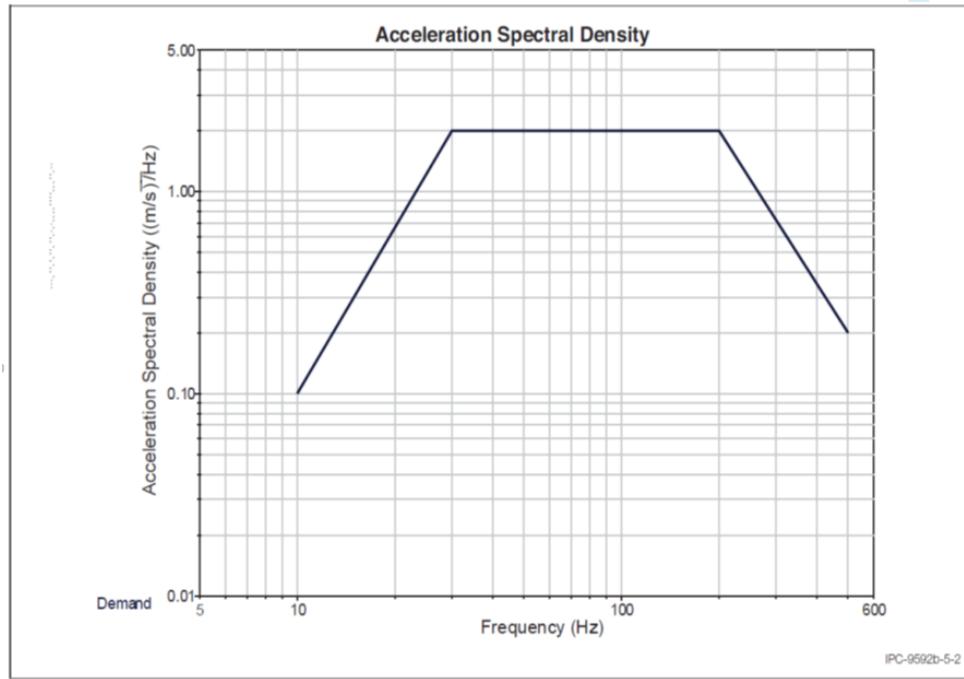


Figure 20. Class II PCDs Operating Vibration Test: Acceleration vs Frequency

The total acceleration for Class II PCDs is approximately 2.4 grms, see [Table 15](#).

Frequency Hz	Class I Acceleration Specification		Class II Acceleration Specification	
	(m/s ²) ² /Hz	G ² /Hz	(m/s ²) ² /Hz	G ² /Hz
10	0.022	0.000229	0.1	0.00046
30	0.20	0.0021	2	0.0052
200	0.20	0.0021	2	0.0052
500	0.0052	0.000054	0.2	0.0001
		Grms = 0.71	Grms = 2.40	

Table 15. Operation Vibration Profile Charts

Pass Criteria: Each power and signal output of each unit under test shall be monitored continuously during the test. Sampling at greater than 1 millisecond periods is not permitted. The units under test shall operate within specification during the entire test.

13.3.2 RANDOM VIBRATION - NON-OPERATING

Sample Size: For all product categories and product classes, the minimum number of samples shall be 3 devices packaged in their fully populated, bulk shipping package or individual packages of product.

Test Method: The devices shall be tested per the methods described in IEC 60068-2-64, Environmental testing –

Part 2: Test methods - Test Fh: Vibration, broad-band random (digital control) and guidance, with the acceleration spectral density curves provided in this document. The products are in the shipping packaging for this test. For non-operating vibration testing, see Table 5-11. Each shipping package shall be tested in three axes for a minimum of 30 minutes per axis.

The total acceleration for Class II PCDs is approximately 3.8Grms, see [Table 16](#).

Frequency Hz	Class I Acceleration Specification		Class II Acceleration Specification	
	(m/s ²) ² /Hz	G ² /Hz	(m/s ²) ² /Hz	G ² /Hz
5	1	0.01	5	0.0052
200	1	0.01	5	0.0052
500	0.03	0.003	0.3	0.003
Grms = 1.90			Grms = 3.80	

Table 16. Non-Operating Vibration Profile Charts

Pass Criteria: At the conclusion of all three axes of testing, the products shall be unpackaged and visually inspected for any signs of damage. Only minor cosmetic damage that does not affect form, fit or function is allowed. Bent connector pins, damaged switches, damaged handles, labels with impaired readability, or bent or deformed sheet metal are not allowed. All units shall also pass a functional test. There are no requirements on the condition of the shipping package.

13.3.3 SHOCK – OPERATING

Sample Size: For all product types and product classes, the minimum number of samples shall be three (3) devices.

Test Method: The devices shall be tested per the methods described in IEC 60068-2-27, Environmental Testing-Part 2.27 Test Ea and guidance: Shock. Each tested device shall be exposed to three shocks in each of three axes. The amplitude of each shock shall be no less than 30 g with a half sine wave shape and a duration of 11 mS.

Pass Criteria: Each power and signal output of each unit under test shall be monitored continuously during the test. Sampling at greater than 1 millisecond periods is not permitted. The units under test shall operate within specification during the entire test.

13.3.4 THERMAL SHOCK (SHIPPING)

Non-operating: -40°C to +70°C, 50 cycles, 30°C/min. ≥ transition time ≥ 15°C/min., duration of exposure to temperature extremes for each half cycle shall be 30 minutes.

14. RELIABILITY

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
MTBF Mean time between failure	T _A = 40°C, 75% load, according Telcordia SR-332, issue 3	250			kh

Comment: All components de-rating follow IPC9592B.

15. MECHANICAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Dimensions	Width		80		mm
	Height		40		mm
	Depth		195		mm
<i>m</i> Weight			1		kg

Tolerance unless otherwise stated: 0.5-30 mm: +/-0.3 mm; 30-120 mm: +/-0.4 mm; 120-400 mm: +/-0.5 mm.

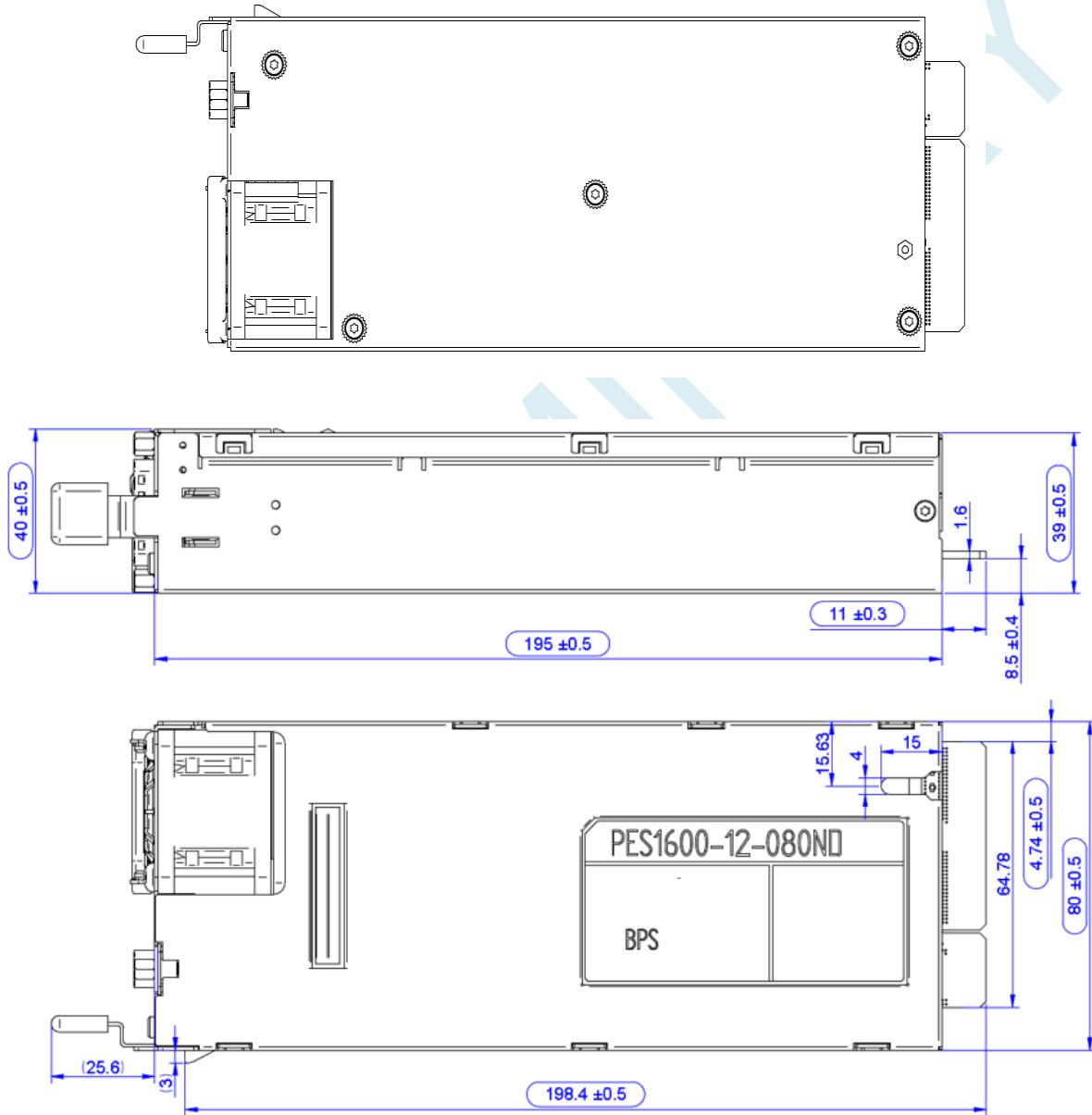


Figure 21. Top, bottom and side view

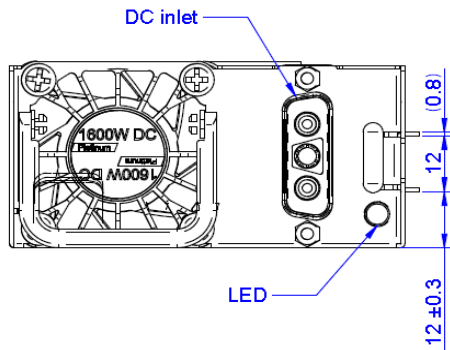


Figure 22. Front view

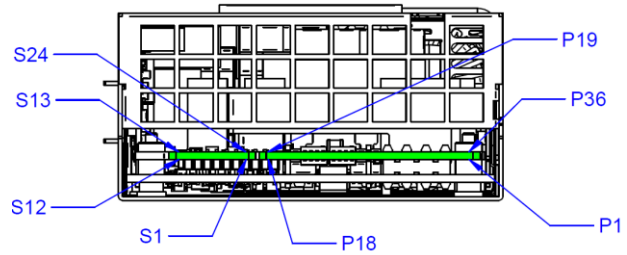


Figure 23. Rear view

16. CONNECTORS

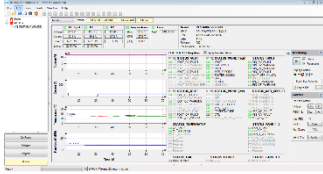
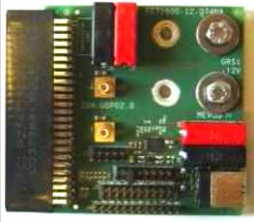
PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
DC inlet	D-SUB connector				
DC cord requirement	Wire size		8		AWG
Output connector	36 Power + 24signals Pins PCB card edge				
Mating output connector	Manufacturer : FCI Electronics Manufacturer P/N: 10130248-005LF BEL P/N: ZES.00678				

PIN	SIGNAL NAME	DESCRIPTION	Mating Sequence*
P1 ~ P10	GND	Power and signal ground (return)	1
P29 ~ P36	GND		
P11 ~ P18	V1	+12 VDC main output	2
P19 ~ P28	V1		
S1	A0	I ² C address selection input	1
S2	A1	I ² C address selection input	1
S3, S4	VSB	+12 V Standby positive output (as pins S3, S4)	1
S5	Hot_Standby	Hot standby Bus	1
S6	ISHARE	Analog current share bus	1
S7	VIN_OK_H	Input OK signal output, active-high	1
S8	PRESENT_L	Power supply seated, active-low	3
S9	A2	I ² C address selection input	1
S10 ~ S15	GND	Power and signal ground (return)	1
S16	PWOK_H	Power OK signal output, active-high	1
S17	V1_SENSE	Main output positive sense	1
S18	V1_SENSE_R	Main output negative sense	1
S19	SMB_ALERT_L	SMB Alert signal output, active-low	1
S20	PSON_L	Power supply on input, active-low	3
S21, S22	VSB	+12 V Standby positive output (as pins S3, S4)	1
S23	SCL	I ² C clock signal line	1
S24	SDA	I ² C data signal line	1

*1=First, 3=Last, given by different card edge finger pin lengths and mating connector pin arrangement.

Table 17. Output connector pin assignment

17. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	<p>I²C Utility Windows XP/Vista/7 compatible GUI to program, control and monitor PES1600-12-080ND Front-Ends (and other I²C units)</p>	<p>N/A</p>	<p>belfuse.com/power-solutions</p>
	<p>Evaluation Board Connector board to operate PES1600-12-080ND. Includes an on-board USB to I²C converter (use I²C Utility as desktop software).</p>	<p>YTM.00103</p>	<p>belfuse.com/power-solutions</p>

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PRELIMINARY

18. REVISION HISTORY

DATE	REVISION	SECTION	ISSUE	PREPARED BY	APPROVED BY
2017/05/15	001	/	First release	Baker Xu	Baojun Zeng
2017/06/16	002	2	Block Diagram update the output GND connect to PE.	Baker Xu	Baojun Zeng
2017/06/16	002	3	Change the maximum input voltage from -75V to -78V.	Baker Xu	Baojun Zeng
2017/06/16	002	4	1) Change the input normal operation voltage Vi max from -72V to -75V, also update the other sections. 2) Defined the max input current is 46A. 3) Clarify the turn-on and turn-off voltage for V1 and Vsb. 4) Defined the 10% load efficiency is 82%. 5) Defined the hold-up time for V1 and Vsb. 6) Add 4.5 DC line transient test from DC CRPS requirement.	Baker Xu	Baojun Zeng
2017/06/16	002	5	1) Change the V1 max rise time from 200ms to 70ms. 2) Change the V1 max capacitive loading from 10mF to 22mF.	Baker Xu	Baojun Zeng
2017/06/16	002	6.3	Correct the PSU name is PES1600-12-080ND.	Baker Xu	Baojun Zeng
2017/06/28	002	7	Monitoring some items should be TBD.	Baker Xu	Baojun Zeng
2017/06/28	002	8.5	Separate PWOK for each PSU design in system side.	Baker Xu	Baojun Zeng
2017/06/28	002	8.7	Update the T1 time to 1ms Min.	Baker Xu	Baojun Zeng
2017/06/28	002	8.8	Defined the hold-up time for V1 and Vsb.	Baker Xu	Baojun Zeng
2017/06/28	002	9.1	Update the Figure 14 for the A2 address.	Baker Xu	Baojun Zeng
2017/06/28	002	10	Temperature sensor some items should be TBD.	Baker Xu	Baojun Zeng
2017/06/28	002	11.1	Update the surge 1kV line to ground.	Baker Xu	Baojun Zeng
2017/06/28	002	12	1) Update CE - Low Voltage Directive 2014/35/EC. 2) Remove the CNS14336-1.	Baker Xu	Baojun Zeng
2017/06/28	002	13.3	Update the Shock and Vibration.	Baker Xu	Baojun Zeng
2017/07/04	003	4	Add the description for Inrush current limitation	Baker Xu	Baojun Zeng
2017/07/04	003	6	Add the OTP description refer to Table 17.	Baker Xu	Baojun Zeng
2017/07/04	003	8.8	Update the T _{PWOK_H_holdup} to 1.5ms MIN.	Baker Xu	Baojun Zeng
2017/08/02	003	8.5	Update the PWOK_H description to keep the same with AC version. 1) Add mechanical drawing in section 15. 2) Update DC inlet connector info and output connector mating sequence and make it same to PES1600-12-080NA mating sequence in section 16.	Baker Xu	Baojun Zeng
2017/08/08	003	15,16		Roby Chen	Andrew Li
2017/08/14	004	8.1, 8.7, 16	Rename all the VIN_GOOG_H to VIN_OK_H.	Baker Xu	Baojun Zeng
2017/09/05	004	0	Remove 80 plus "Platinum" efficiency since 80+ is not applicable for DC/DC PSU	Baker Xu	Baojun Zeng
2017/09/05	004	11.2, 13	Acoustical noise is not part of EMC.	Baker Xu	Andrew Li
2017/09/05	004	14	CMTBF, SR-332, issue 3 is the latest version	Baker Xu	Baojun Zeng
2017/09/05	004	11.1	The newest standard is EN 55024:2010/A1:2015, update the description.	Baker Xu	Baojun Zeng
2017/11/15	004	4, 4.4	Update the Turn-on / Turn-off V1 input voltage, update the hold-up time for Vsb, update the efficiency curve.	Baker Xu	Baojun Zeng
2017/11/15	004	7	Update the monitoring limit.	Baker Xu	Baojun Zeng
2017/11/15	004	8.8	Recover the T _{PWOK_H_holdup} to 1ms MIN, update the hold-up time for Vsb.	Baker Xu	Baojun Zeng
2017/11/15	004	9.6	Update Figure 17.	Baker Xu	Baojun Zeng
2017/11/15	004	10	Update Table 17 and Figure 19.	Baker Xu	Baojun Zeng
2017/11/17	004	8	In section 8.10, update LED wave length.	Roby Chen	Andrew Li
2017/11/17	004	13	In table 21, 22 and 23, update acoustic noise value.	Roby Chen	Andrew Li
2017/11/22	005	6.2/8.6	Mask SMB_ALERT_L signal for OTW event, update the related description for SMB_ALERT_L.	Baker Xu	Baojun Zeng
2018/01/18	005	4	Update the nominal input voltage from -48V _{nom} to -48V _{min} and -60V _{max} per safety required.	Baker Xu	Baojun Zeng
2018/01/18	005	4	Update the ramping up voltage from -31V _{max} to -32V _{max} and ramping down voltage from -29V _{max} to -30V _{max} for Vsb.	Baker Xu	Baojun Zeng
2018/01/18	005	10	Remove internal air temperature (outlet air temperature).	Baker Xu	Baojun Zeng
2018/01/19	005	/	Add PSU picture in page 1.	Roby Chen	Andrew Li
2018/02/26	006	7	Update the accuracy limit of monitoring about the lin/Pin/Ein.	Baker Xu	Baojun Zeng

PRELIMINARY

For more information on these products consult: tech.support@psbel.com

NUCLEAR AND MEDICAL APPLICATIONS - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.

TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.



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