VND830E-E

Double channel high-side driver

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VND830E-E	65 mΩ[1]	9.5 A[1]	36 V

1. Per each channel.

- Output current: 9.5 A
- CMOS compatible inputs
- On-state open-load detection
- Off-state open-load detection
- Output stuck to V_{CC} detection
- Open drain status outputs
- Undervoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Current and power limitation
- Very low standby current
- Protection against loss of ground and loss of V_{CC}
- Reverse battery protection
- Very low electromagnetic susceptibility
- Optimized electromagnetic emission

SO-16L
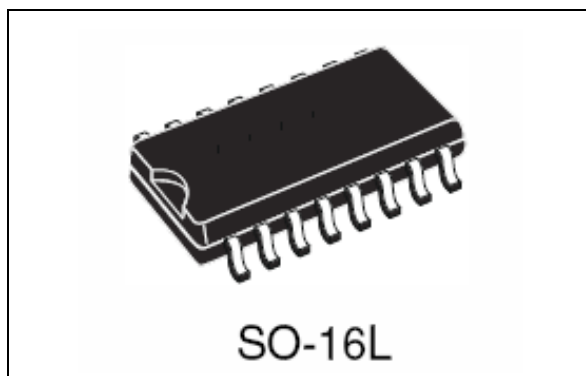
Description

The VND830E-E is a monolithic device made by using STMicroelectronics™ VIPower™ M0-3 technology. It is intended for driving resistive or inductive loads with one side connected to ground.

Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

The device detects open-load condition both in on-state and off-state. Output shorted to V_{CC} is detected in the off-state.

Output current limitation protects the device in overload condition. In case of long duration overload, the device limits the dissipated power to safe level up to thermal shutdown intervention.

Thermal shutdown with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

Table 1.   Device summary

Package	Order codes	
	Tube	Tape and reel
SO-16L	VND830E-E	VND830ETR-E

Contents

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1   Block diagram and pin description

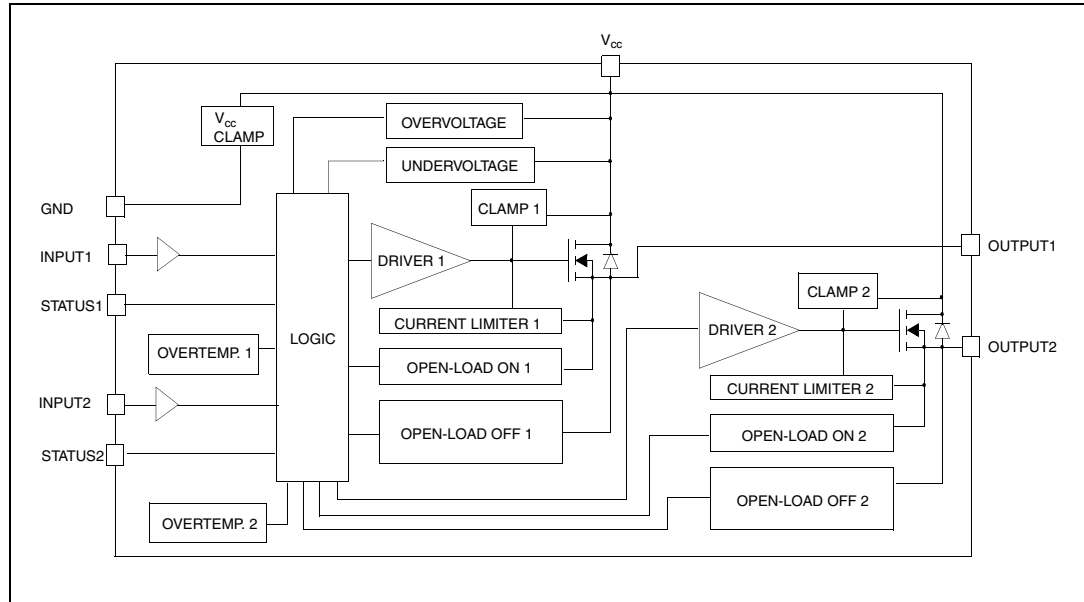**Figure 1.   Block diagram**

Figure 2.   Configuration diagram (top view)

Table 2.   Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground	-	X	-	Through 10 KΩ resistor

2   Electrical specifications

2.1   Absolute maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3.   Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
- V_{CC}	Reverse DC supply voltage	- 0.3	V
- I_{GND}	DC reverse ground pin current	- 200	mA
I_{OUT}	DC output current	Internally limited	A
- I_{OUT}	Reverse DC output current	- 6	A
I_{IN}	DC input current	+/- 10	mA
I_{STAT}	DC status current	+/- 10	mA
V_{ESD}	Electrostatic discharge (Human Body Model: R = 1.5 KΩ; C = 100 pF) - INPUT - STATUS - OUTPUT - V_{CC}	 4000 4000 5000 5000	 V V V V
E_{MAX}	Maximum switching energy (L = 0.45 mH; R_L = 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150 °C; I_L = 13.5 A)	57	mJ
P_{tot}	Power dissipation T_C = 25 °C	8.3	W
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	- 40 to 150	°C
T_{stg}	Storage temperature	- 55 to 150	°C

2.2 Thermal data

Table 4.   Thermal data (per island)

Symbol	Parameter	Value		Unit
$R_{thj\text{-}lead}$	Thermal resistance junction-lead	15		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	65[1]	47[2]	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5 cm^2 of Cu (at least 35 μm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

2. When mounted on a standard single-sided FR-4 board with 6 cm^2 of Cu (at least 35 μm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 36 V; -40 °C < T_j < 150 °C, unless otherwise stated.

(Per each channel)

Figure 3.   Current and voltage conventions
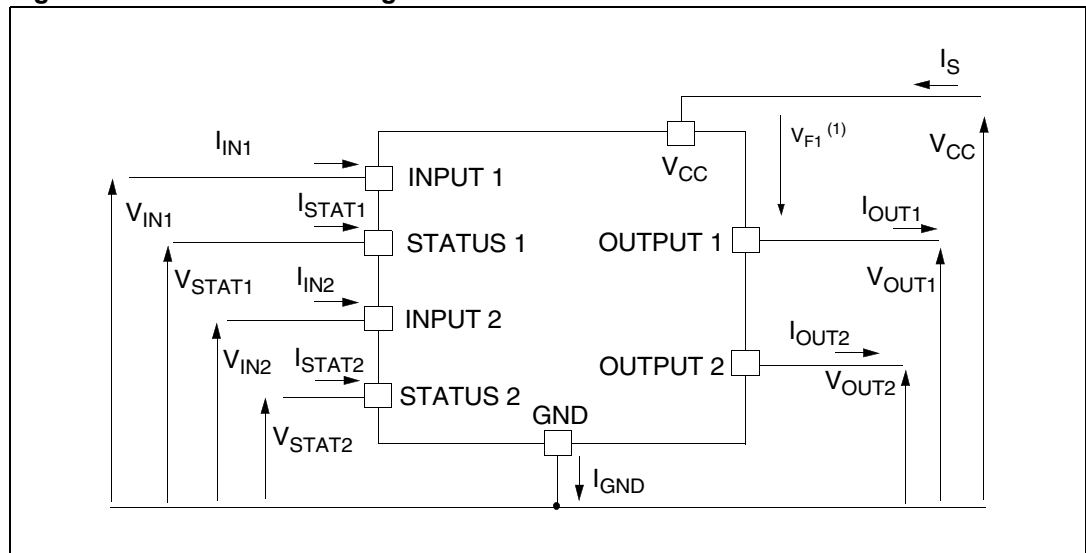
1. $V_{Fn} = V_{CCn} - V_{OUTn}$ during reverse battery condition.

Table 5.   Power outputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
V_{OV}	Overvoltage shutdown		36			V
R_{ON}	On-state resistance	I_{OUT} = 2 A; T_j = 25°C			65	mΩ
		I_{OUT} = 2 A; V_{CC} > 8 V			130	mΩ

Table 5. **Power outputs (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Supply current	Off-state; V_{CC} = 13 V; V_{IN} = V_{OUT} = 0 V		12	40	µA
		Off-state; V_{CC} = 13 V; V_{IN} = V_{OUT} = 0 V; T_j = 25°C		12	25	µA
		On-state; V_{CC} = 13 V; V_{IN} = 5 V; I_{OUT} = 0 A		5	7	mA
$I_{L(off1)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V	0		50	µA
$I_{L(off2)}$	Off-state output current	V_{IN} = 0 V; V_{OUT} = 3.5 V	-75		0	µA
$I_{L(off3)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125°C			5	µA
$I_{L(off4)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j =25°C			3	µA

Table 6. **Switching (V_{CC} = 13 V)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 6.5 Ω from V_{IN} rising edge to V_{OUT} = 1.3 V	-	50	-	µs
$t_{d(off)}$	Turn-off delay time	R_L = 6.5 Ω from V_{IN} falling edge to V_{OUT} = 11.7 V	-	50	-	µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 6.5 Ω from V_{OUT} = 1.3 V to V_{OUT} = 10.4 V	-	See *Figure 21*	-	V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 6.5 Ω from V_{OUT} = 11.7 V to V_{OUT} = 1.3 V	-	See *Figure 22*	-	V/µs

Table 7. **Logic input**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level				1.25	V
I_{IL}	Low level input current	V_{IN} = 1.25 V	1			µA
V_{IH}	Input high level		3.25			V
I_{IH}	High level input current	V_{IN} = 3.25 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA I_{IN} = -1 mA	6	6.8 -0.7	8	V V

Table 8. **V$_{CC}$ - output diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V$_F$	Forward on voltage	-I$_{OUT}$ = 1.2 A; T$_j$ = 150 °C	-	-	0.6	V

Table 9. **Status pin**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V$_{STAT}$	Status low output voltage	I$_{STAT}$ = 1.6 mA			0.5	V
I$_{LSTAT}$	Status leakage current	Normal operation; V$_{STAT}$ = 5 V			10	µA
C$_{STAT}$	Status pin Input capacitance	Normal operation; V$_{STAT}$ = 5 V			100	pF
V$_{SCL}$	Status clamp voltage	I$_{STAT}$ = 1 mA I$_{STAT}$ = - 1 mA	6	6.8 - 0.7	8	V V

Table 10. **Protections[1]**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T$_{TSD}$	Shutdown temperature		150	175	200	°C
T$_R$	Reset temperature		135			°C
T$_{hyst}$	Thermal hysteresis		7	15		°C
t$_{SDL}$	Status delay in overload conditions	T$_j$ > T$_{TSD}$			20	µs
I$_{lim}$	Current limitation	V$_{CC}$ = 13 V 5.5 V < V$_{CC}$ < 36 V	9.5	13.5	18 18	A A
V$_{demag}$	Turn-off output clamp voltage	I$_{OUT}$ = 2 A; L = 6 mH	V$_{CC}$-41	V$_{CC}$-48	V$_{CC}$-55	V

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 11. **Open-load detection**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I$_{OL}$	Open-load on-state detection threshold	V$_{IN}$ = 5 V	50	115	200	mA
t$_{DOL(on)}$	Open-load on-state detection delay	I$_{OUT}$ = 0 A			200	µs
V$_{OL}$	Open-load off-state voltage detection threshold	V$_{IN}$ = 0 V	1.5	2.9	3.5	V
t$_{DOL(off)}$	Open-load detection delay at turn-off				1000	µs

Figure 4.   Status timings
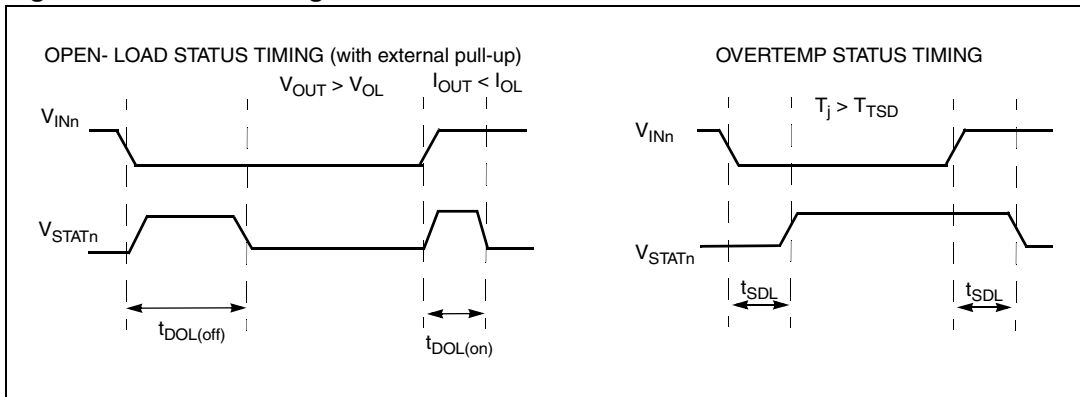
Figure 5.   Switching time waveforms
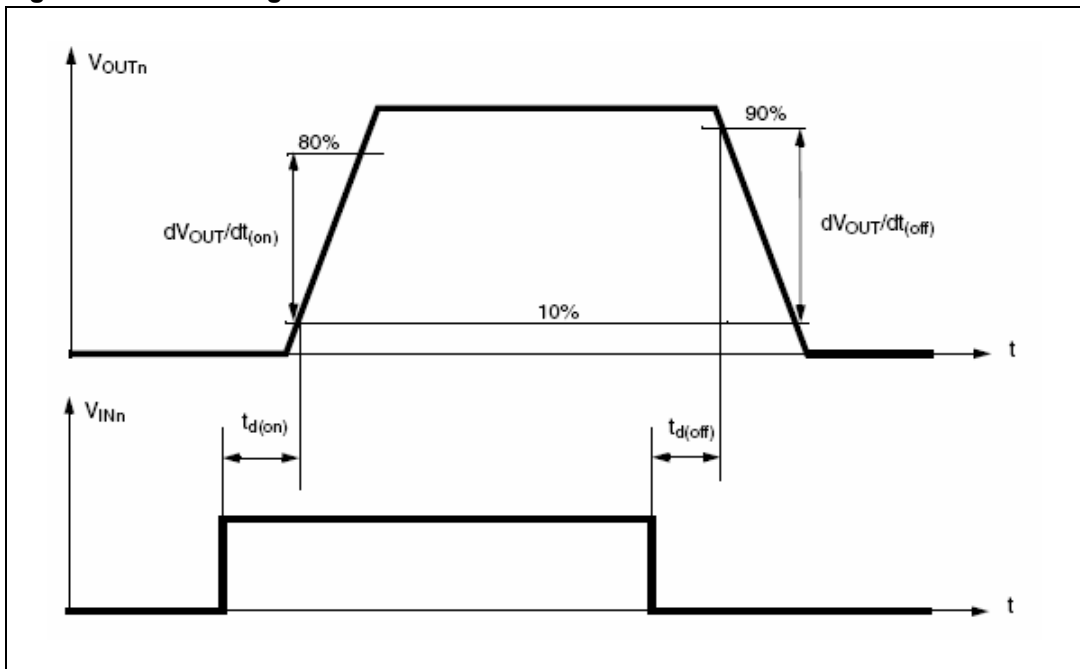
Table 12.   Truth table

Conditions	Input$_n$	Output$_n$	Status$_n$
Normal operation	L H	L H	H H
Current limitation	L H H	L X X	H ($T_j < T_{TSD}$) H ($T_j > T_{TSD}$) L
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X

Table 12.   Truth table (continued)

Conditions	Input$_n$	Output$_n$	Status$_n$
Overvoltage	L H	L L	H H
Output voltage > V$_{OLn}$	L H	H H	L H
Output current < I$_{OLn}$	L H	L H	H L

Table 13.   Electrical transient requirements on V$_{CC}$ pin (part 1)

ISO T/R 7637/1 test pulse	Test levels				
	I	II	III	IV	Delays and impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms, 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms, 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs, 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs, 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

Table 14.   Electrical transient requirements on V$_{CC}$ pin (part 2)

ISO T/R 7637/1 test pulse	Test levels results			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Table 15.   Electrical transient requirements on V$_{CC}$ pin (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 6.   Waveforms
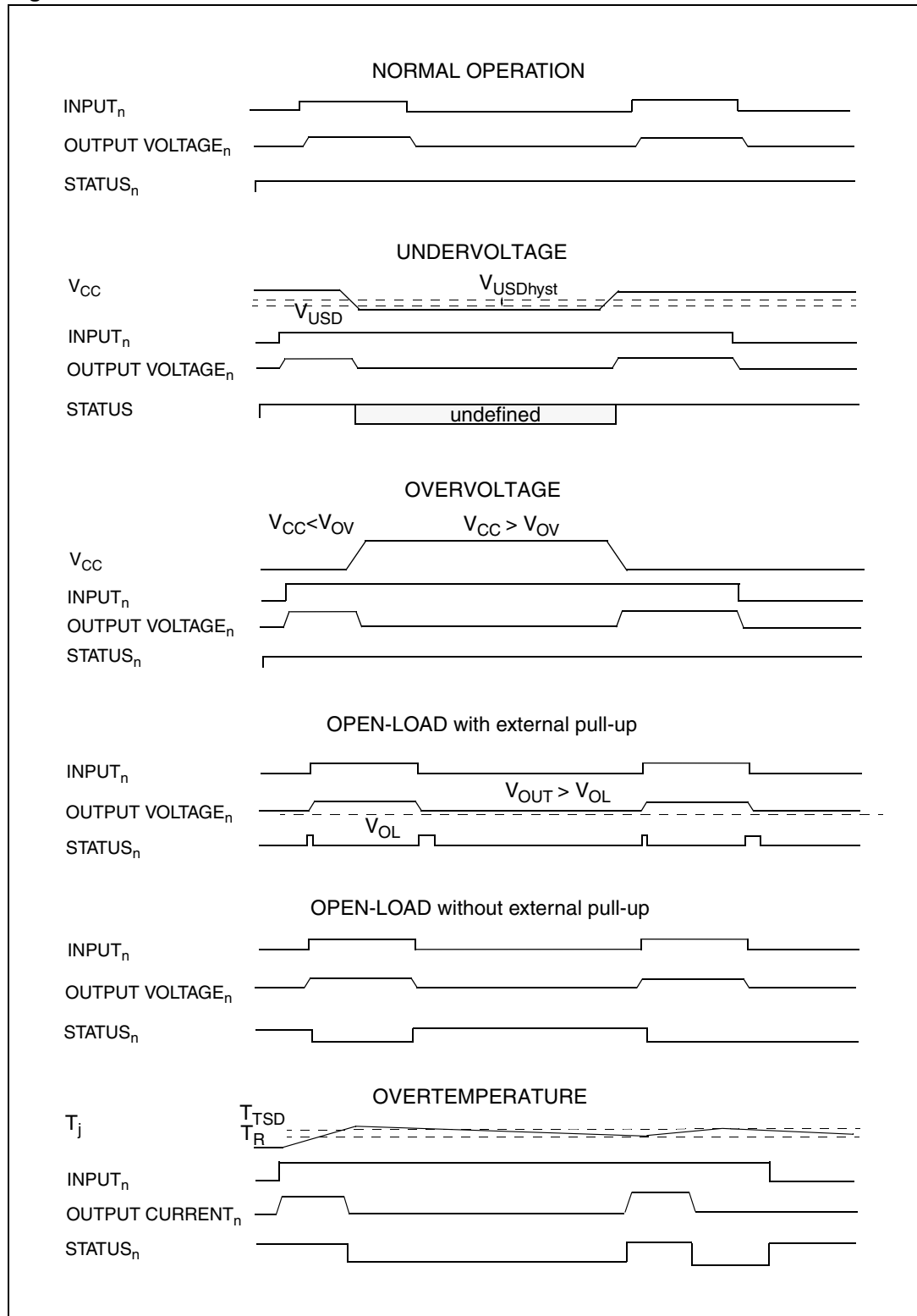
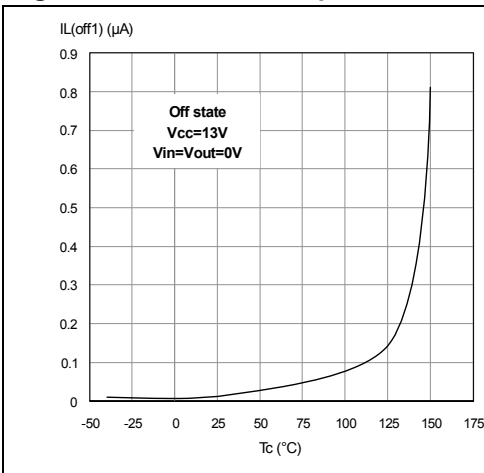## 2.4 Electrical characteristics curves

Figure 7. **Off-state output current**
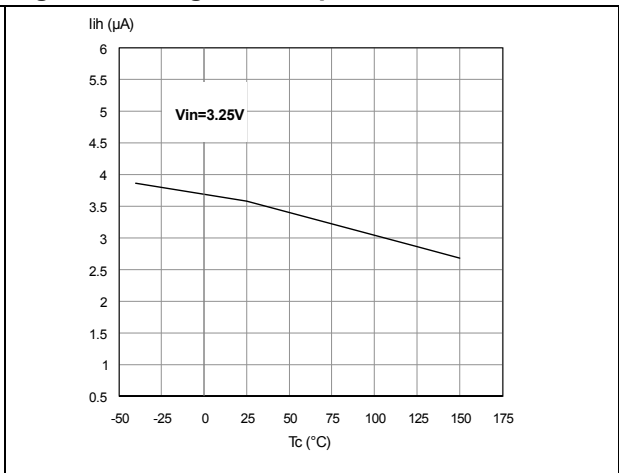

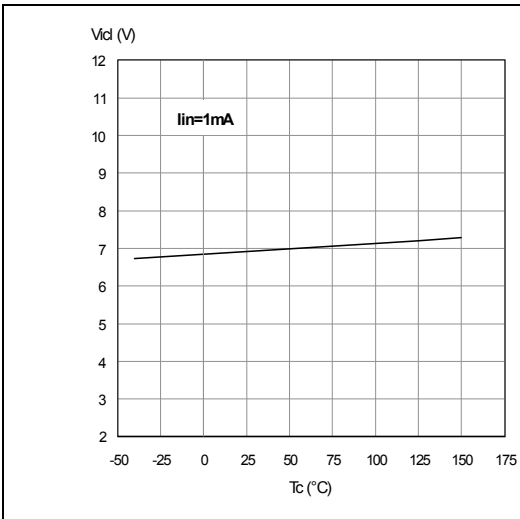**Figure 8.** **High level input current**

Figure 9. **Input clamp voltage**

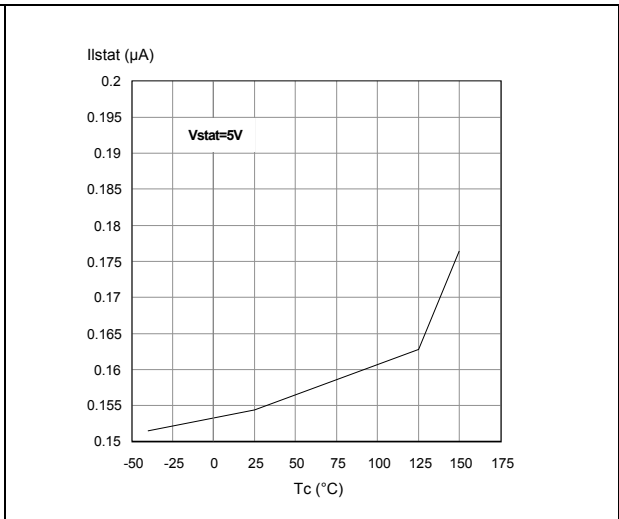**Figure 10.** **Status leakage current**

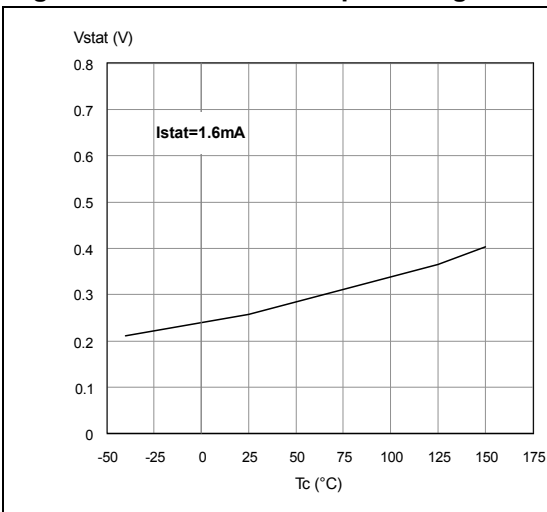**Figure 11.** **Status low output voltage**
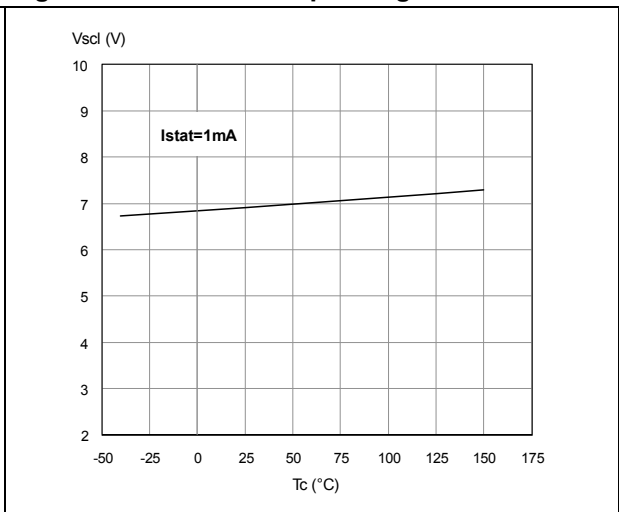

Figure 12. **Status clamp voltage**

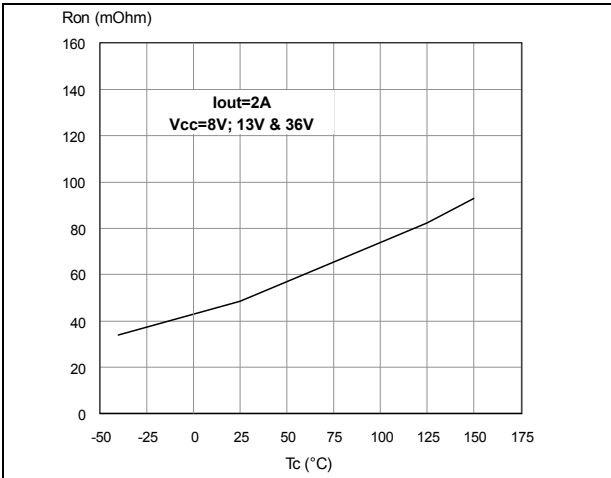**Figure 13.   On-state resistance vs T_case**

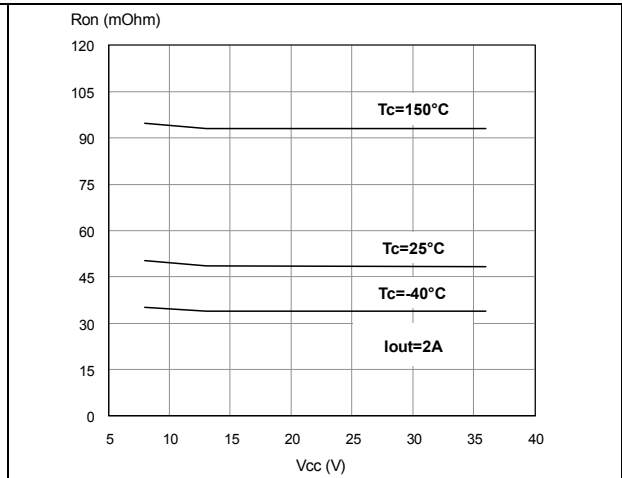**Figure 14.   On-state resistance vs V_CC**

Figure 15.   Open-load on-state detection threshold
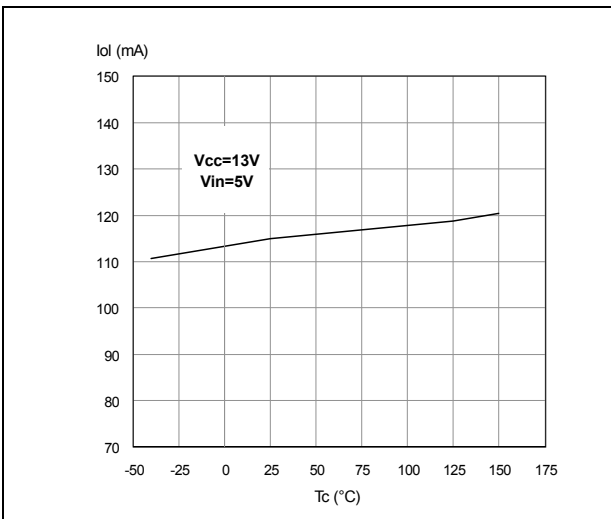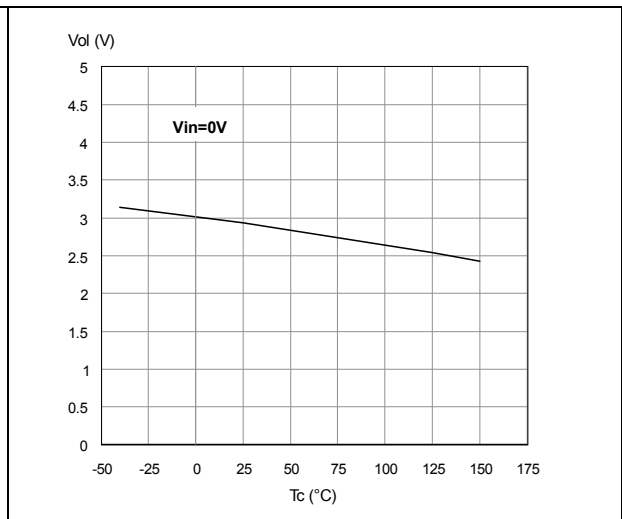

Figure 16.   Open-load off-state detection threshold

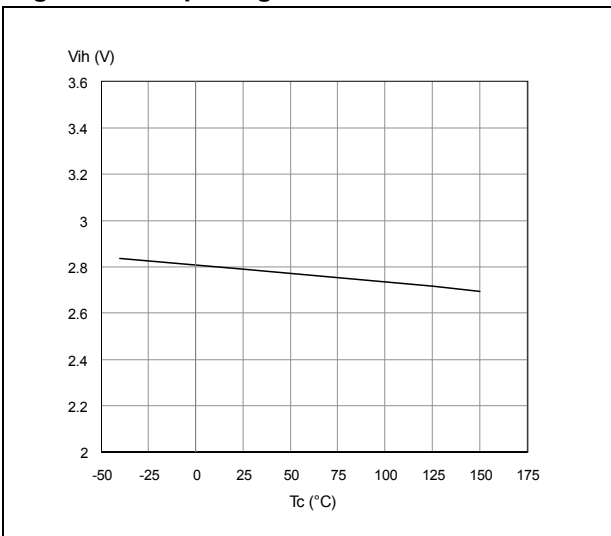**Figure 17.   Input high level**

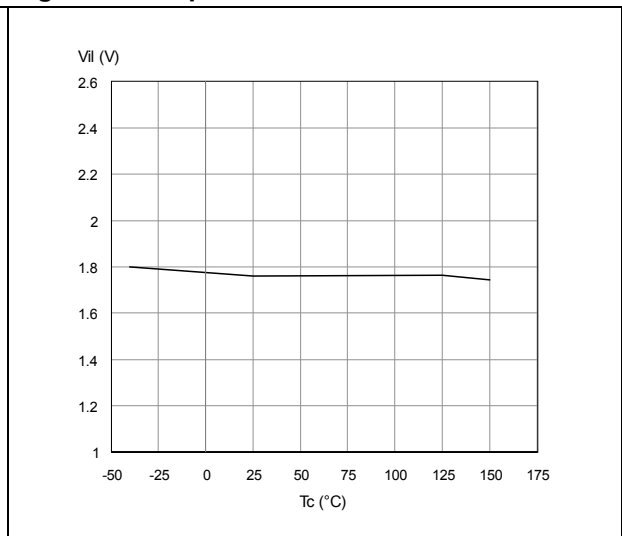
Figure 18.   Input low level
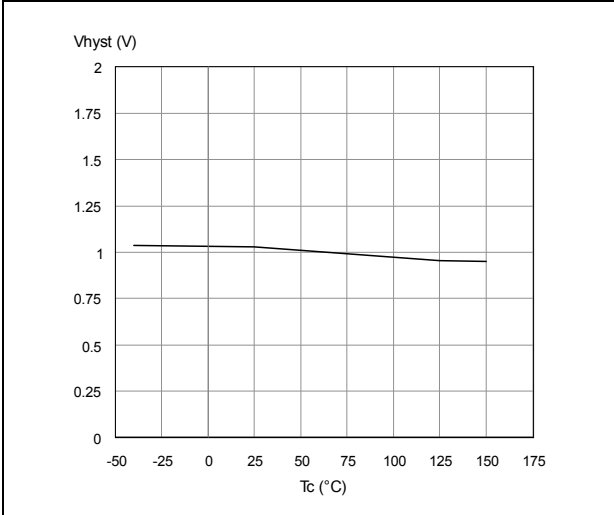
Figure 19. Input hysteresis voltage

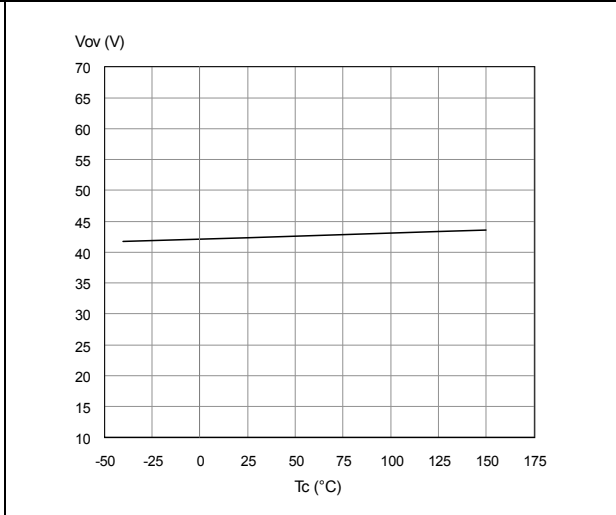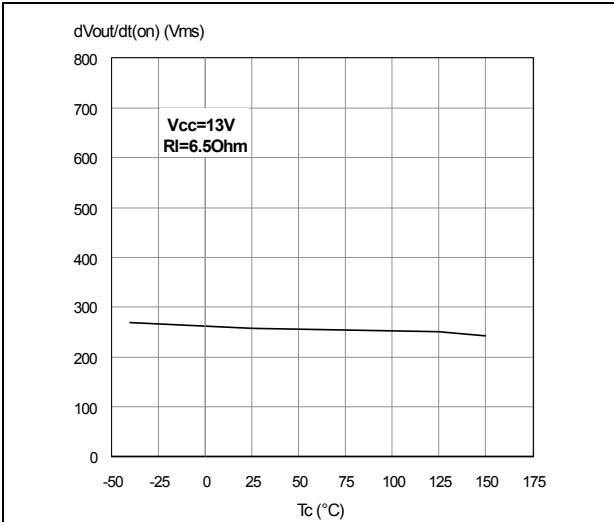**Figure 20. Overvoltage shutdown**

Figure 21. Turn-on voltage slope
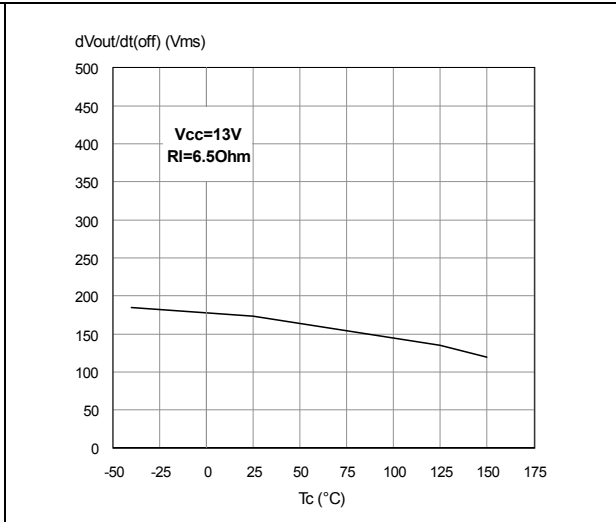

Figure 22. Turn-off voltage slope

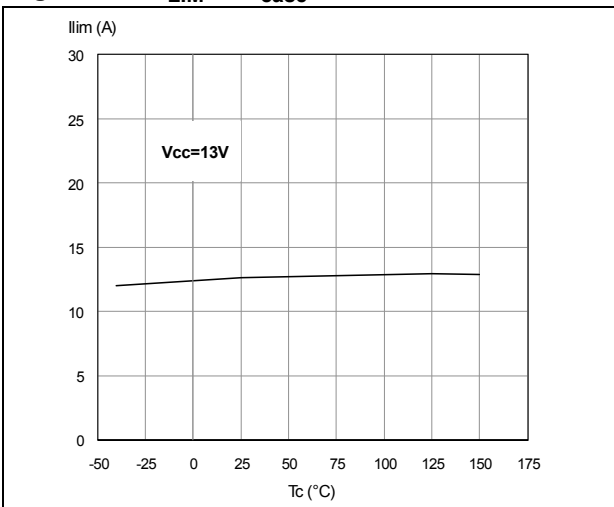**Figure 23. I_{LIM} vs T_{case}**

Figure 24. Undervoltage shutdown
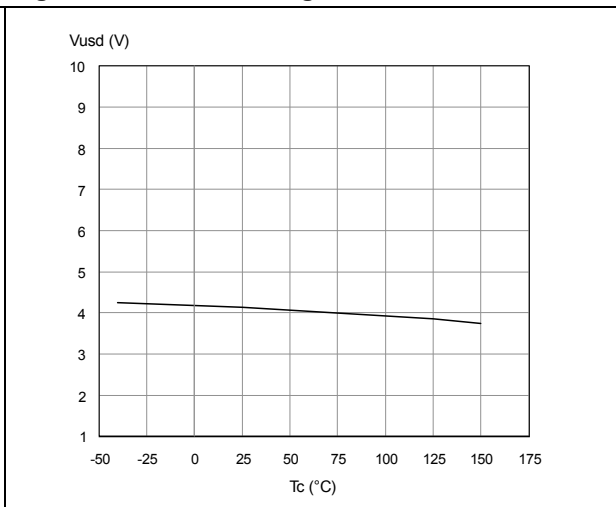
3 Application information

Figure 25. Application schematic
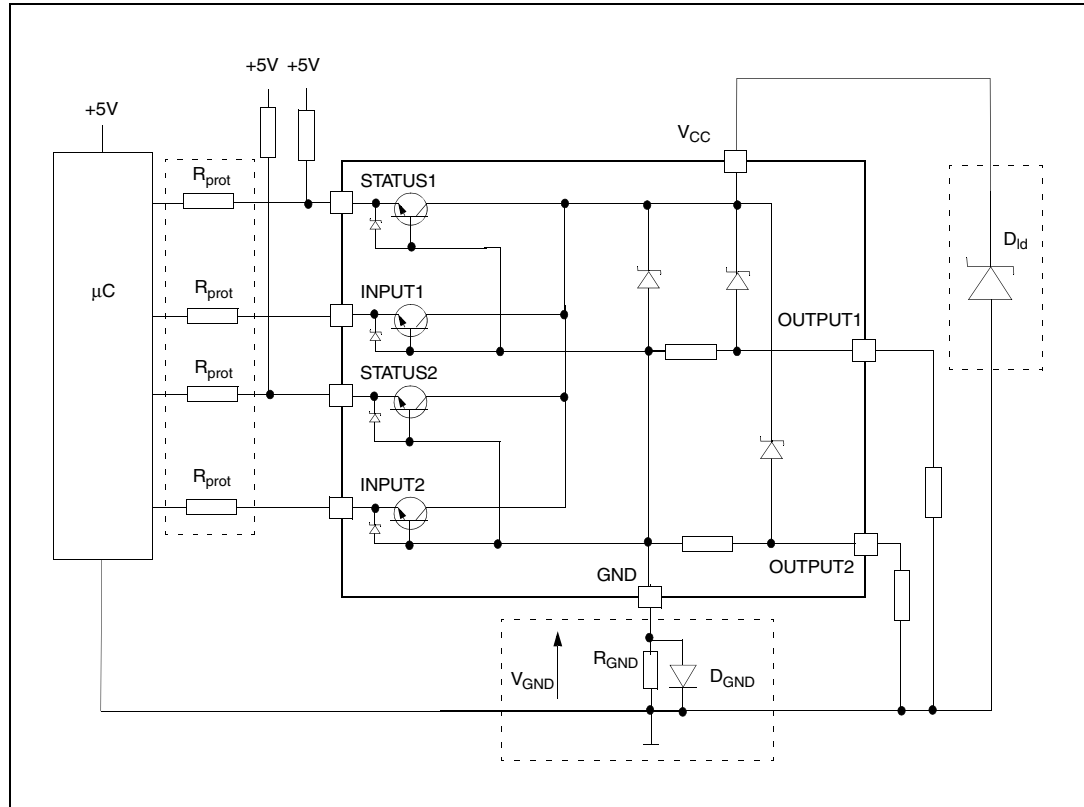
3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: a resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following shows how to dimension the R_{GND} resistor:

1. $R_{GND} \leq 600$ mV / ($I_{S(on)max}$)
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$ during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not common with the device ground, then the R_{GND} produces a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high-side drivers sharing the same R_{GND}.

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using *Section 3.1.2* described below.

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1 kΩ) should be inserted in parallel to D_{GND} if the device is driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network produce a shift (~600 mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating. Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} maximum DC rating. The same applies if the device is subjected to transients on the V_{CC} line that are greater than those shown in *Table 13*.

3.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins are pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os:

- V_{CCpeak} / $I_{latchup}$ ≤ R_{prot} ≤ ($V_{OHµC}$ - V_{IH} - V_{GND}) / I_{IHmax}

Example

For the following conditions:

V_{CCpeak} = -100 V

$I_{latchup}$ ≥ 20 mA

$V_{OHµC}$ ≥ 4.5 V

5 kΩ ≤ R_{prot} ≤ 65 kΩ.

The recommended values are:

R_{prot} = 10 kΩ

3.4   Open-load detection in off-state

Off-state open-load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5 V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

1.   No false open-load indication when load is connected: in this case it needs to avoid V_{OUT} to be higher than V_{Olmin}; this results in the following condition
      $V_{OUT} = (V_{PU} / (R_L + R_{PU}))R_L < V_{Olmin}$.

2.   No misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax}; this results in the following condition $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$.

Because $I_{s(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.
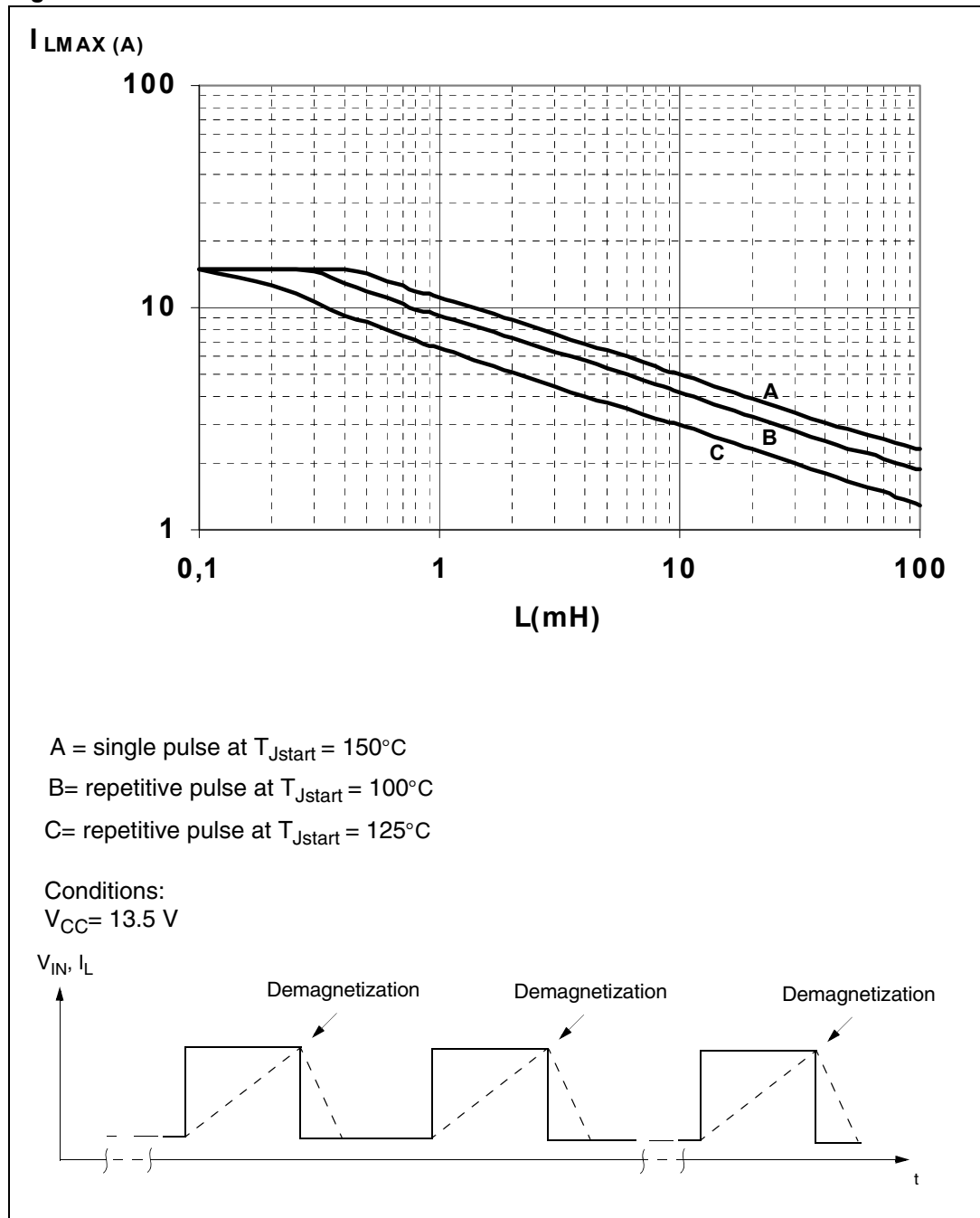
The values of V_{OLmin}, V_{OLmax} and $I_{L(off2)}$ are available in *Chapter 2: Electrical specifications*.

Figure 26.   Open-load detection in off-state
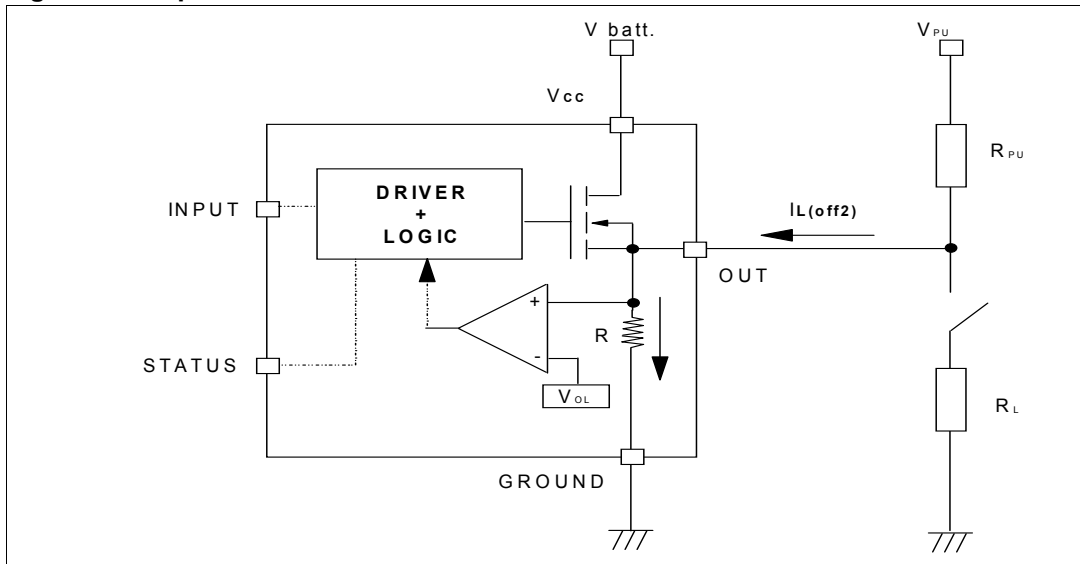
3.5 Maximum demagnetization energy

Figure 27. Maximum turn-off current versus load inductance

A = single pulse at T_{Jstart} = 150°C

B = repetitive pulse at T_{Jstart} = 100°C

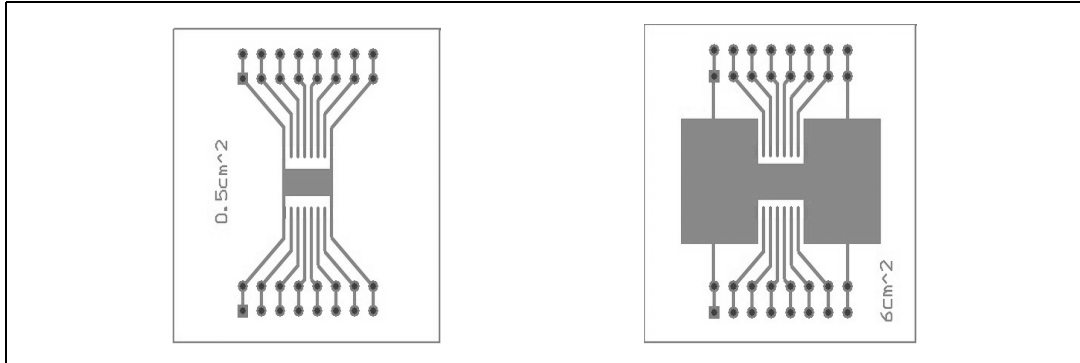C = repetitive pulse at T_{Jstart} = 125°C

Conditions:
V_{CC} = 13.5 V

Note: *Values are generated with RL = 0 Ω.*

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

4 Package and PCB thermal data

4.1 SO-16L thermal data

Figure 28. SO-16L PC board[1]

1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 41 mm x 48 mm, PCB thickness = 2 mm, Cu thickness = 35 µm, Copper areas: 0.5 cm^2, 6 cm^2).

Figure 29. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition
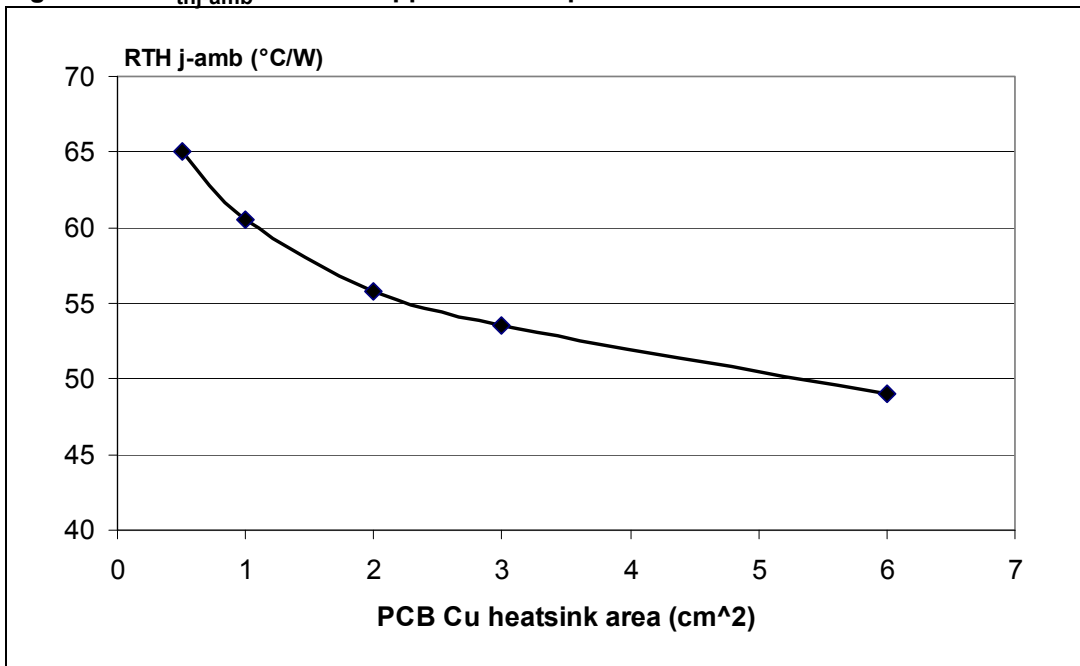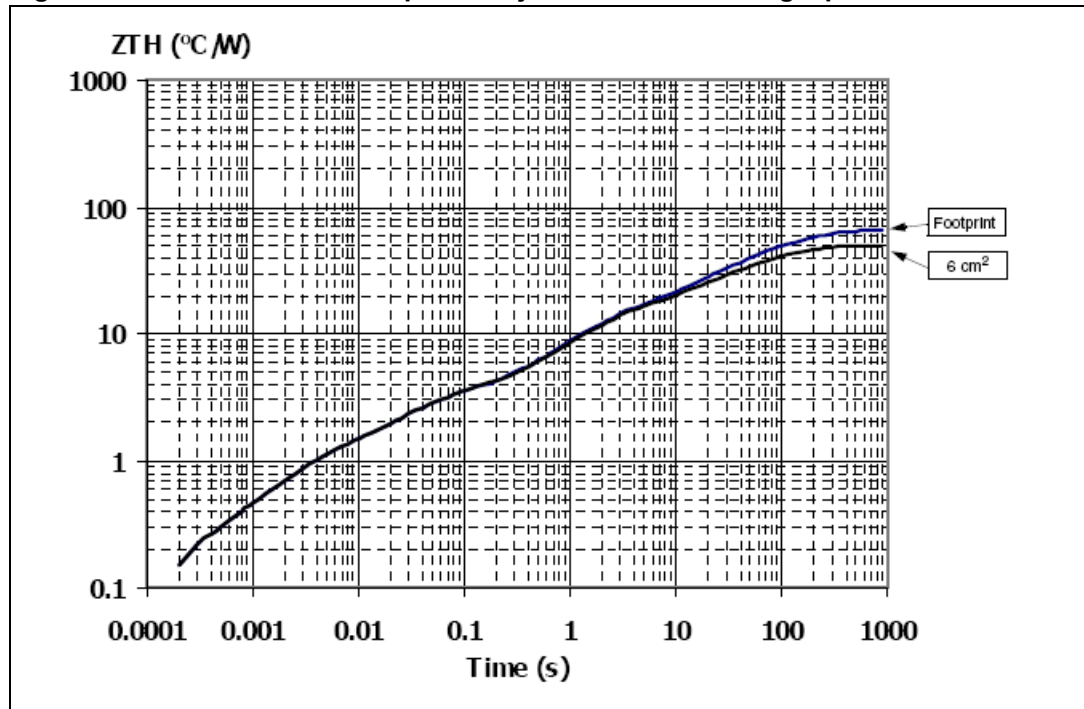
Figure 30.   SO-16 L thermal impedance junction ambient single pulse

Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\quad \delta = t_p / T$

Figure 31.   Thermal fitting model of a quad channel HSD in SO-16L
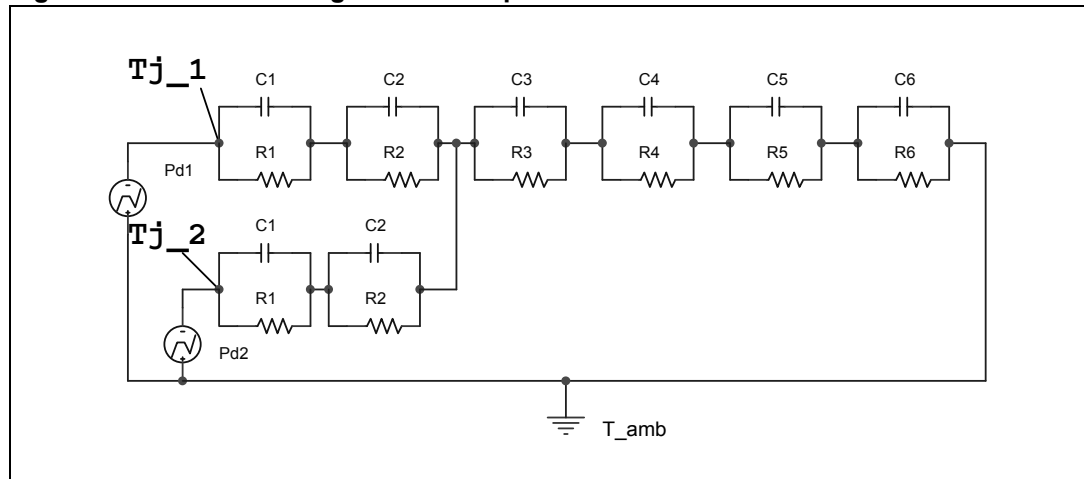
Table 16. **Thermal parameters**

Area/ island (cm^2)	Footprint	6
R1 (°C/W)	0.15	
R2 (°C/W)	0.7	
R3 (°C/W)	2	
R4 (°C/W)	10	
R5 (°C/W)	15	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0005	
C2 (W.s/°C)	0.003	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.15	
C5 (W.s/°C)	1.5	
C6 (W.s/°C)	3	5

5   Package and packing information

5.1   ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 32.   SO-16L package dimensions
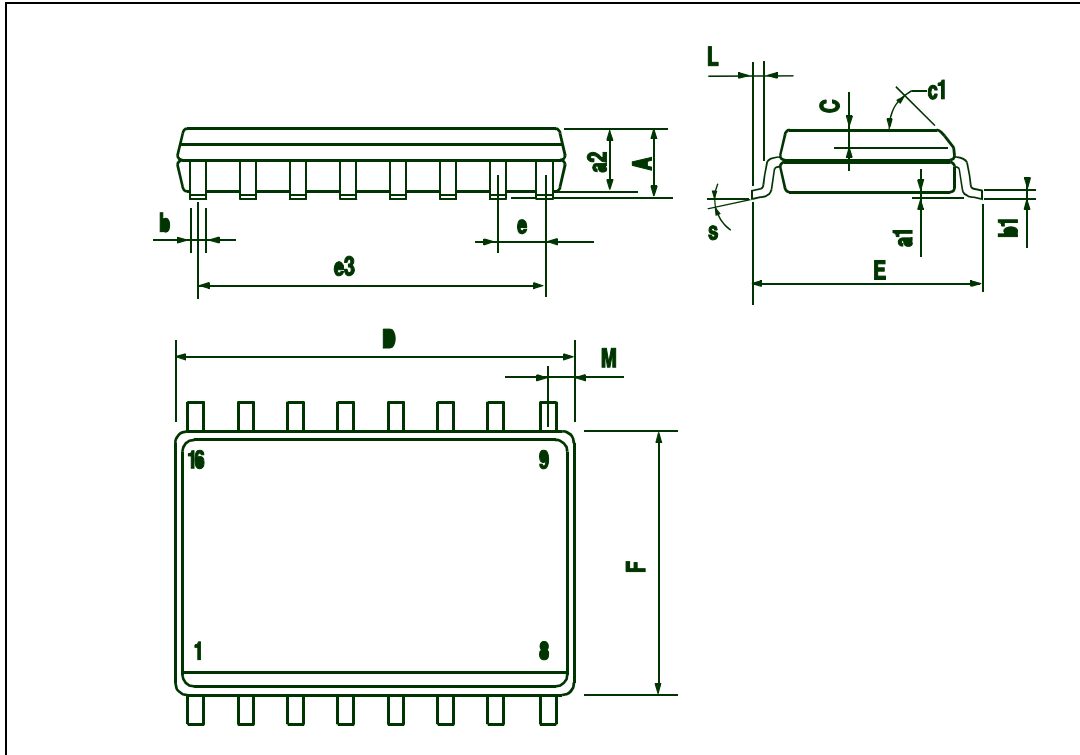
Table 17.   SO-16L mechanical data

DIM.	mm.		
	Min.	**Typ.**	**Max.**
A			2.65
a1	0.1		0.2
a2			2.45
b	0.35		0.49
b1	0.23		0.32
C		0.5	
c1	45° (typ.)		
D	10.1		10.5
E	10.0		10.65
e		1.27	
e3		8.89	
F	7.4		7.6
L	0.5		1.27
M			0.75
S	8° (max.)		

6 Revision history

Table 18.   Document revision history

Date	Revision	Changes
03-May-2010	1	Initial release.
19-Sep-2013	2	Updated Disclaimer

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