P-Channel Enhancement-Mode Vertical DMOS FET

Features

- High input impedance
- Low threshold (-2.4V max.)
- Low input capacitance (110pF max.)
- Fast switching speeds
- Low on-resistance
- Low input and output leakage
- Free from secondary breakdown

Applications

- Logic level interfaces - ideal for TTL and CMOS
- Battery operated systems
- Photo voltaic devices
- Analog switches
- General purpose line drivers
- Telecom switches

General Description

The Supertex TP5322 is a low threshold enhancement-mode (normally-off) transistor utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Part Number	Package Option	Packing
TP5322K1-G	TO-236AB (SOT-23)	3000/Reel
TP5322N8-G	3-Lead TO-92	2000/Reel

-G denotes a lead (Pb)-free / RoHS compliant package.
Contact factory for Wafer / Die availablity.
Devices in Wafer / Die form are lead (Pb)-free / RoHS compliant.

Product Summary

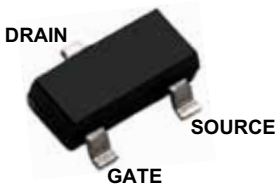
BV_{DSS}/BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)
-220V	12Ω	-700mA	-2.4V

Absolute Maximum Ratings

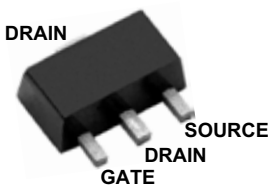
Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



TO-236AB (SOT-23)



TO-243AA (SOT-89)

Typical Thermal Resistance

Package	θ_{ja}
TO-236AB (SOT-23)	203°C/W
TO-243AA (SOT-89)	133°C/W

Product Marking

P3CW

W = Code for week sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-236AB (SOT-23)

TP3CW

W = Code for week sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-243AA (SOT-89)

Thermal Characteristics

Package	I_D (continuous)†	I_D (pulsed)	Power Dissipation @T_A = 25°C	I_{DR} †	I_{DRM}
TO-236AB (SOT-23)	-120mA	-700mA	0.36W	-120mA	-700mA
TO-243AA (SOT-89)	-260mA	-0.90mA	1.6W‡	-260mA	-0.90mA

Notes:

† I_D *(continuous) is limited by max rated* T_j.

‡ *Mounted on FR4 board, 25mm x 25mm x 1.57mm.*

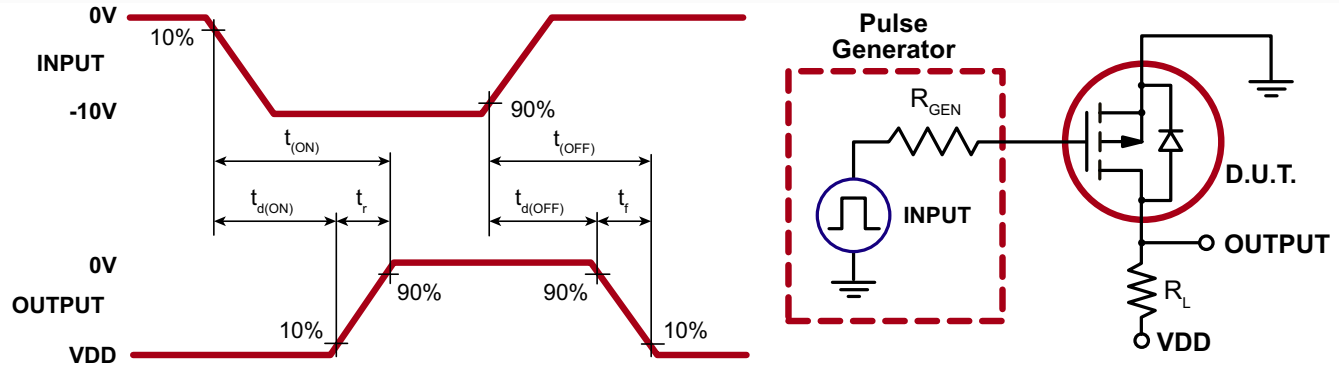
Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-220	-	-	V	V_{GS} = 0V, I_D = -2.0mA
$V_{GS(TH)}$	Gate threshold voltage	-1.0	-	-2.4	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(TH)}$	Change in $V_{GS(TH)}$ with temperature	-	-	4.5	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate body leakage current	-	-	-100	nA	V_{GS} = ±20V, V_{DS} = 0V
$I_{D(SS)}$	Zero gate voltage drain current	-	-	-10	µA	V_{DS} = Max rating, V_{GS} = 0V
		-	-	-1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	-0.7	-0.95	-	A	V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	10	15	Ω	V_{GS} = -4.5V, I_D = -100mA
			8.0	12		V_{GS} = -10V, I_D = -200mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.7	%/°C	V_{GS} = -10V, I_D = -200mA
G_{FS}	Forward transconductance	100	250	-	mmho	V_{DS} = -25V, I_D = -200mA
C_{ISS}	Input capacitance	-		110	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-		45		
C_{RSS}	Reverse transfer capacitance	-		20		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	V_{DD} = -25V, I_D = -700mA, R_{GEN} = 25Ω,
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	20		
t_f	Fall time	-	-	15		
V_{SD}	Diode forward voltage drop	-	-	-1.8	V	V_{GS} = 0V, I_{SD} = -500mA
t_{rr}	Reverse recovery time	-	300	-	ns	V_{GS} = 0V, I_{SD} = -500mA

Notes:

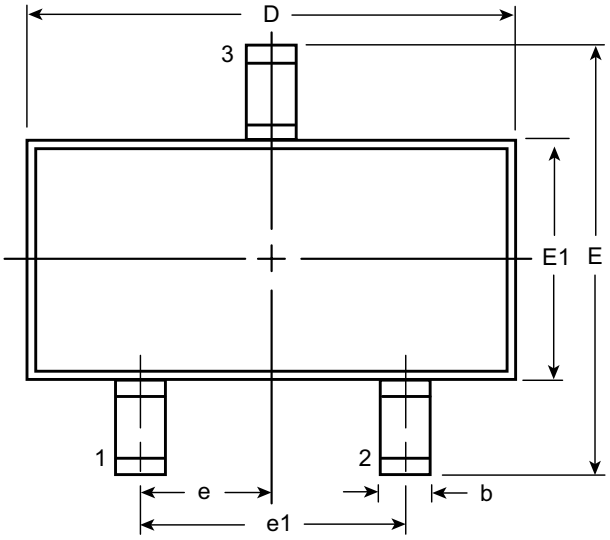
1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

Switching Waveforms and Test Circuit

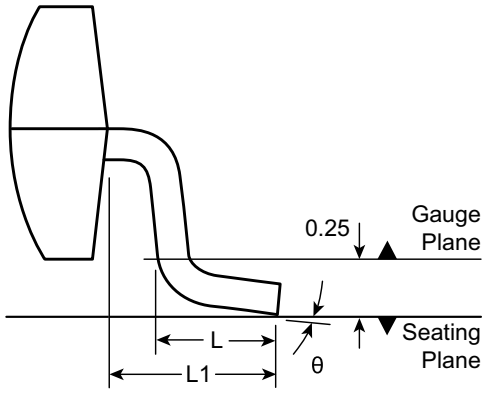


3-Lead TO-236AB (SOT-23) Package Outline (K1)

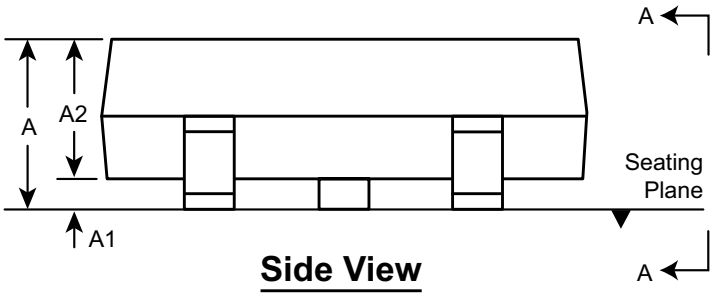
2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



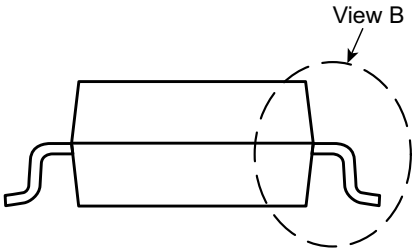
Top View



View B



Side View

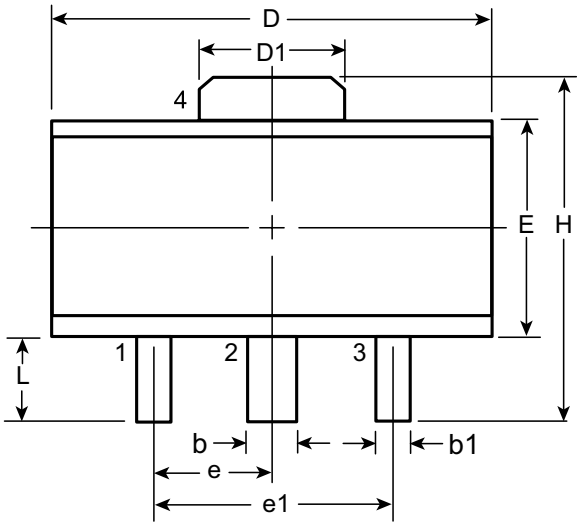


View A - A

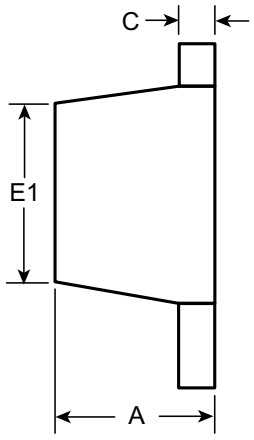
Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	θ
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20†	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc.#: *DSPD-3TO236ABK1, Version C041309.*

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Top View



Side View

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00†	1.50 BSC	3.00 BSC	3.94	0.73†
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.
† This dimension differs from the JEDEC drawing
Drawings not to scale.
***Supertex Doc. #:** DSPD-3TO243AAN8, Version F111010.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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