Boost 1channel white LED driver For large LCDs

BD9285F

●General Description

BD9285F is a high efficiency driver for white LEDs and designed for large LCDs. This IC is built-in a boost DCDC converters that employ an array of LEDs as the light source. BD9285F has some protect function against fault conditions, such as the over-voltage protection (OVP), the over current limit protection of DCDC (OCP), LED over current protection (LEDOCP), the open detection of LED string. Therefore BD9285F is available for the fail-safe design over a wide range output voltage.

●Features

- Current mode DCDC converter
- Vout discharge circuit as shutdown
- LED protection circuit (OPEN protection, LED OCP protection)
- LED protect detection as small PWM dimming signal
- Over-voltage protection (OVP) and low-voltage protection (SCP: short circuit protection) for the output voltage Vout
- Adjustable soft start time constant
- The wide range of analog dimming 0.2V-3.5V
- The built-in transformation circuit from pulse to DC
- 2 PWM dimming signal
- The UVLO detection for the input voltage of the power stage
- FAIL logic output

●Applications

- TV, PC display and other LCD backlight system.

●Key Specifications

- Input voltage range: 9.0V to 18.0V
- DCDC oscillation frequency: 150kHz (RT=100kΩ)
- Active current consumption: 1.2mA(Typ.)
- Operating temperature range: -40℃ to +85℃

●Package(s)

	W(Typ.) x D(Typ.) x H(Max.)
SOP18	11.20mm x 7.80mm x 2.01mm
	Pin pitch 1.27mm

Figure 1. SOP18

●Typical Application Circuit(s)

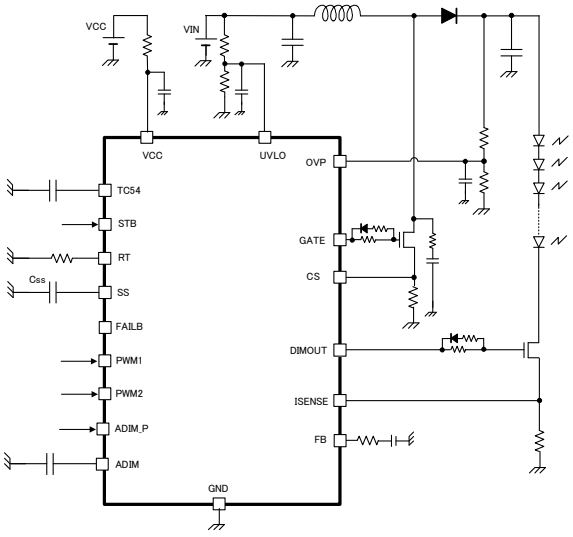


Figure 2. Typical application circuit

●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Input voltage	Vccmax	20	V
STB pin voltage	STB	20	V
OVP, UVLO, SS, RT, ISENSE, FB, CS, TC54 pin voltage	OVP, UVLO, SS, RT, ISENSE, FB, CS, TC54	7	V
PWM1, PWM2, FAILB, ADIM, ADIM_P pin voltage	PWM1, PWM2, FAILB, ADIM, ADIM_P	20	V
DIMOUT, GATE pin voltage	DIMOUT, GATE	VCC	V
Power Dissipation	Pd	687 (*1)	mW
Operating Temperature Range	Topr	-40 to +85	℃
Junction Temperature	Tjmax	150	℃
Storage Temperature Range	Tstg	-55 to +150	℃

*1 Pd derated at 5.5 mW/℃ for temperature above Ta=25℃,
mounted on 70mm × 70mm × 1.6mm 1 layer glass-epoxy PCB.

●Operation range

Parameter	Symbol	Range	Unit
VCC Power source voltage	VCC	9.0 to 18.0	V
DC/DC oscillation frequency	fsw	50 to 800	kHz
The effective range of ADIM signal	VADIM	0.2 to 3.5	V
PWM input frequency range	FPWM	100 to 100k	Hz

●Pin Configuration

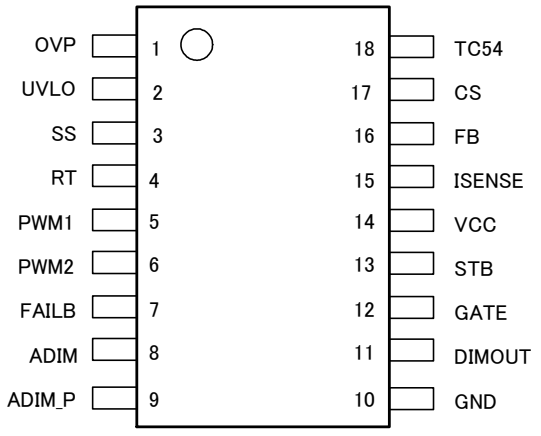


Figure 3-1. Pin configuration

●Package dimension, marking diagram

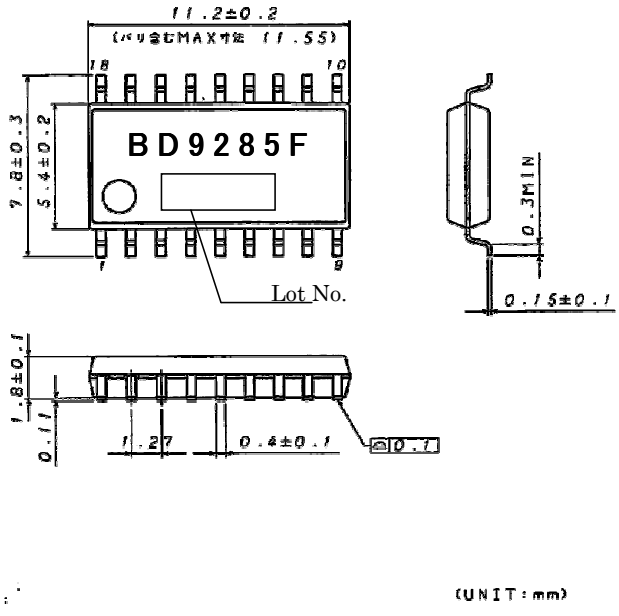


Figure 3-2. Package dimension

●1.1 Electrical character (Unless otherwise specified Ta=25℃, VCC=12V)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
【Total current consumption】						
Circuit current	Icc	－	1.2	1.8	mA	VSTB=3V, PWM1=PWM2=0V
Standby current	IST	－	0	3	μA	VSTB=0V
【UVLO block】						
Operation voltage（VCC）	VUVLO_VCC	6.5	7.5	8.5	V	VCC=SWEEP UP
Hysteresis Voltage（VCC）	VUHYS_VCC	150	300	600	mV	VCC=SWEEP DOWN
UVLO release voltage	VUVLO	2.88	3.00	3.12	V	VUVLO=SWEEP UP
UVLO hysteresis voltage	VUHYS	160	200	240	mV	VUVLO=SWEEP DOWN
UVLO pin leak current	UVLO_LK	-2	0	2	μA	VUVLO=4V
【DC/DC block】						
ISENSE threshold voltage 1	VLED1	1.47	1.50	1.53	V	VADIM=1.5V
ISENSE threshold voltage 2	VLED2	3.33	3.50	3.67	V	VADIM=5.0V (as mask analog dimming)
ISENSE threshold voltage 3	VLED3	-2	-	+2	%	VADIM=0.7V
Oscillation frequency	FCT	142.5	150	157. 5	KHz	RT=100kohm
GATE pin MAX DUTY output	NMAX_DUTY	90	95	99	%	RT=100kohm
GATE pin ON resistance (as source)	RONSO	3.0	6.0	12.0	Ω	ION=-10mA
GATE pin ON resistance (as sink)	RONSI	1.2	2.5	5.0	Ω	ION=10mA
RT pin voltage	VRT	1.0	1.5	2.0	V	RT=100kohm
SS pin source current	ISSSO	-4.20	-3.0	-2.14	μA	VSS=2V
SS pin Low output voltage	VSS_L	-	0.20	0.50	V	VSTB=0V, Ioss=50uA
Soft start ended voltage	VSS_END	2.7	3.0	3.3	V	SS=SWEEP UP
FB source current	IFBSO	-140	-100	-60	μA	VISENSE=0.2V, VADIM=1.0V, VFB=1.0V
FB sink current	IFBSI	60	100	140	μA	VISENSE=2.0V, VADIM=1.0V, VFB=1.0V
OCP detect voltage	VCS	450	500	550	mV	CS=SWEEP UP
【DC/DC protection block】						
OVP detect voltage	VOVP	2.88	3.00	3.12	V	VOVP SWEEP UP
OVP detect hysteresis	VOVP_HYS	50	100	150	mV	VOVP SWEEP DOWN
SCP detect voltage	VSCP	0.14	0.20	0.26	V	VOVP SWEEP DOWN
SCP detect hysteresis	VSCP_HYS	25	50	75	mV	
OVP pin leak current	OVP_LK	-2	0	2	μA	VOVP=4V

●1.2 Electrical character (Unless otherwise specified Ta=25℃, VCC=12V)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
【LED protection block】						
LED OCP detect voltage	VLEDOCP	3.8	4.0	4.2	V	VISENSE=SWEEP UP
LED OPEN detect voltage	VOPEN	0.05	0.10	0.15	V	VISENSE=SWEEP DOWN
【Analog dimming block】						
ADIM_P pin HIGH voltage	ADIM_PH	2.0	-	3.8	V	
ADIM_P pin LOW voltage	ADIM_PL	-0.3	-	0.8	V	
ADIM_P pin input mask voltage	ADIM_PPU	4.2	-	5.6	V	
ADIM_P pin pull-down resistance	RADIM_P	130	200	300	kΩ	VADIM_P=3.0V
ADIM pin output voltage H	ADIMH	3.201	3.30	3.399	V	ADIM_P=3.3V
ADIM pin output voltage L	ADIML	-	0.0	0.05	V	ADIM_P=0.0V
ADIM pin output resistance	ADIMR	6.6	10	15	kΩ	
ADIM pin leak current	ILADIM	-2	0	2	μA	VADIM=4V, ADIM_P=5.0V
ISENSE pin leak current	IL_ISENSE	-2	0	2	μA	VISENSE=4V
【Dimming signal output block】						
DIMOUT source on-resistance	RONSO	6.0	12.0	24.0	Ω	ION=-10mA
DIMOUT sink on-resistance	RONSI	1.7	3.5	7.0	Ω	ION=10mA
【TC54 block】						
TC54 output voltage	VTC54	5.2	5.4	5.6	V	IO=0mA
TC54 available current	|ITC54|	100	-	-	μA	
TC54_UVLO detect voltage	TC54_TH	2.232	2.4	2.568	V	VSTB=H, TC54=SWEEP DOWN
TC54_UVLO hysteresis	TC54_HYS	50	100	200	mV	VSTB=H->L, TC54=SWEEP UP
TC54 discharge current	TC54_DIS	5	10	15	μA	VSTB=H->L, TC54=4V
【STB block】						
STB pin HIGH voltage	STBH	2.2	-	19	V	VSTB=SWEEP UP
STB pin LOW voltage	STBL	-0.3	-	0.8	V	VSTB=SWEEP DOWN
STB pin input current	ISTB	2.0	3.0	4.5	μA	VSTB=3.0V
【PWM block】						
PWMx pin HIGH Voltage	PWM_H	2.0	-	5.0	V	VPWMx=SWEEP UP
PWMx pin LOW Voltage	PWM_L	-0.3	-	0.8	V	VPWMx=SWEEP DOWN
PWM x pin Pull Down resistance	RPWM	130	200	300	kΩ	VPWMx=3.0V
【FAIL block (OPEN DRAIN)】						
FAILB pin on-resistance	RFAIL	0.75	1.5	3.0	kΩ	VFAIL=1.0V
FAILB pin leak current	ILFAIL	-2	0	2	μA	VFAIL=15V

●**1.3** Pin number, pin name, pin function

No.	name	IN/OUT	function	rating[V]
1	OVP	In	Over voltage protection detection pin	-0.3 to 7
2	UVLO	In	Under voltage lock out detection pin	-0.3 to 7
3	SS	Out	Slow start setting pin	-0.3 to 7
4	RT	Out	For DC/DC switching frequency setting pin	-0.3 to 7
5	PWM1	In	External PWM dimming signal input pin1	-0.3 to 20
6	PWM2	In	External PWM dimming signal input pin2	-0.3 to 20
7	FAILB	Out	Abnormality detection output pin	-0.3 to 20
8	ADIM	In/Out	ADIM signal input-output pin	-0.3 to 20
9	ADIM_P	In	ADIM pulse signal input pin	-0.3 to 20
10	GND	-	-	
11	DIMOUT	Out	Dimming signal pin for driving MOSFET	-0.3 to VCC
12	GATE	Out	DC/DC switching output pin	-0.3 to VCC
13	STB	In	IC On/OFF pin	-0.3 to 20
14	VCC	-	Power supply pin	-0.3 to 20
15	ISENSE	In	Current detection input pin	-0.3 to 7
16	FB	In/Out	Error amplifier output pin	-0.3 to 7
17	CS	In	DC/DC output current detect pin, OCP input pin	-0.3 to 7
18	TC54	Out	5.4V output pin, shutdown timer pin	-0.3 to 7

●2.1.1 Pin ESD Type

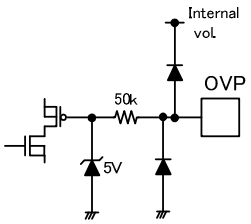
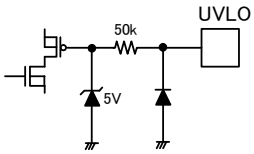
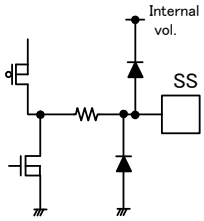
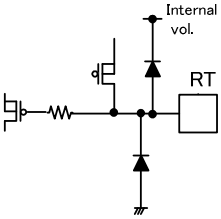
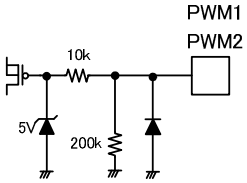
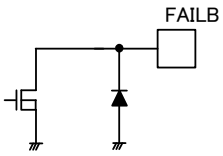
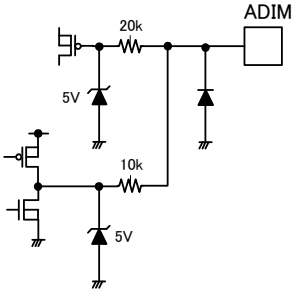
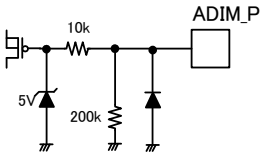
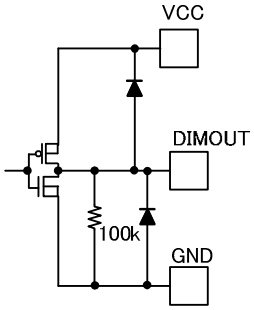
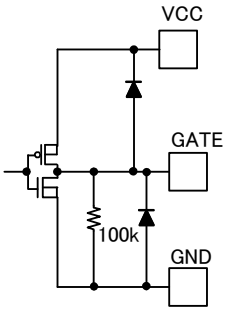
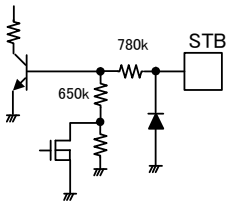
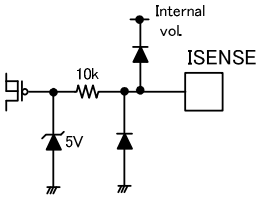
OVP	UVLO	SS
		
RT	**PWM1, PWM2**	**FAILB**
		
ADIM	**ADIM_P**	**DIMOUT**
		
GATE	**STB**	**ISENSE**
		

Figure 4-1. Internal equivalent circuit

●2.1.2 Pin ESD Type

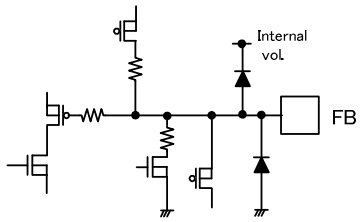
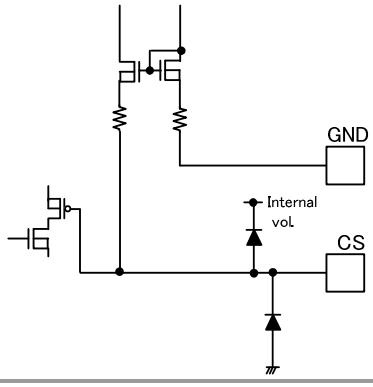
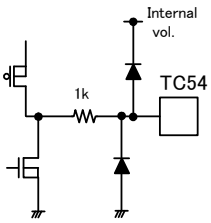
FB	CS	TC54
		

Figure 4-2. Internal equivalent circuit

●2.2 Block diagram

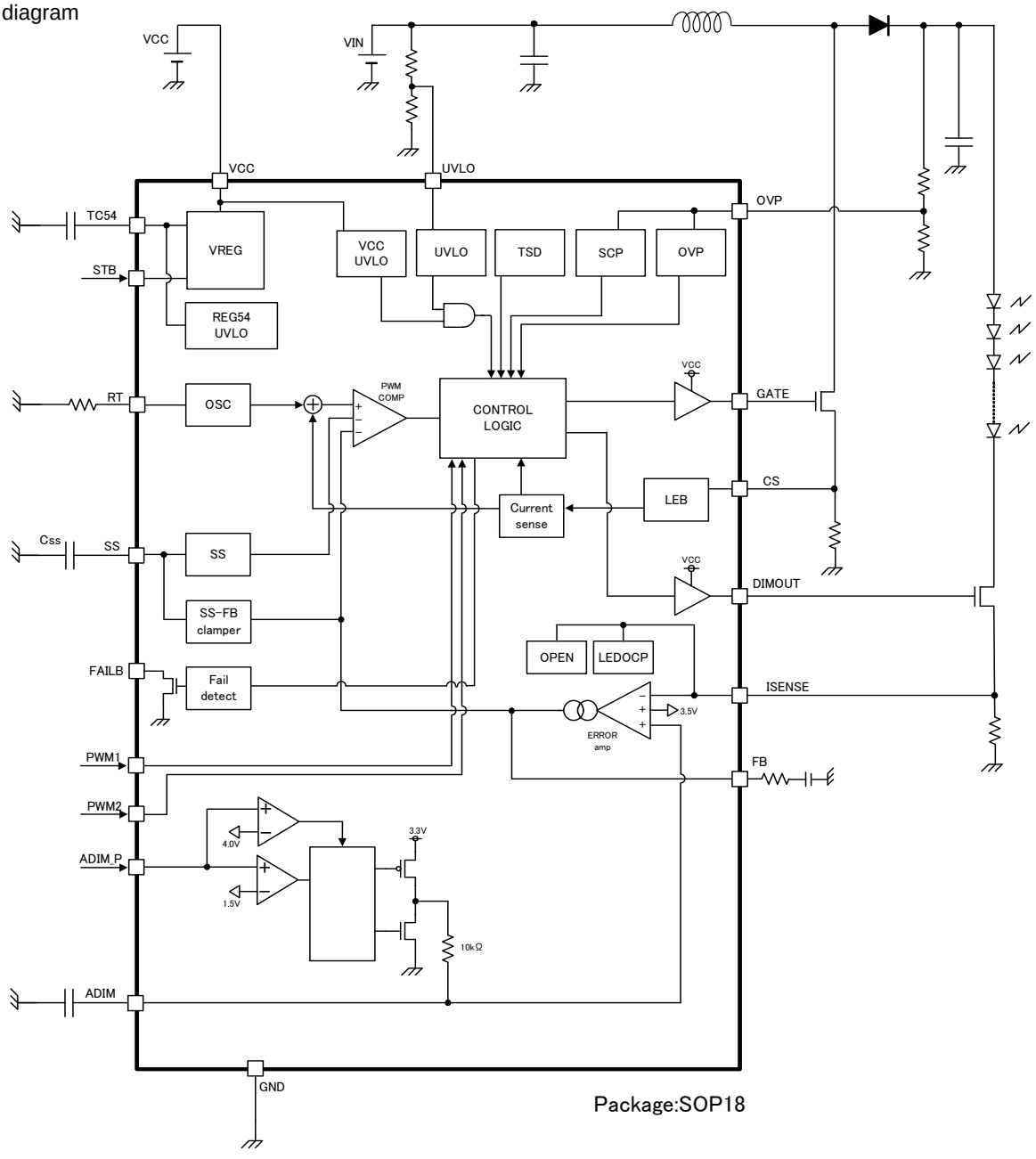


Figure 5. Block diagram

●2.3 Typical performance Curves

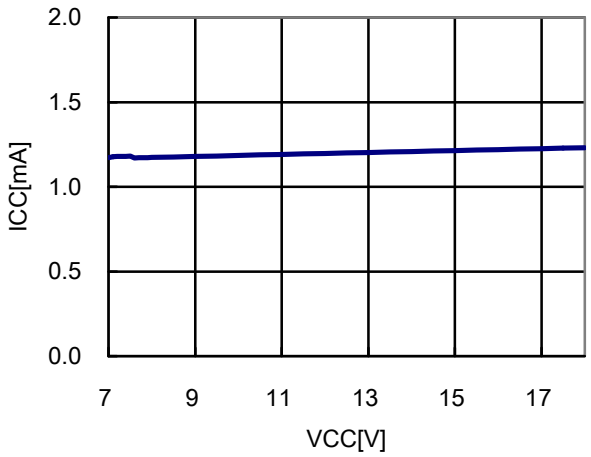


Figure 6. Operating current (ICC) vs VCC

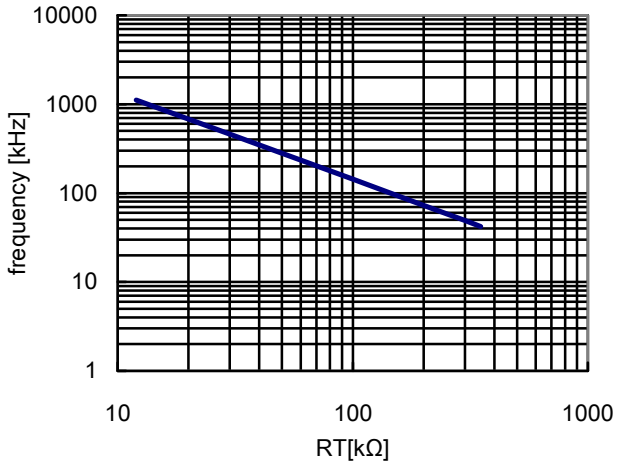


Figure 7. GATE frequency vs RT

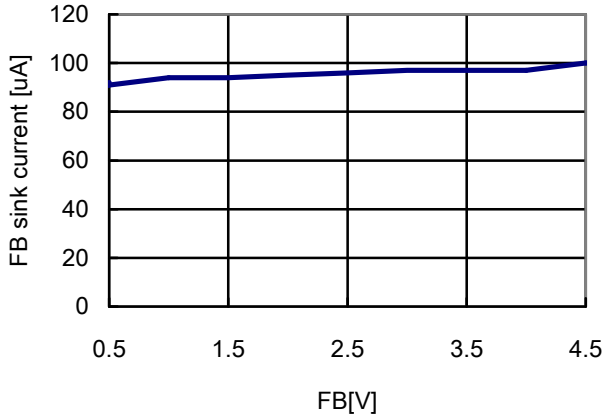


Figure 8. FB sink current vs FB voltage

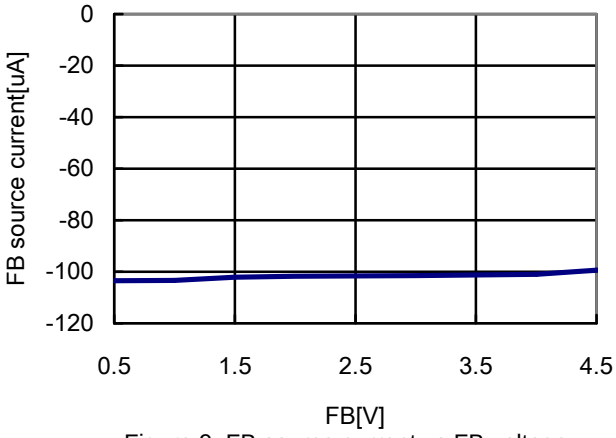


Figure 9. FB source current vs FB voltage

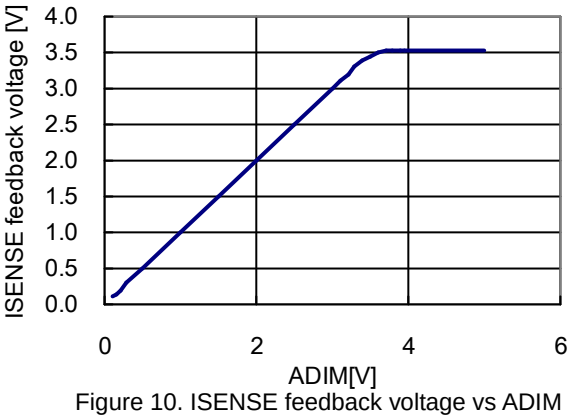


Figure 10. ISENSE feedback voltage vs ADIM

●2.4 Pin function description

○Pin1: OVP

The OVP terminal is the input for over-voltage protection and short circuit protection of output voltage. As OVP is more than 3.0V, the over-voltage protection (OVP) will work. On the other hand, OVP is lower than 0.2V, the short circuit protection (SCP) will work. At the moment of these detections, the BD9285 stops the switching of the output GATE and starts to count up the abnormal interval, but IC doesn't reach latch off state instantaneously until the detection continues up to the number of counts of GATE terminals, which depend on the kind of abnormality. (Please refer to the time chart in the section 3.5.7)

The OVP pin is high impedance, because the internal resistance to a certain bias is not connected.

So, the bias by the external components is required, even if OVP function is not used, because the open connection of this pin is not fixed the potential.

The setting examples is separately described in the section 3.4.6, ”external components selection, how to set OVP, SCP”

○Pin2: UVLO

Under voltage lock out pin for the input voltage of the power stage. More than 3.0V(typ.), IC starts the boost operation and stops lower than 2.8V(typ.).

The UVLO pin is high impedance, because the internal resistance to a certain bias is not connected.

So, the bias by the external components is required, even if UVLO function is not used, because the open connection of this pin is not fixed the potential.

The setting examples is separately described in the section 3.4.5, ”external components selection, how to set UVLO”

○Pin3: SS

The pin which sets soft start interval of DC/DC converter. It performs the constant current charge of 3.0 μA to external capacitance Css(0.001μF to 4.7μF). The switching duty of GATE output will be limited during 0V to 3.0V of the SS voltage.

So the equality of the soft start interval can be expressed as following

Tss = $1.0*10^{6}$*Css Css: the external capacitance of the SS pin.

Regarding of the logic of SS=L

(SS=L) = (PWM1andPWM2 have not asserted H since ResetB=L->H) or (latch off state)

where ResetB = (STB=H) and (VCCUVLO=H) and (UVLO=H) and (TC54UVLO=H)

Please refer to the time chart on soft start behavior in the section 3.7.4

○Pin4: RT

DC/DC switching frequency setting pin. RT set the oscillation frequency inside IC.

○The relationship between the frequency and RT resistance value **(ideal)**

$$R_{RT} = \frac{15000}{f_{SW}[kHz]} \quad [k\Omega]$$

The oscillation setting range from 50kHz to 800kHz.

The setting examples is separately described in the section 3.4.4, ”external components selection, how to set DCDC oscillation frequency”

○Pin5, Pin6: PWM1, PWM2

The ON / OFF terminal of the LED driver. LED lights when both PWM signal are high (DIMOUT = H). The Duty signal of this pin can control the PWM dimming.

The high / low level of PWM pins are following.

State	PWM input voltage
PWM1=H or PWM2=H	PWM=2.0V to 5.0V
PWM1=L or PWM2=L	PWM=-0.3V to 0.8V

PWM1 and PWM2 have the functional difference, and GATE pin outputs only by the logic of PWM1.
This is why only boost operation continues while PWM1=H, PWM2=L. In this case, the adequate confirmation is required not to be over voltage of the output voltage Vout.

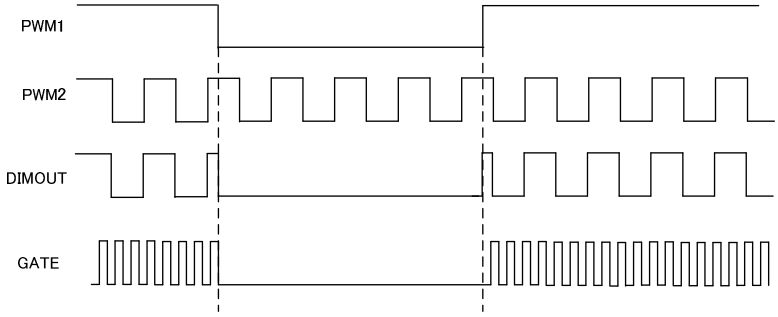


Figure 11. PWM pin function

○Pin7: FAILB

FAIL signal output pin (open drain). As abnormal, the internal NMOS turn on.

Status	FAILB output
Normal	OPEN
Abnormal	GND Level

○Pin8: ADIM

The input output pin for analog dimming signal. The pin function can be changed according to the input level of ADIM_P pin. The pulse-DC transform circuit is included into BD9285F.

ADIM_P input level	ADIM_P pin function	ADIM pin function	Required signal to IC
-0.3V<ADIM_P<3.8V	Pulse signal input for analog dimming	DC output signal for analog dimming	DUTY signal for analog dimming
4.2V <ADIM_P<5.6V	ADIM_P pin function is masked.	DC input signal for analog dimming	DC signal for analog dimming

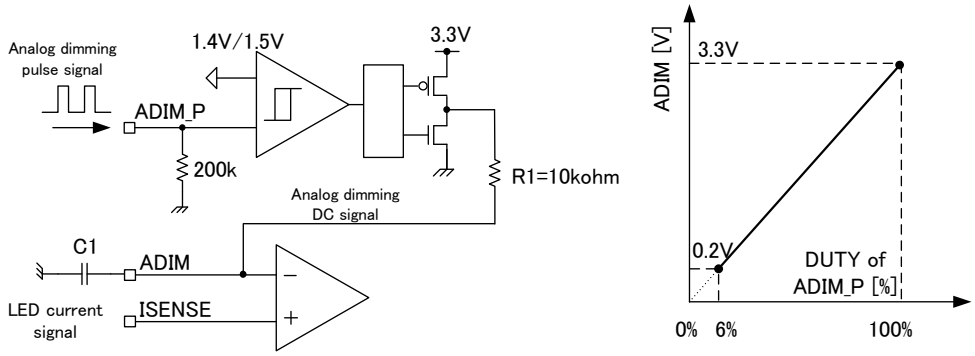


Figure 12. Analog dimming function and character

Above functions enable BD9285 use both of the duty and DC signal for analog dimming.

○When the duty signal is used, that input to the pin ADIM_P with the amplitude about 3.3V. The input duty of ADIM_P needs to be larger than 6% so that the output ADIM is larger than 0.2V. In the case of the normal feedback with analog dimming, The ADIM pin voltage is equal to the ISENSE pin voltage. Therefore, please be careful that the lower ADIM voltage than 0.1V causes the OPEN abnormal detection.

○When the DC signal is used, ADIM_P will be pulled up, and the signal input to the pin ADIM.
In the driver module with more than two BD9285, and the analog dimming is performed by the duty signal, the architecture will be shown in the right figure. That can reduce the LED current error between the channels, because the common circuit of the pulse DC transform is used.
The pulse DC transform circuit outputs DC signal to the ADIM pin with the time constant of R1, C1 in the above diagram. More C1 value, the ripple components of the ADIM pin

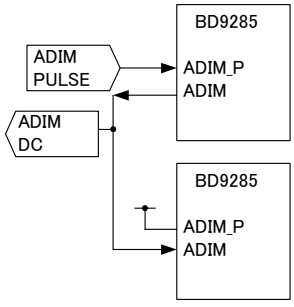


Figure 13. the analog dimming circuit as two BD9285 are used.

is decreased, on the other hand, the transient response is delayed.
And please keep in mind the error voltage if the pull down resistor of ADIM pin will be connected.

○Pin9: ADIM_P

The pulse signal input pin for analog dimming. Please pull up the voltage level more than 4.2V(typ.), when DC signal is used for the analog dimming. In normal operation, please set the input voltage under 5.6V. For more details, please refer to <ADIM> pin descriptions.
The input frequency of this pin assumed from 2kHz to 100kHz. Please keep in mind that the capacitor of ADIM pin is small considering of this input frequency, the error of LED current can be cause.

○Pin10: GND

GND pin of IC.

○Pin11: DIMOUT

This is the output pin for external NMOS of dimming. The below table shows the rough output logic of each operation state, and the output H level is VCC. Please refer to the time chart in the section 3.7 for detail explanations, because The DIMOUT logic has the exceptional behavior. Please insert the resistance between the dimming MOS gate to improve the over shoot of LED current, as PWM turns from low to high.

Status	DIMOUT output
Normal	PWM1 and PWM2
Abnormal	GND Level

○Pin12: GATE

This is the output terminal for driving the gate of the boost MOSFET. The high level is VCC of IC. Frequency can be set by the resistor connected to RT. Please refer to the <RT> pin description for the frequency setting.

○Pin13: STB

ON/OFF setting terminal for IC, which can be used to perform a reset at shutdown. Please reset this pin after latch off.
Regarding of the sequence of turning on, if the input logic STB turns from low to high, the internal power supply is activated. After the positive edge of PWM is input , BD9285 starts the boost operation.

- The input voltage of STB pin toggles the IC state(IC ON/OFF). Please avoid the use of the intermediate level (from 0.8V to 2.2V).

Regarding of the power down sequence, while STB=L and TC54UVLO=H, in order to discharge the output voltage, DIMOUT logic can assert high, depending on the PWM logic. This discharge behavior is separately described in the time chart in the section 3.7.3, or in the section 3.4.2, ”how to shutdown and set TC54 capacitance”

○Pin14: VCC

Power supply pin of IC. Input range is from 9V to 18.0V.

The operation starts more than 7.5 V(TYP.) and shuts down less than 7.2 V(TYP.).

○Pin15: ISENSE

This is the input terminal for the current detection. The error amplifier compares the lower voltage the analog dimming pin ADIM and 3.5V. The abnormal voltage of this pin activates the protection function of LED, such as LEDOCP, OPEN.

[LED OCP Protection Function]

More than ISENSE = 4.0V (typ.), the over current of LED (LEDOCP) will be detected. If that states continues 4096 clock of GATE pin, IC will latch off. (Please refer to the time chart in the section 3.7.8.)

[LED OPEN Protection Function]

If OPEN state (ISENSE<0.1V) continues during 4 clocks interval of GATE terminal, BD9285 starts to count the interval of the abnormal state. In that counting state, DIMOUT logic keeps high output no matter what PWM logic so that the OPEN abnormal state can be detected continuously. If the abnormal condition continues by the completion of counting, BD9285 will be latched off. (Please refer to the time chart in the section 3.7.7.)
Exceptionally the OPEN protect detection are masked in the following conditions,
CASE1. When PWM = L. ISENSE is less than 0.1V even in normally, because DIMOUT = L.
CASE2. In the soft-start interval. ISENSE is less than 0.1V, because of the insufficient output voltage Vout.

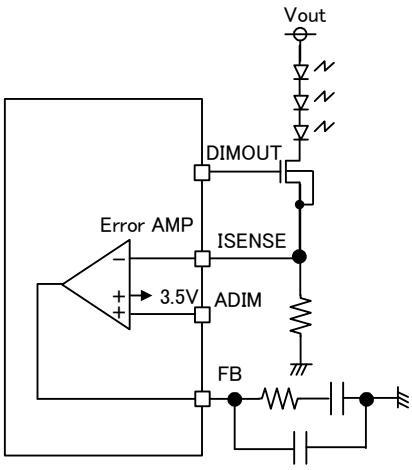


Figure 14. ISENSE pin circuit

○Pin16: FB

This is the output terminal of error amplifier. Monitoring the ISENSE terminal voltage, this pin outputs the error signal with the analog dimming signal (pin ADIM) or 3.5V.
After the completion of the SS, this pin outputs high impedance as the logic “PWM1 and PWM2” asserts low. FB voltage

is hold to the external capacitance.
(For more detail on the compensation setting is described in the section " 3.6 loop compensation".)

○Pin17: CS

The CS pin has two functions.

1. DC / DC current mode Feedback terminal

The inductor current is converted to the CS pin voltage by the sense resistor R_{CS} and this CS pin voltage controls the output voltage by compared with the error amp output.

2. Inductor current limit (OCP) terminal

The CS terminal also has a over current protection (OCP), if it voltage is more than 0.5V, the switching operation will be stopped compulsorily.

Both of above functions are enable after 300ns (typ.) when GATE pin asserts high, because the leading Edge Blanking function is included into this IC to prevent the affect noise. Please refer to the section 3.5.1 “DCDC parts selection / how to set OCP”, for detail explanation.

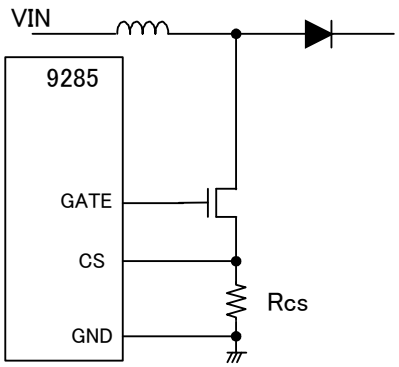


Figure 15. CS pin circuit

○Pin18: TC54

This is the 5.4V (TYP.) output pin that is used for internal power supply. Available current is 100uA

TC54 can be used as a timer for the discharge of output capacitance DCDC. For detailed instructions, please refer the section 3.4.2 “how to shutdown and set TC54 capacitance”

●3.1 Application circuit example
The bellows are example circuits of using BD9285F.

・The basic application circuit example

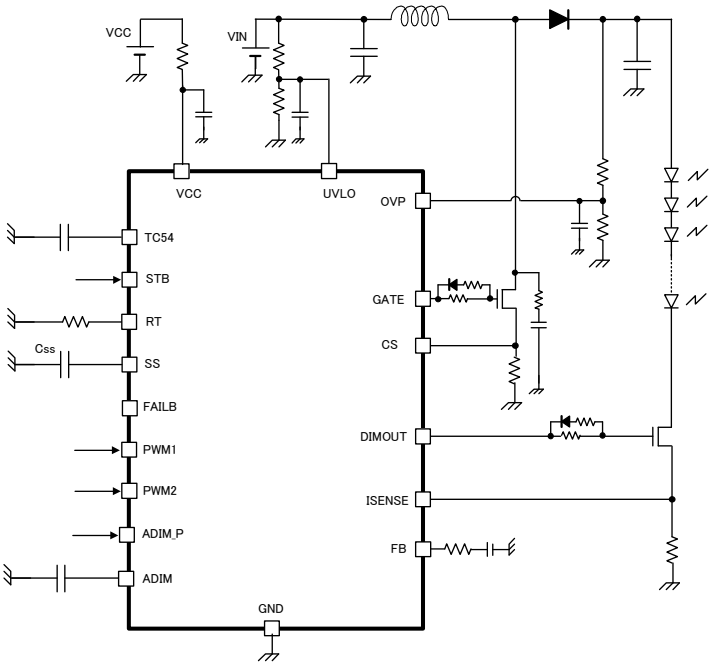


Figure 16. The basic application circuit example

・As for the dimming signal, the single PWM and the DC for analog dimming

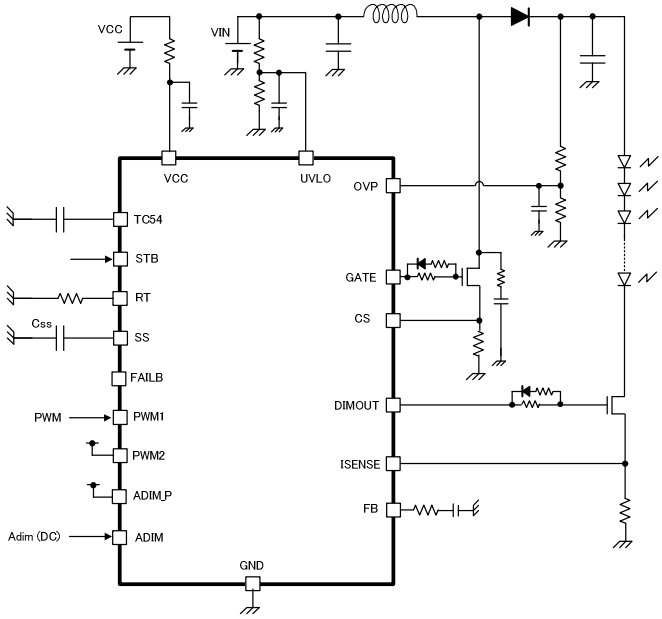
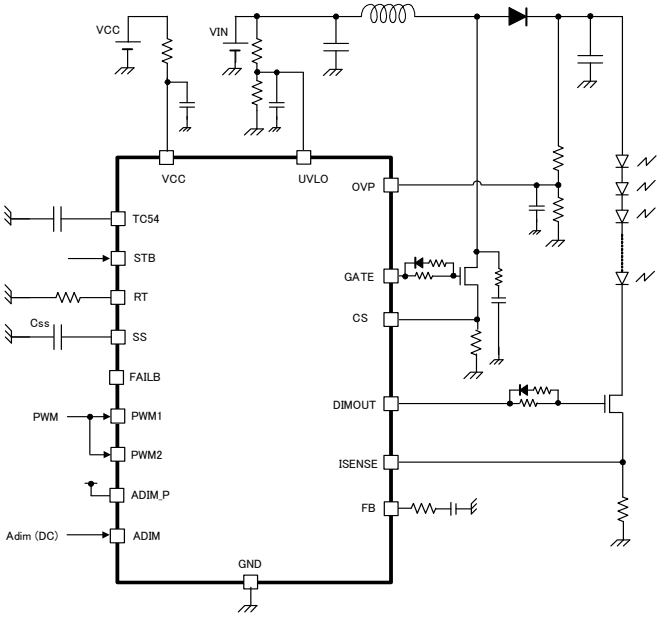


Figure 17. the circuit example with single PWM (1)



PWM1 pin and PWM2 pin are shorted.

Figure 18. the circuit example with single PWM (2)

・Only analog dimming

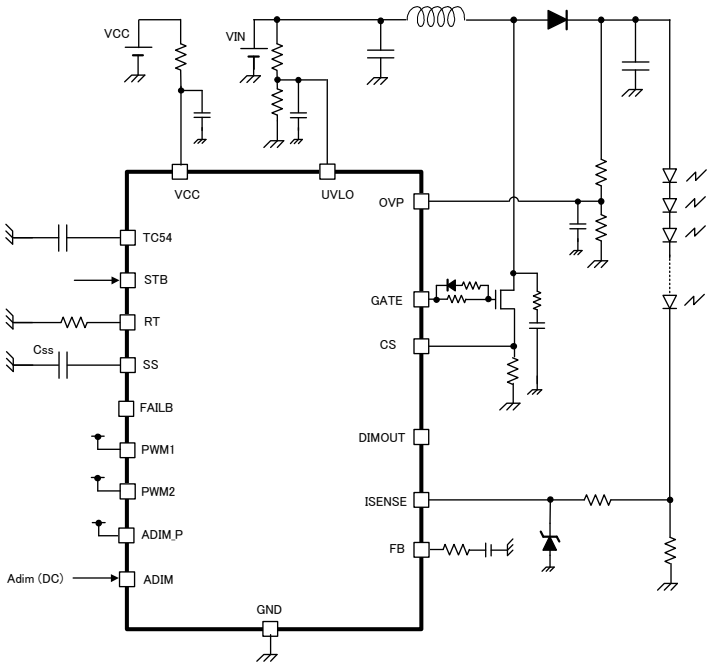


Figure 19. the circuit example of analog dimming only

・Application example when use numerous IC

The application circuit of analog dimming by external duty signal.

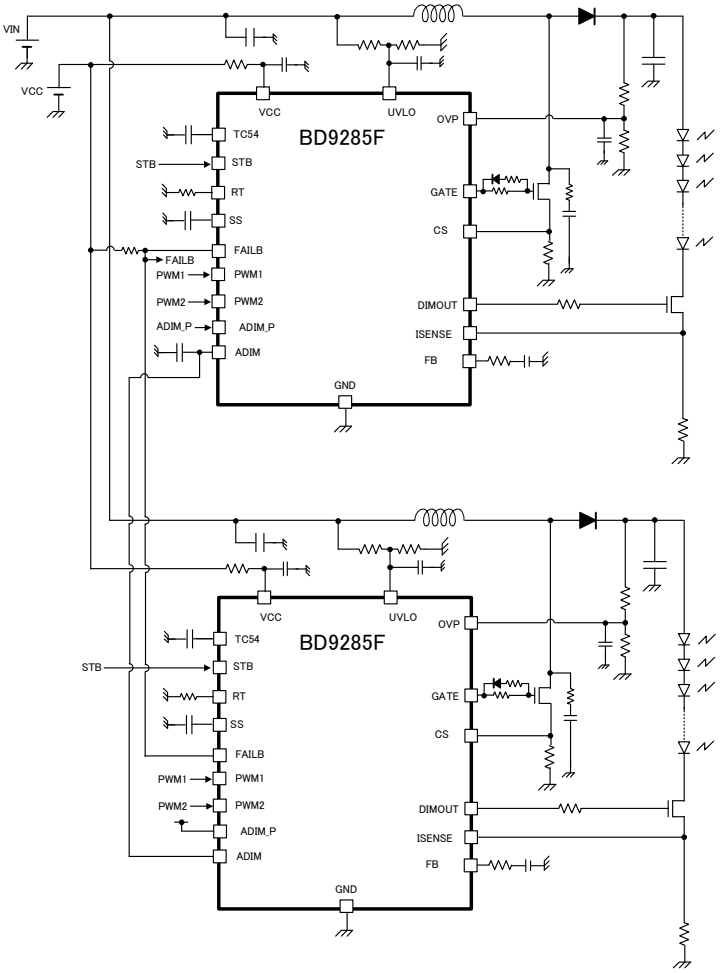


Figure 20. the circuit example of when plural IC is used.

●3.2 **The detection condition list of the protection (TYP. Condition)**

Protection	Detection pin	Detect condition			Release condition	Timer operation	Protection type
		pin condition	PWM1 and PWM2	SS			
LED OPEN	ISENSE	ISENSE < 0.1V	H(4ck)	SS>3.0V	ISENSE > 0.1V	4096 count	Latch off
LED OCP	ISENSE	ISENSE > 4.0V	-	-	ISENSE < 4.0V	4096 count	Latch off
UVLO	UVLO	UVLO<2.8V	-	-	UVLO>3.0V	NO	Auto recovery
TC54 UVLO	TC54	TC54<2.4V	-	-	TC54>2.5V	NO	Auto recovery
VCC UVLO	VCC	VCC<7.2V	-	-	VCC>7.5V	NO	Auto recovery
OVP	OVP	OVP>3.0V	-	-	OVP<2.9V	4 count	Latch off
SCP	OVP	OVP<0.2V	-	SS>3.0V	OVP>0.25V	4096 count	Latch off
OCP	CS	CS>0.5V	-	-	-	NO	Pulse by Pulse

To reset the latch type protection, please input of STB logic to 'L' once. Otherwise the detection of VCCUVLO, TC54UVLO is required.

●3.3 **The behavior list of the protection**

Protect Function	The operation of the protection			
	DC/DC Gate output	Dimming transistor (DIMOUT) logic	Soft Start	FAILB pin
LED OPEN	Stops after latch	H after 4clk, L after latch	discharge after latch	L after latch
LED OCP	Stops immediately	H immediately, L after latch	discharge after latch	L after latch
STB	Stops immediately	L if TC54<2.4V	discharge immediately	OPEN
UVLO	Stops immediately	immediately L	discharge immediately	immediately L
TC54 UVLO	Stops immediately	immediately L	discharge immediately	immediately L
VCC UVLO	Stops immediately	immediately L	discharge immediately	immediately L
OVP	Stops immediately	immediately L	discharge after latch	L after latch
SCP	Stops immediately	immediately L	discharge after latch	L after latch
OCP	Stops immediately	Normal operation	Not discharge	OPEN

Please refer to the timing chart in the section 3.7 for the detail.

●3.4 External components selection

●3.4.1 The start up operation and the setting of Soft Start external capacitance

The below explanations are the start up sequency of BD9285.

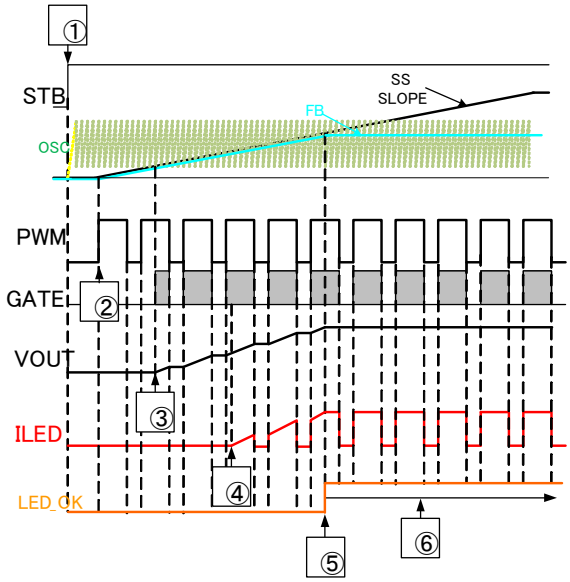


Figure 21. the turn-on waveform

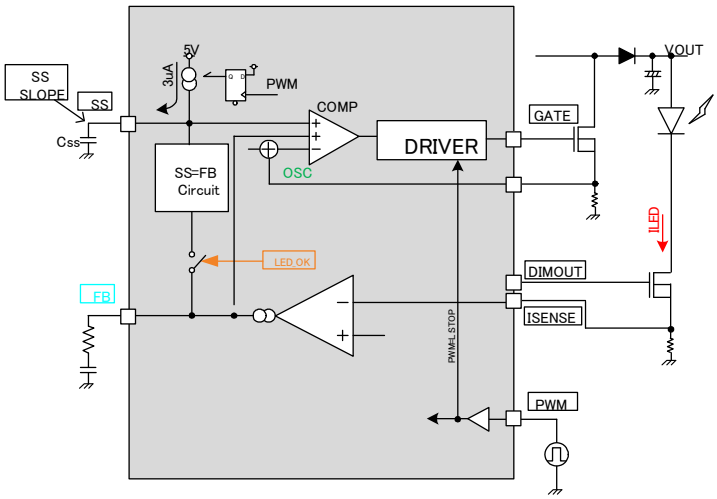


Figure 22. the turn-on circuit

○The explanation of start up sequency

①When STB is H, the internal bias voltage of TC54 rising.

②With the first PWM=H, BD9285 enables output the boost pulse, and the SS start to charge to the external capacitance. At this moment, the voltage of FB will be the same as SS voltage internally regardless of the PWM logic.

③The FB=SS voltage reach the bottom voltage of saw-toothed wave and the DC/DC start to output the pulse signal. Therefore the boost of VOUT is started.

④VOUT is boosted to fixed level, and the LED current is rising.

⑤When the LED current reached to fixed level, FB is removed from SS internally. The start up operation completed.

⑥IC start the normal operation by sensing the voltage of ISENSE pin. When SS is more than 3.0V, even if the LED current does not flows, the clamped circuit of SS and FB is off, and the protect detection of SCP and OPEN starts.

○The setting method of SS external capacitance

As above desribed, DC/DC stops when the PWM1=L. It means the boost operation only enabled within PWM1=H duration and SS time will be extented while boost with samll PWM duty. Also the SS time is affected by the output capacitance, the LED current and application conditions.

Tss is defined as the time for the SS voltage to reach to the FB feedback voltage. Please set the Tss longer than Trise_min, which is the start up time of the minimum PWM duty.

When the FB voltage during LED turns on is expressed VFB, the equality on Tss is the following.

$$T_{ss} = \frac{C_{ss}[F] \times VFB[V]}{3[\mu A]} \quad [Sec]$$

So please set the external capacitance to meet the Tss>>Trise_min.

●3.4.2 **how to shutdown and set TC54 capacitance**

This IC is equipped the discharge function when shutdown is operated.

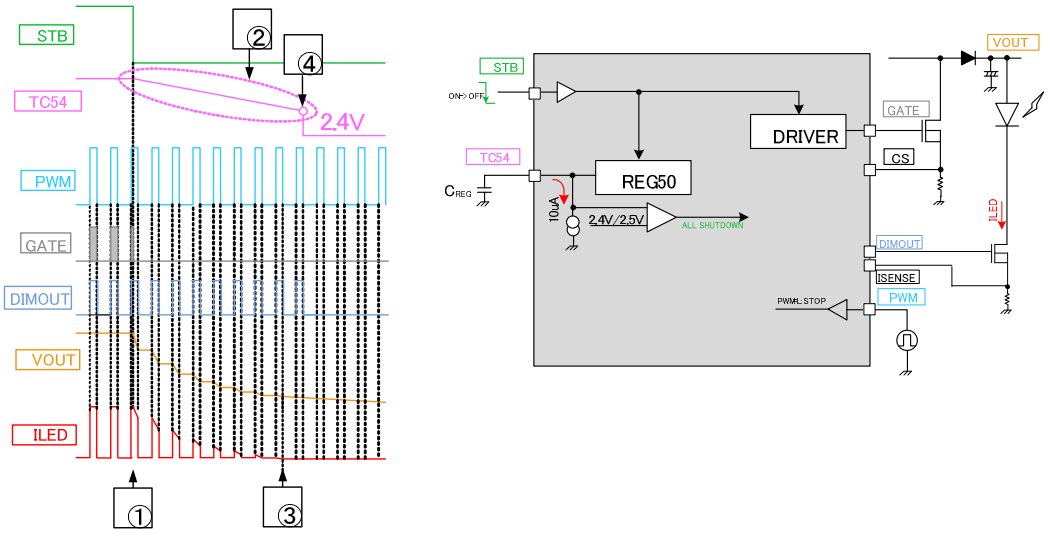


Figure 23. the shutdown waveform and circuit

○Explanation of shutdown sequence

①When STB=L, DC/DC and TC54 are stop.

②When STB=L, TC54UVLO=H, the DIMOUT logic asserts the PWM logic. The voltage of TC54 (5.4V) will decrease by the constant current -10uA and is discharged to 2.4V.

③VOUT will be discharged and ILED decresing.

④When the voltage of TC54 pin is under 2.4V(typ.), the IC will shutdown.

○The setting method of TC54 external capacitance

Please use below formula to calculate the shutdown time TOFF.

$$T_{OFF} = \frac{C_{REG}[F] \times 3.0\,[V]}{10\,[uA]} \quad [Sec]$$

As shown the above, the PWM signal is required even after STB=L.

The discharge interval of VOUT is the longest in the minimum PWM duty. Please set the Creg value with a enough timing margin from the end of the VOUT discharge to shutdown.

●3.4.3 The LED current setting

LED current can be adjusted by setting the resistance R_{ISENSE} which connects to ISENSE pin.

○the relationship between RISET and ILED current

With DC dimming

$$R_{ISENSE} = \frac{ADIM\,[V]}{I_{LED}[A]}[\Omega]$$

Without DC dimming

$$R_{ISENSE} = \frac{3.5[V]}{I_{LED}[A]}[\Omega]$$

[setting example]

If ILED current is 400mA as ADIM is 1.5V, we can calculate R_{ISENSE} as below.

$$R_{ISENSE} = \frac{ADIM\,[V]}{I_{LED}[A]} = \frac{1.5[V]}{0.4[A]} = 3.75[\Omega]$$

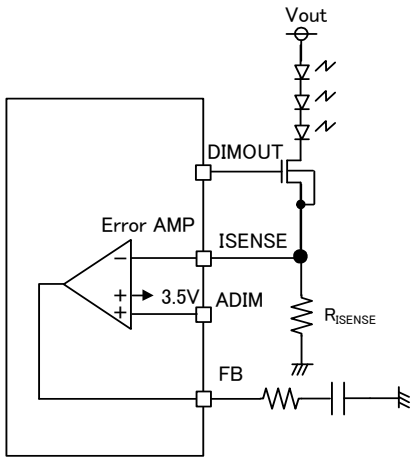


Figure 24. the example of LED current setting

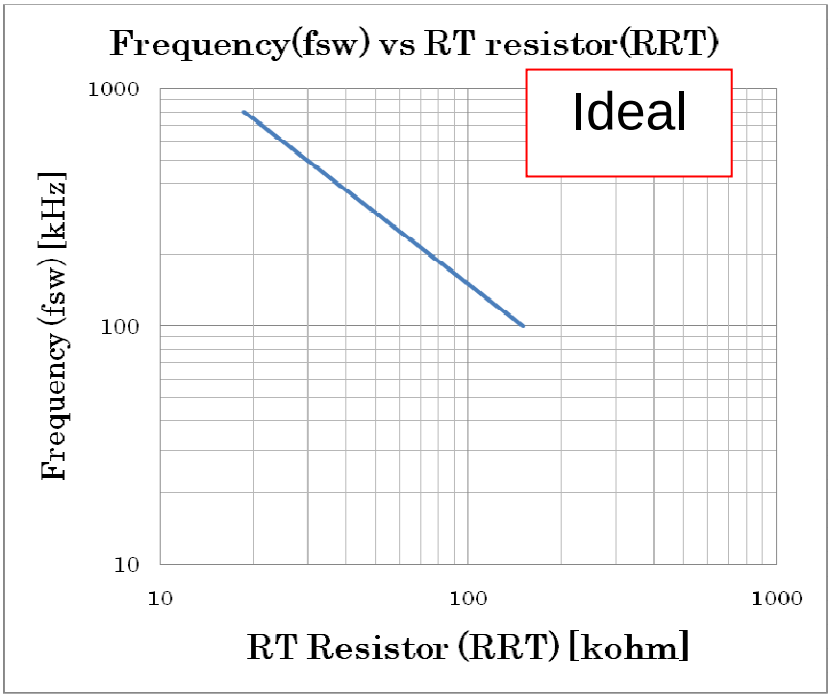
●3.4.4. how to set DCDC oscillation frequency

R_{RT} which connects to RT pin set the oscillation frequency of DCDC.

○ **the relationship between OSC and R_{RT} (ideal)**

$$R_{RT} = \frac{15000}{f_{SW}[kHz]} \quad [k\Omega]$$

where fsw is the oscillation frequency of DCDC [kHz]



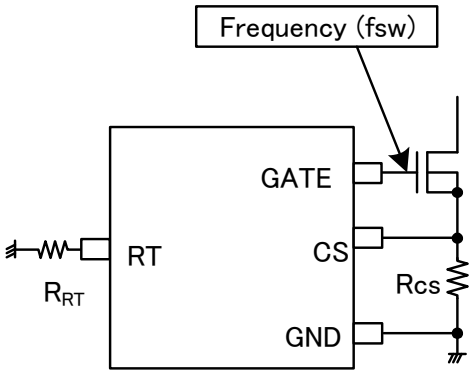


Figure 25. RT pin setting example

This equation is an ideal equation in which correction factors are not applied.
The adequate verification with an actual set needs to be performed to set frequency precisely.

[setting example]

If DCDC oscillation frequency is 200kHz, we can calculate the R_{RT} as below.

$$R_{RT} = \frac{15000}{f_{sw}[kHz]} = \frac{15000}{200[kHz]} = 75 \quad [k\Omega]$$

●3.4.5. how to set UVLO

Under voltage lock out pin for the input voltage of the power stage. More than 3.0V(typ.), IC starts boost operation and stops lower than 2.8V(typ.).

The UVLO pin is high impedance, because the internal resistance to a certain bias is not connected.

So, the bias by the external components is required, even if UVLO function is not used, because the open connection of this pin is not fixed the potential.

The resistor value can be calculated by the below formula, if the VIN voltage is monitored, and that is divided by the resistor R1, R2 like the below diagram.

○UVLO detection equality

If VIN decreases, R1, R2 value is expressed the following formula by the VINdet, the detect voltage of UVLO.

$$R1 = R2[k\Omega] \times \frac{(VIN_{DET}[V] - 2.8[V])}{2.8[V]} \quad [k\Omega]$$

○UVLO release equality

By using the R1, R2 in the above equality, the release voltage of UVLO can be expressed as following.

$$VIN_{CAN} = 3.0V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} \quad [V]$$

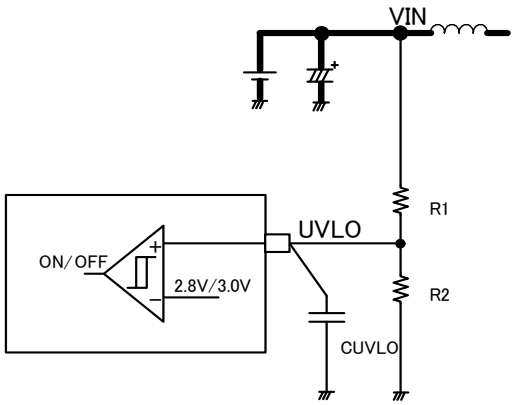


Figure 26. UVLO setting example

[setting example]

If the normal input voltage, VIN is 24V, the detect voltage of UVLO is 18V, R2 is 30k ohm, R1 is calculated as following.

$$R1 = R2[k\Omega] \times \frac{(VIN_{DET}[V] - 2.8[V])}{2.8[V]} = 30[k\Omega] \times \frac{(18[V] - 2.8[V])}{2.8[V]} = 163 \quad [k\Omega]$$

By using these R1, R2, the release voltage of UVLO, VINcan can be calculated as following.

$$VIN_{CAN} = 3.0[V] \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} = 3.0[V] \times \frac{30[k\Omega] + 163[k\Omega]}{30[k\Omega]}[V] = 19.3 \quad [V]$$

●3.4.6. how to set OVP, SCP

The OVP terminal is the input for over-voltage protection and short circuit protection of output voltage.
The OVP pin is high impedance, because the internal resistance to a certain bias is not connected.
So, the bias by the external components is required, even if OVP function is not used, because the open connection of this pin is not fixed the potential.
The resistor value can be calculated by the below formula, if the VOUT voltage is monitored, and that is divided by the resistor R1, R2 like the below diagram.

○OVP detection equality

If the VOUT is boosted abnormally, VOVPdet is the detect voltage of OVP, R1, R2 can be expressed by the following formula.

$$R1 = R2[k\Omega] \times \frac{(VOVP_{DET}[V] - 3.0[V])}{3.0[V]} \quad [k\Omega]$$

○OVP release equality

By using the R1, R2 in the above equality, the release voltage of OVP, VOVPcan can be expressed as following.

$$VOVP_{CAN} = 2.9V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} \quad [V]$$

○SCP detection equality

In the same way, the detect voltage of SCP, VSCPdet is

$$VSCP_{DET} = 0.2V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} \quad [V]$$

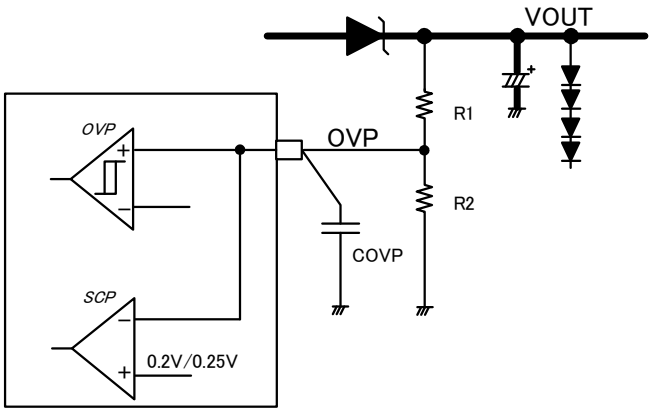


Figure 27. OVP/SCP setting example

[setting example]

If the normal output voltage, VOUT is 40V, the detect voltage of OVP is 48V, R2 is 10k ohm, R1 is calculated as following.

$$R1 = R2[k\Omega] \times \frac{(VOVP_{DET}[V] - 3.0[V])}{3.0[V]} = 10[k\Omega] \times \frac{(48[V] - 3[V])}{3[V]} = 150 \quad [k\Omega]$$

By using these R1, R2, the release voltage of OVP, VOVPcan can be calculated as following.

$$VOVP_{CAN} = 2.9[V] \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} = 2.9[V] \times \frac{10[k\Omega] + 150[k\Omega]}{10[k\Omega]}[V] = 46.4 \quad [V]$$

Moreover, by using these R1, R2 the detect voltage of SCP, VSCPdet is

$$VSCP_{DET} = 0.2[V] \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} = 0.2[V] \times \frac{10[k\Omega] + 150[k\Omega]}{10[k\Omega]}[V] = 3.2 \quad [V]$$

●3.4.7. how to set the interval until latch off

BD9285 built in the counter by latch off time, that is performed by counting the oscillation clock which is set by the RT pin. Since the common oscillation circuit is used for counting, the interval until latch off is corresponding to the 4096 clock, which the GATE pulse output continuously. Please refer the time chart of the operation from the detect abnormality to the latch off in the section 3.7.

○latch off time

BD9285 starts the counting up from the detection of each abnormal state, falls to the latch off state when the following interval has passed.
Only PWM=L input does not reset the timer counter, if the abnormal state continues.

$$LATCH_{TIME} = 2^{12} \times \frac{R_{RT}[\Omega]}{1.5 \times 10^{10}} = 4096 \times \frac{R_{RT}[k\Omega]}{1.5 \times 10^{7}} [\mathrm{sec}]$$

Where $LATCH_{TIME}$ is the interval until latch off state
R_{RT} is the connected resistor of RT pin.

[setting example]

If the resistor of RT pin is 100k ohm, the timer latch interval is as following.

$$LATCH_{TIME} = 4096 \times \frac{R_{RT}[k\Omega]}{1.5 \times 10^{7}} = 4096 \times \frac{100[k\Omega]}{1.5 \times 10^{7}} = 27.3[m\mathrm{sec}]$$

●3.5. DCDC parts selection

3.5.1. how to set OCP / the calculation method for the current rating of DCDC parts

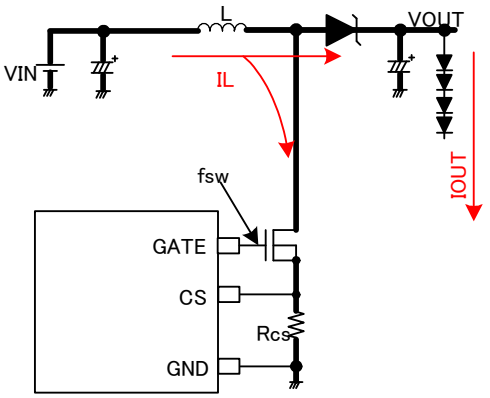
BD9285 stops the switching by the OCP detect, when the CS pin voltage is more than 0.5V. The resistor value of CS pin, R_{CS} need to be considered by the coil L current. And the current rating of DCDC external parts is required more than the peak current of the coil.
It is shown below that the calculation method of the coil peak current, the selection method of Rcs (the resistor value of CS pin) and the current rating of the external DCDC parts.

(the calculation method of the coil peak current, Ipeak)
At first, since the ripple voltage at CS pin depend on the application condition of DCDC, those put onto the equality to calculate as following.
The output voltage = VOUT [V]
LED total current = IOUT [A]
The DCDC input voltage of the power stage = VIN [V]
The efficiency of DCDC = η [%]
And then, the averaged input current IIN is calculated by the following equality

$$I_{IN} = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} \quad [A]$$

And the ripple current of the inductor L (ΔIL[A]) can be calculated by using DCDC the switching frequency, fsw, as following.

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} \quad [A]$$



On the other hand, the peak current of the inductor Ipeak can be expressed as the following equality.

$$\boxed{Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2} \quad [A]} \qquad \cdots (1)$$

Therefore, the bottom of the ripple current Imin is or 0

$$\mathrm{Im}\,in = I_{IN}[A] - \frac{\Delta IL[A]}{2}$$

As Imin>0, that operation mode is CCM (Continuous Current Mode), otherwise another mode is DCM (Discontinuous Current Mode).

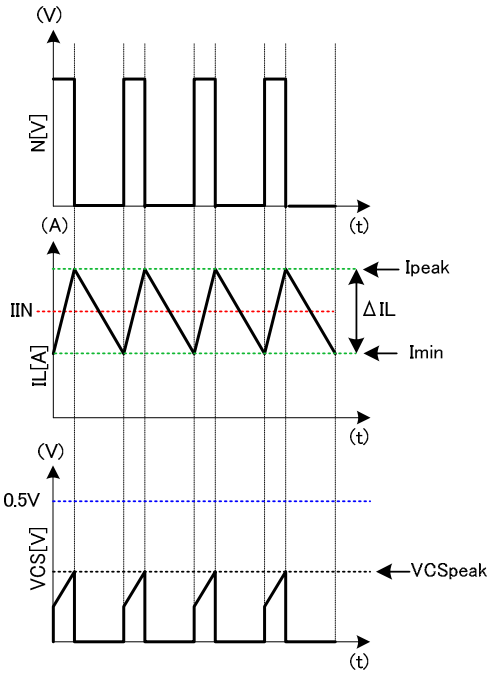


Figure 28. Coil current waveform

(the selection method of Rcs)
Ipeak flows into Rcs and that cause the voltage signal to CS pin. (Please refer the right timing chart)
That peak voltage VCSpeak is as following.

$$VCS_{peak} = Rcs \times Ipeak \quad [V]$$

As this VCSpeak reaches to 0.5V, the DCDC output stops the switching.
Therefore, Rcs value is necessary to meet the under condition.

$$\boxed{Rcs \times Ipeak[V] << 0.5[V]}$$

(the current rating of the external DCDC parts)
The peak current as the CS voltage reaches to OCP level (0.5V) is defined as Ipeak_det.

$$I_{peak\_det} = \frac{0.5[V]}{Rcs[\Omega]} \quad [A] \qquad \cdots (2)$$

The relation among Ipeak (equality (1)), Ipeak_det (equality (2)) and the current rating of parts is required to meet the following

$$I_{peak} << I_{peak\_det} << \text{The current rating of parts}$$

Please make the selection of the external parts to meet the above condition such as FET, Inductor, diode.

[setting example]
The output voltage = VOUT [V] = 40V
LED total current = IOUT [A] = 0.48V

The DCDC input voltage of the power stage = VIN [V] = 24V
The efficiency of DCDC = η [%] = 90%
The averaged input current IIN is calculated as the following.

$$I_{IN}[A] = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} = \frac{40[V] \times 0.48[A]}{24[V] \times 90[\%]} = 0.89 \quad [A]$$

And the ripple current of the inductor L (ΔIL[A]) can be calculated if the switching frequency, fsw = 200kHz, the inductor, L=100µH.

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} = \frac{(40[V] - 24[V]) \times 24[V]}{100 \times 10^{-6}[H] \times 40[V] \times 200 \times 10^{3}[Hz]} = 0.48 \quad [A]$$

Therefore the inductor peak current, Ipeak is

$$\boxed{Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2}[A] = 0.89[A] + \frac{0.48[A]}{2} = 1.13 \quad [A]}$$

The calculation result of the peak current

If Rcs is assume to be 0.3 ohm

$$\boxed{VCS_{peak} = Rcs \times Ipeak = 0.3[\Omega] \times 1.13[A] = 0.339 \quad [V] << 0.5V}$$

The Rcs value confirmation

The above condition is met.
And Ipeak_det, the current OCP works is

$$I_{peak\_det} = \frac{0.5[V]}{0.3[\Omega]} = 1.67 \quad [A]$$

If the current rating of the used parts is 2A,

$I_{peak} << I_{peak\_det} <<$ The current rating $\boxed{= 1.13[A] << 1.67[A] << 2.0[A]}$

The current rating confirmation of DCDC parts

This inequality meets the above relationship. The parts selection is proper.
And Imin, the bottom of the IL ripple current can be calculated as following.

$$I_{MIN} = I_{IN}[A] - \frac{\Delta IL[A]}{2}[A] = 1.13[A] - 0.48[A] = 0.65[A] >> 0$$

This inequality implies the operation is the continuous current mode.

3.5.2. Inductor selection

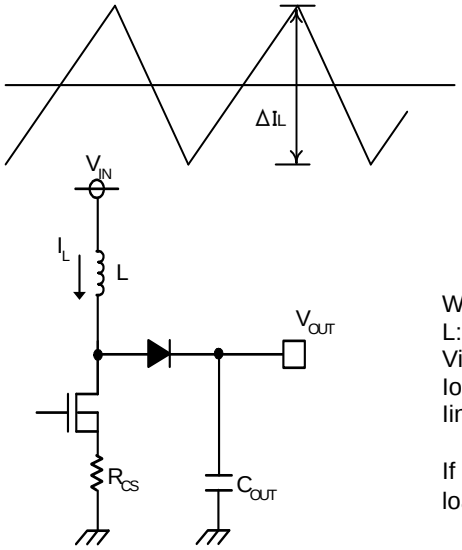


Figure 29. the waveform and the circuit of inductor current

The inductor value affects the input ripple current. The equality in the section 3.5.1 is as following.

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} \quad [A]$$

$$I_{IN} = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} \quad [A]$$

$$Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2} \quad [A]$$

Where
L: the coil inductance [H] Vout: the DCDC output voltage [V]
Vin: the input voltage [V]
Iout: the output load current (the summation of LED current) [A]
Iin: the input current [A] Fsw: the oscillation frequency [Hz]

If in the continuous current mode, Please set ⊿IL to 30% - 50% of the output load current.

* The current exceeding the rated current value of inductor flown through the coil causes magnetic saturation, results in decreasing in efficiency. Inductor needs to be selected to have such adequate margin that peak current does not exceed the rated current value of the inductor.
* To reduce inductor loss and improve efficiency, inductor with low resistance components (DCR, ACR) needs to be selected

3.5.3. Output capacitance Cout selection

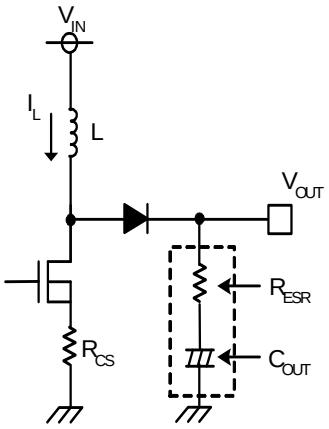


Figure 30. the output capacitor circuit

Output capacitor needs to be selected in consideration of equivalent series resistance required to even the stable area of output voltage or ripple voltage. Be aware that set LED current may not be flown due to decrease in LED terminal voltage if output ripple component is high.
Output ripple voltage ⊿V_{OUT} is determined by Equation (4):

$$\Delta V_{OUT} = ILMAX \times R_{ESR} + \frac{1}{C_{OUT}} \times \frac{I_{OUT}}{\eta} \times \frac{1}{f_{SW}} [V] \quad \cdots\cdots \quad (4)$$

where, R_{ESR} is the equivalent series resistance of Cout.

* Rating of capacitor needs to be selected to have adequate margin against output voltage.
* To use an electrolytic capacitor, adequate margin against allowable current is also necessary. Be aware that the LED current is larger than the set value transitionally in case that LED is provided with PWM dimming especially.

3.5.4. MOSFET selection

Though there is no problem if the absolute maximum rating is larger than the rated current of the inductor L, or is larger than the sum of the tolerance voltage of C_{OUT} and the rectifying diode V_F. The product with small gate capacitance (injected charge) needs to be selected to achieve high-speed switching.

* One with over current protection setting or higher is recommended.
* The selection of one with small on resistance results in high efficiency.

3.5.5. Rectifying diode selection

A schottky barrier diode which has current ability higher than the rated current of L, the reverse voltage larger than the tolerance voltage of C_{OUT}, and the low forward voltage VF especially needs to be selected.

●3.6. Loop compensation

A current mode DCDC converter has each one pole (phase lag) f_p due to CR filter composed of the output capacitor and the output resistance (= LED current) and zero (phase lead) f_Z by the output capacitor and the ESR of the capacitor.
Moreover, a step-up DCDC converter has RHP zero (right-half plane zero point) f_{ZRHP} which is unique with the boost converter. This zero may cause the unstable feedback. To avoid this by RHP zero, the loop compensation that the cross-over frequency f_c set as following, is suggested.
$fc = f_{ZRHP} /5$ (f_{ZRHP}: RHP zero frequency)
Considering the response speed, the below calculated constant is not always optimized completely. It needs to be adequately verified with an actual device.

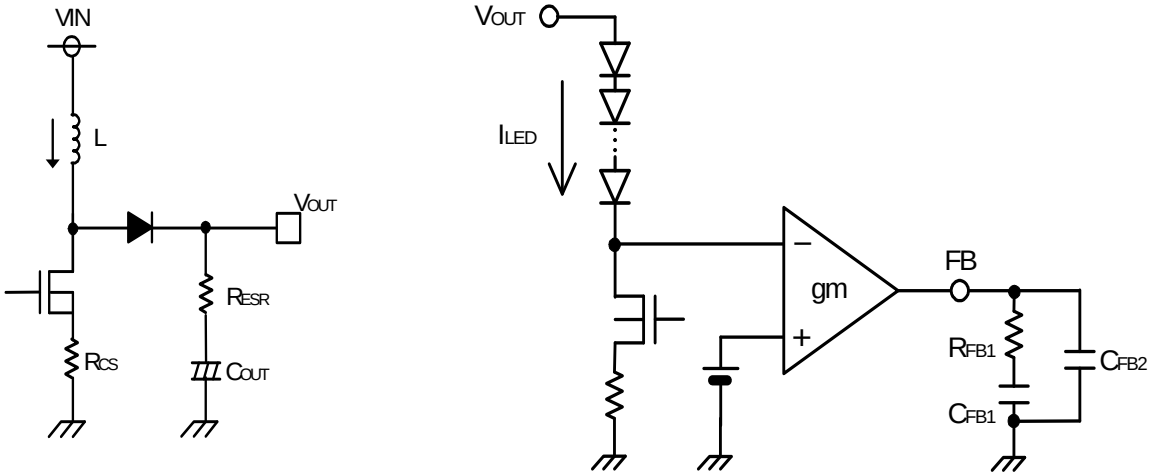


Figure 31. the circuit of output stage and the error amplifier

i. Calculate the pole frequency fp and the RHP zero frequency f_{ZRHP} of DC/DC converter

$$f_p = \frac{I_{LED}}{2\pi \times V_{OUT} \times C_{OUT}} [Hz] \qquad f_{ZRHP} = \frac{V_{OUT} \times (1-D)^2}{2\pi \times L \times I_{LED}} [Hz]$$

Where I_{LED} = the summation of LED current, $D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$ (Continuous Current Mode)

ii. Calculate the phase compensation of the error amp output ($f_c = f_{ZRHP}/5$)

$$R_{FB1} = \frac{f_{RHZP} \times R_{CS} \times I_{LED}}{5 \times f_p \times gm \times V_{OUT} \times (1-D)} [\Omega] \qquad C_{FB1} = \frac{1}{2\pi \times R_{FB1} \times f_p} [F]$$

Where

$$gm = 4.0 \times 10^{-4} [S]$$

iii. Calculate zero to compensate ESR (R_{ESR}) of C_{OUT} (electrolytic capacitor)

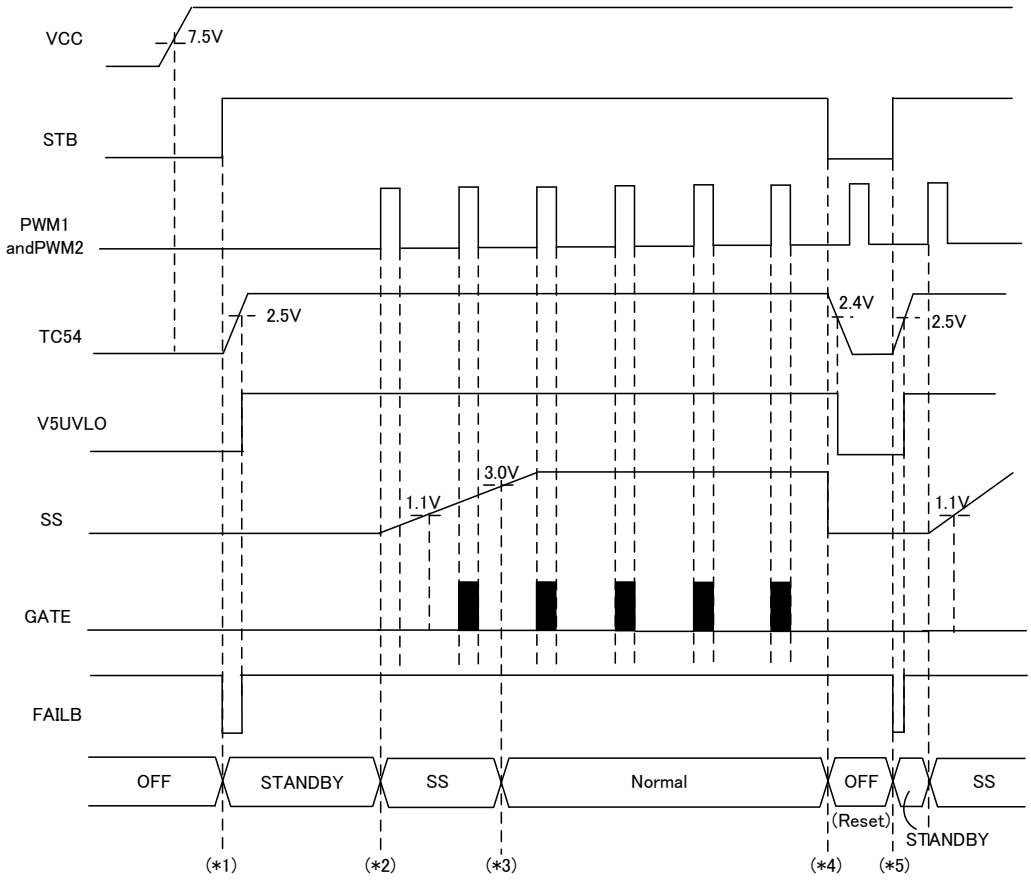
$$C_{FB2} = \frac{R_{ESR} \times C_{OUT}}{R_{FB1}} [F]$$

*When a ceramic capacitor (with R_{ESR} of the order of milliohm) is used to C_{OUT}, the operation is stabilized by insertion of C_{FB2}.

To improve the transient response, R_{FB1} need to be increase, C_{FB1} need to be decrease. It needs to be adequately verified with an actual device in consideration of vary from parts to parts since phase margin is decreased.

●3.7. Timing chart

3.7.1 starting up 1 (STB inputs and PWM signal succeeds)



(*1)…TC54 starts up if STB turns from L to H. The pin SS is not charged in the state that the PWM signal is not input, the boost is not started.

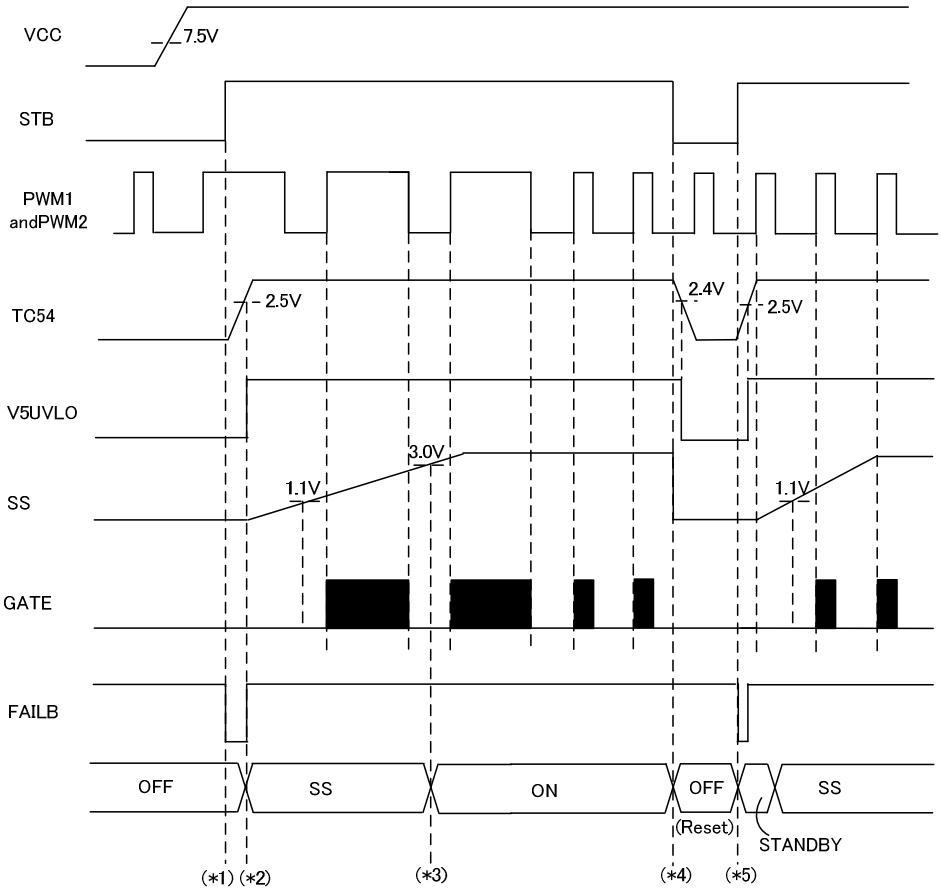
(*2)…The charge of the pin SS starts by the positive edge of PWM=L to H, and the soft start starts. The GATE pulse outputs only during PWM=H. And as the SS is less than 1.1V, the pulse does not output. The pin SS continues charging in spite of the assertion of PWM and OVP.

(*3)…The soft start interval will end if the voltage of the pin SS, Vss reaches to 3.0V. By this time, BD9285 boost Vout where the set LED current flows. It is started to monitor the abnormal detection of SCP and OPEN.

(*4)…As STB=L, instantaneously the boost operation is stopped. (GATE=L, SS=L) On the other hand, the discharge circuit works in the interval “STB=L and V5UVLO=H”. Please refer to the time chart in the section 3.7.3 for details.

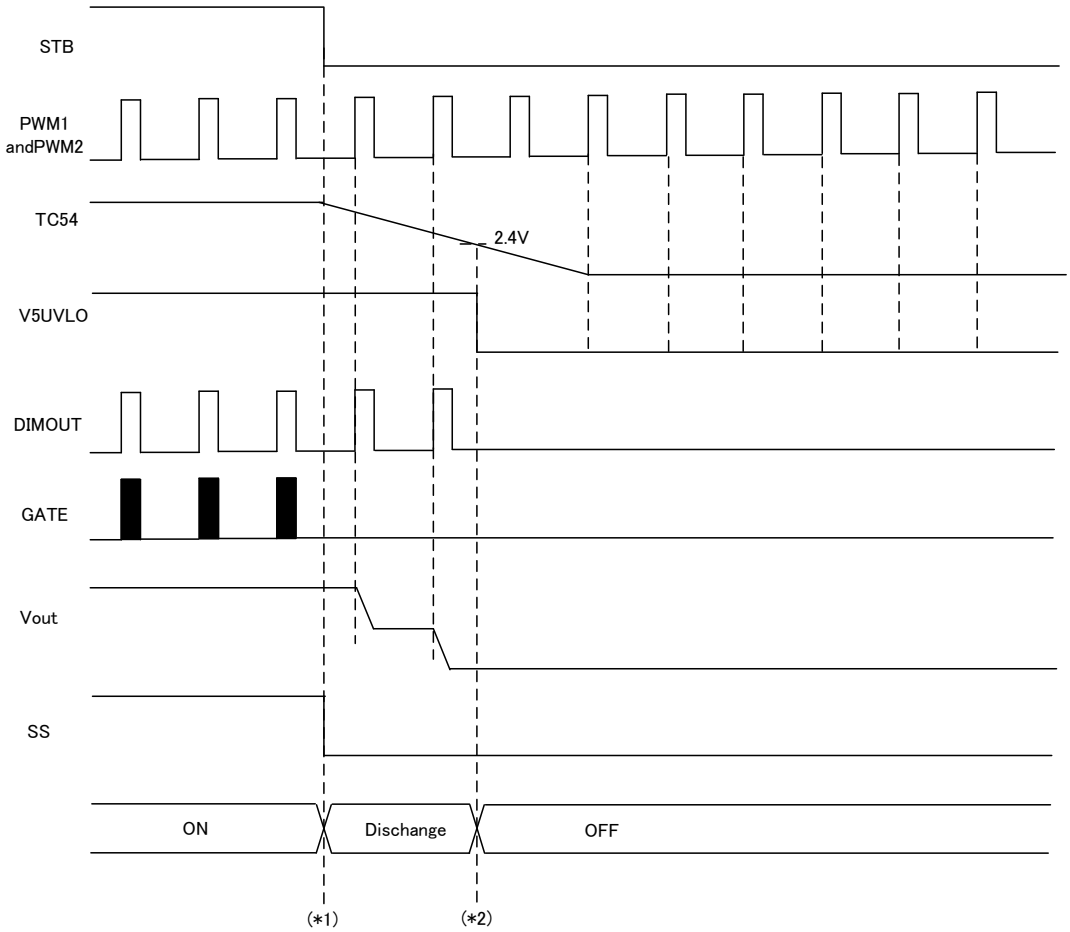
(*5)…As STB=H again, the boost operation restarts by the next PWM=L to H. It is the same operation as the timing of (*1). Please refer to the section 3.4.1 for the setting of soft start external capacitance.

3.7.2 starting up 2 (PWM signal inputs and STB succeeds)



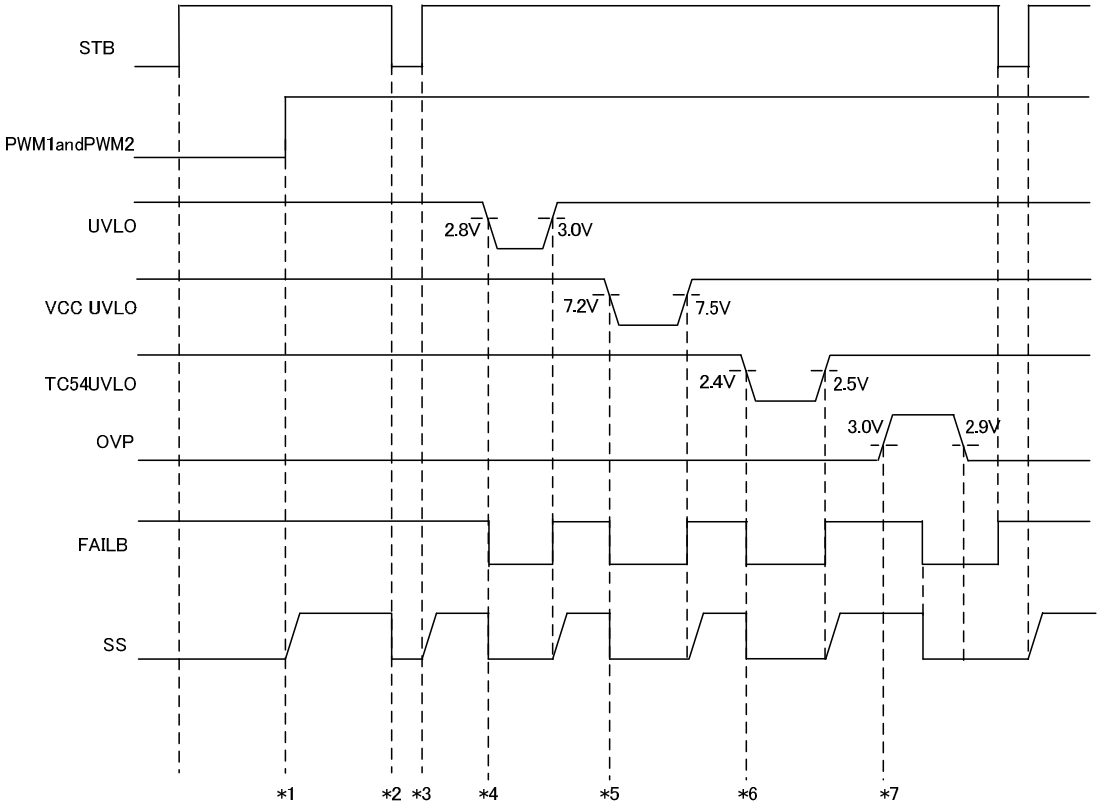
(*1)…TC54 starts up if STB turns from L to H.
(*2)…At the moment the release of V5UVLO (the UVLO of the pin TC54), or the time of the positive edge of PWM=L to H, the soft start starts. The GATE pulse outputs only during PWM1=H. And as the SS is less than 1.1V, the pulse does not output. The pin SS continues charging in spite of the assertion of PWM and OVP.
(*3)…The soft start interval will end if the voltage of the pin SS, Vss reaches to 3.0V. By this time, BD9285 boost Vout where the set LED current flows. It is started to monitor the abnormal detection of SCP and OPEN.
(*4)…As STB=L, instantaneously the boost operation is stopped. (GATE=L, SS=L) On the other hand, the discharge circuit works in the interval “STB=L and V5UVLO=H”. Please refer to the time chart in the section 3.7.3 for details.
(*5)…As STB=H again, it is the same operation as the timing of (*1).

3.7.3 turn off



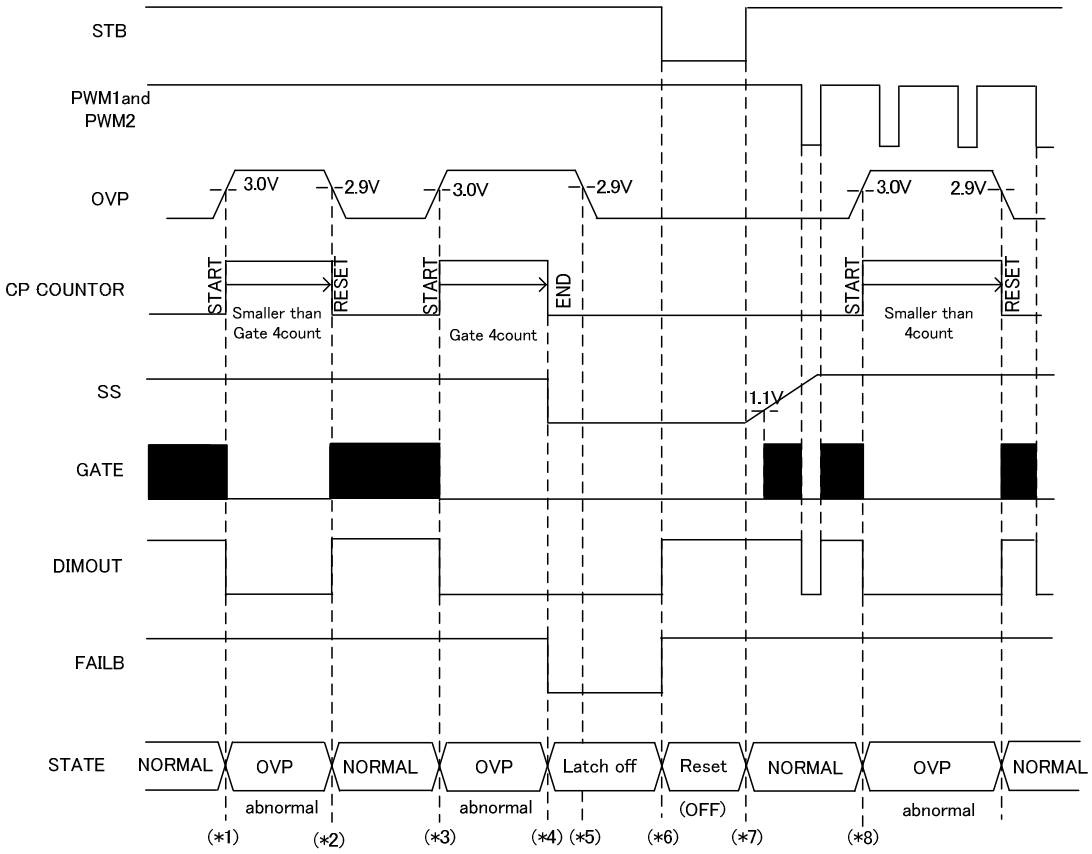
(*1)…As STB pin turns High to Low, BD9285F stops the boost operation, starts the discharge of TC54.
(*2)…During STB=L and V5UVLO=H, the DIMOUT asserts the same logic of PWM. TC54=5.4V is discharged until 2.4V by the constant current 10uA. And IC turns off. Vout need to be discharged adequately so that LED does not turns on drastically at the next start up.
For detailed instructions, please refer the section 3.4.2 “how to shutdown and set TC54 capacitance”

3.7.4 the soft start function



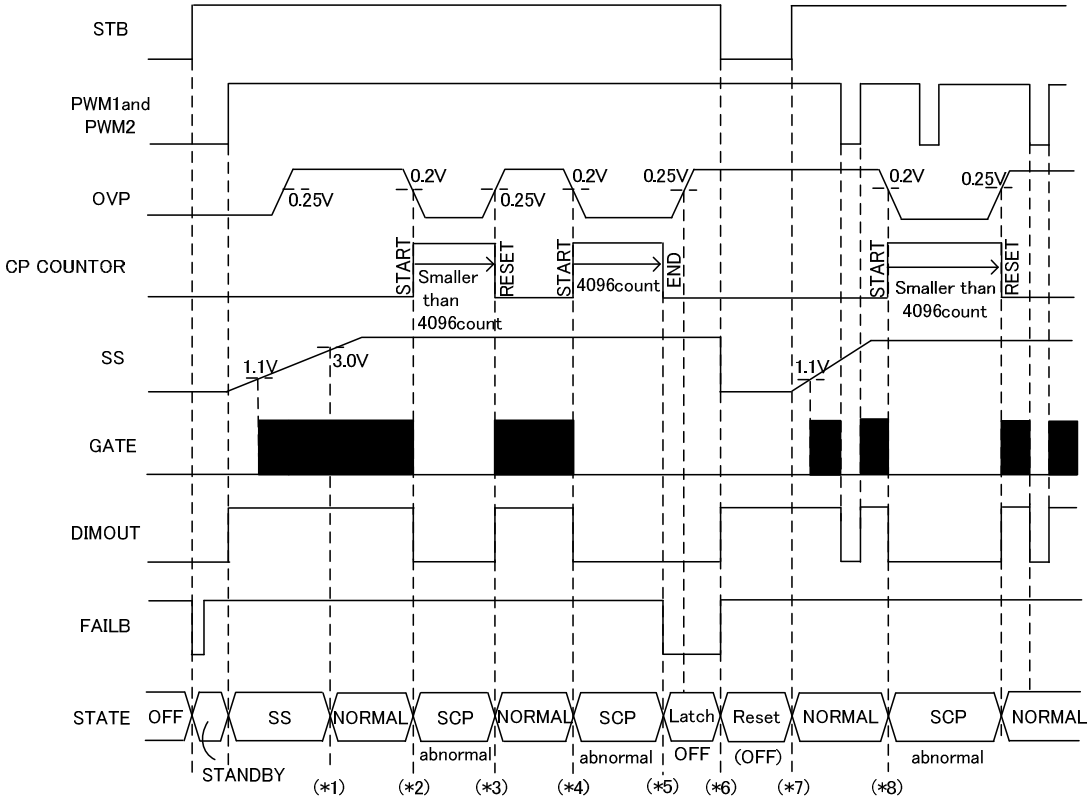
(*1)…The SS pin charge does not start by just STB=H. “PWM1=H and PWM2=H” is required to start the soft start. In the low SS voltage, the GATE pin duty is depend on the SS voltage. And as the SS is less than 1.1V, the pulse does not output.
(*2)…By the low STB=L, the SS pin is discharged immediately.
(*3)…As the STB recovered to STB=H, The SS charge starts immediately by the logic “PWM1 and PWM2=H” in this chart.
(*4)…The SS pin is discharged immediately by the UVLO=L.
(*5)…The SS pin is discharged immediately by the VCCUVLO=L
(*6)…The SS pin is discharged immediately by the TC54UVLO=L
(*7)…The SS pin is not discharged by the abnormal detection of the latch off type such as OVP until the latch off

3.7.5 the OVP detection



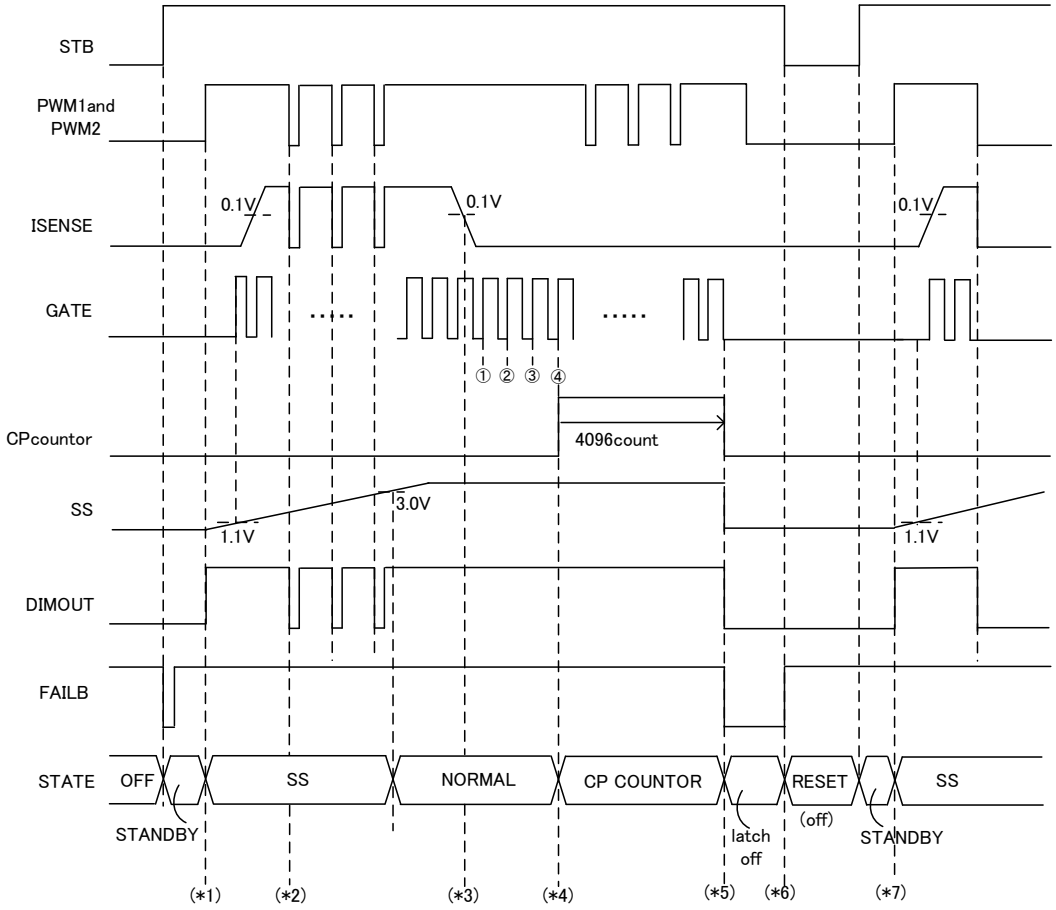
(*1)…As OVP is detected, the output GATE=L, DIMOUT=L, and the CP counter starts
(*2)…If OVP is released within 4 clock of CP counter of the GATE pin frequency, the boost operation restarts.
(*3)…As the OVP is detected again, the boost operation is stopped.
(*4)…As the OVP detection continues up to 4 count by the CP counter, IC will be latched off.
(*5)…As the latched off, the boost operation doesn't restart even if OVP is released.
(*6)…The STB=L input can make IC reset. In this chart, DIMOUT asserts high by the discharge function in the paragraph 3.7.3.
(*7)…It normally starts as STB turns L to H.
(*8)…The operation of the OVP detection is not related to the logic of PWM.

3.7.6 the SCP detection



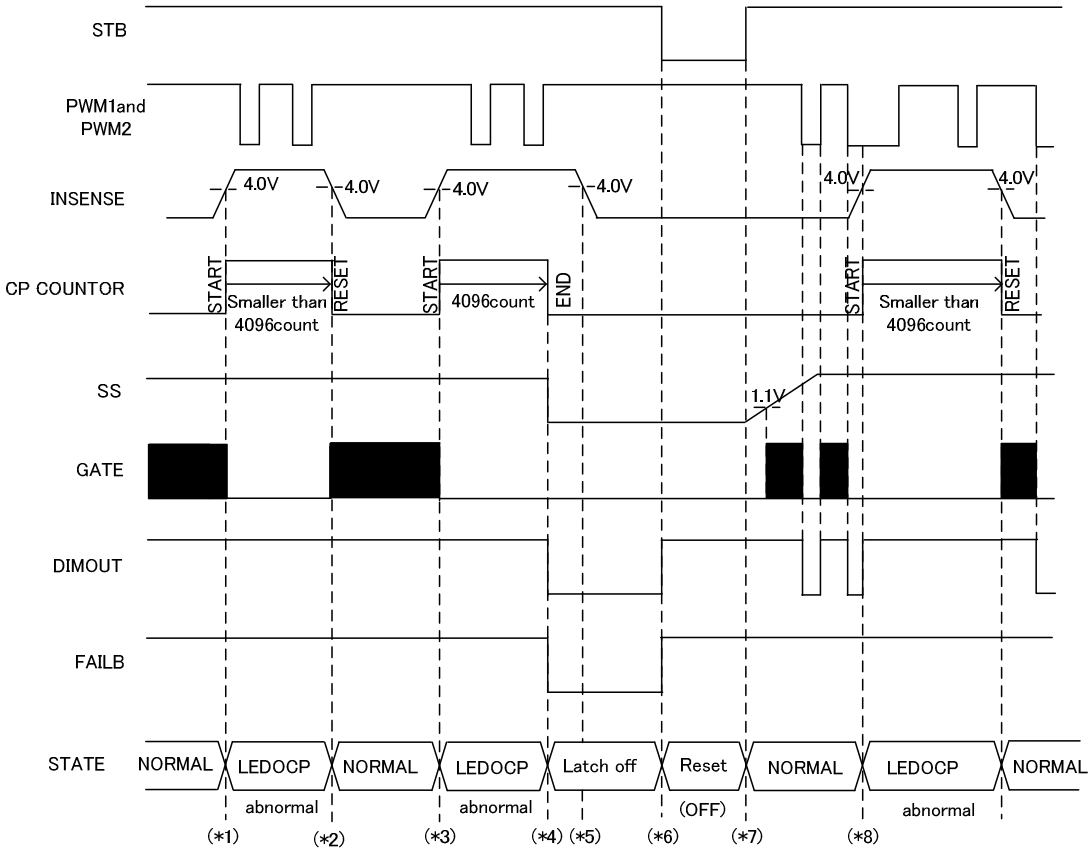
(*1)…During the soft start, the detection of SCP is masked.
(*2)…As SCP is detected, the output GATE=L, DIMOUT=L, and the CP counter starts
(*3)…If SCP is released within 4096 clock of CP counter of the GATE pin frequency, the boost operation restarts.
(*4)…As the SCP is detected again, the boost operation is stopped.
(*5)…As the SCP detection continues up to 4096 count by the CP counter, IC will be latched off.
(*6)…The STB=L input can make IC reset. In this chart, DIMOUT asserts high by the discharge function in the paragraph 3.7.3.
(*7)…It normally starts as STB turns L to H.
(*8)…The operation of the SCP detection is not related to the logic of PWM.

3.7.7 LED OPEN detection



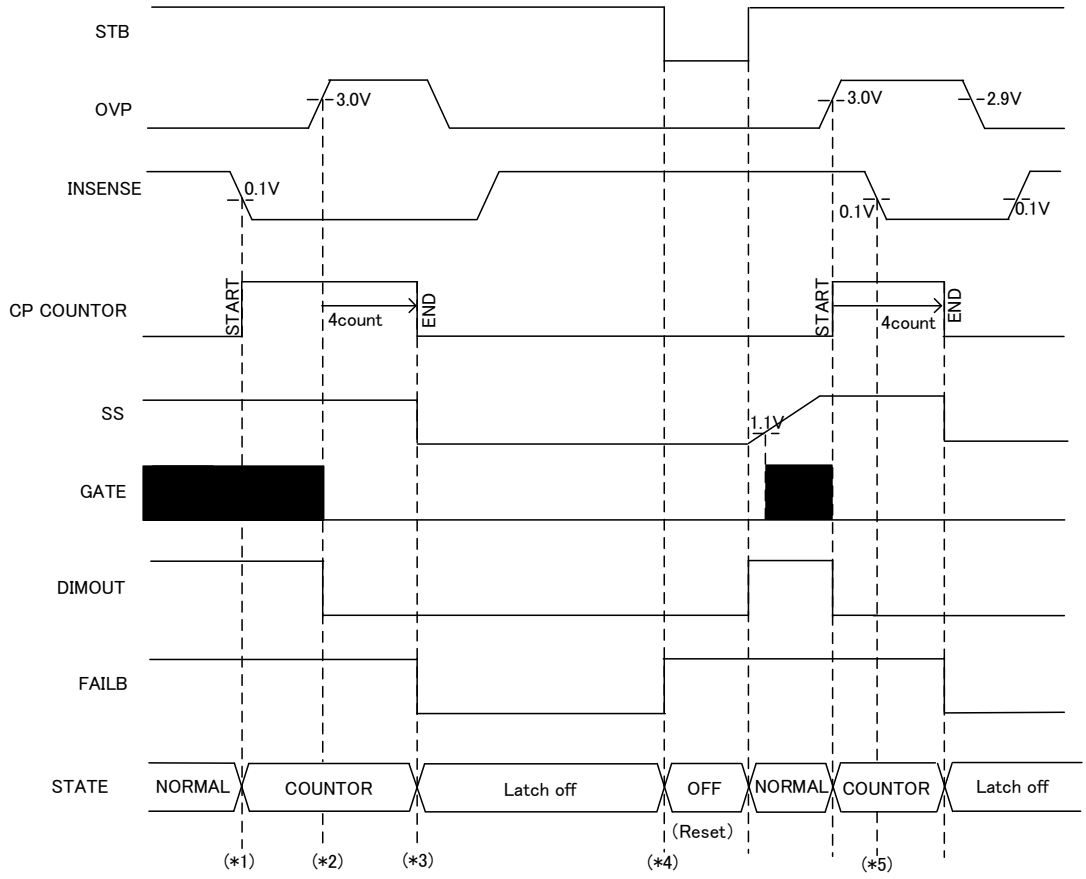
(*1)…During starting up, even if the normality, ISENSE<0.1V because of the low Vout. Therefore the OPEN detection will be masked for the soft start period.
(*2)…In the same way, as PWM=L, ISENSE<0.1V because of DIMOUT=L. OPEN will be masked, too.
(*3)…Though the OPEN is detected if ISENSE<0.1V as the PWM=H, it is not judged immediately to abnormal state. The behavior of GATE, FAILB keeps the normal operation.
(*4)…The CP counter will start if the OPEN detection continues 4 clock of the GATE frequency. To detect the OPEN state continuously, it compulsorily becomes DIMOUT=H regardless of the PWM logic.
(*5)…When the OPEN detection continues up to 4649 count with the CP counter, IC will be latched off. At this time, it asserts GATE=L, DIMOUT=L, FAILB=L for the first time.
(*6)…The latch off state can be reset by the STB=L.
(*7)…It normally starts by STB=L to H, in this figure.

3.7.8 LED OCP detection



(*1)…If ISENSE>4.0V, LEDOCP is detected, it becomes GATE=L. To detect LEDOCP continuously, The DIMOUT is compulsorily high, regardless of the PWM dimming signal.
(*2)…When the LEDOCP releases within the GATE frequency 4096 counts of the CP counter, the boost operation restarts.
(*3) …As the LEDOCP is detected again, the boost operation is stopped, too.
(*4)…If the LEDOCP detection continues up to 4096 count with the CP counter, IC will be latched off.
(*5)…Once IC is latched off, the boost operation doesn't restart even if the LEDOCP releases.
(*6)…The latch off state can be reset by the STB=L. In this chart, DIMOUT asserts high by the discharge function in the paragraph 3.7.3.
(*7)…It normally starts by STB=L to H.
(*8)…The operation of the LEDOCP detection is not related to the logic of the PWM.

3.7.9 the spontaneous detection OVP and OPEN.



(*1)…The time chart shows the OPEN detects faster and does not reach to the latch off state. The DIMOUT asserts high.
(*2)…If OPEN and OVP is detected spontaneously, OVP has the priority, and GATE=L, DIMOUT=L.
(*3)…IC will be latched off by the OVP factor.
(*4)…The latch off state is reset by the STB=L.
(*5)…The OVP has the priority too, in the case the OVP is detected first and the OPEN succeeds.

●Operational Notes

1.) This product is produced with strict quality control, but might be destroyed if used beyond its absolute maximum ratings including the range of applied voltage or operation temperature. Failure status such as short-circuit mode or open mode can not be estimated. If a special mode beyond the absolute maximum ratings is estimated, physical safety countermeasures like fuse needs to be provided.

2.) Connecting the power line to IC in reverse polarity (from that recommended) may cause damage to IC. For protection against damage caused by connection in reverse polarity, countermeasures, installation of a diode between external power source and IC power terminal, for example, needs to be taken.

3.) When this product is installed on a printed circuit board, attention needs to be paid to the orientation and position of IC. Wrong installation may cause damage to IC. Short circuit caused by problems like foreign particles entering between outputs or between an output and power GND also may cause damage.

4.) Since the back electromotive force of external coil causes regenerated current to return, countermeasures like installation of a capacitor between power source and GND as the path for regenerated current needs to be taken. The capacitance value must be determined after it is adequately verified that there is no problem in properties such that the capacity of electrolytic capacitor goes down at low temperatures. Thermal design needs to allow adequate margin in consideration of allowable loss (Pd) in actual operation state.

5.) The GND pin needs to be at the lowest potential in any operation state.

6.) Thermal design needs to be done with adequate margin in consideration of allowable loss (Pd) in actual operation state.

7.) Use in a strong magnetic field may cause malfunction.

8.) Output Tr needs to not exceed the absolute maximum rating and ASO while using this IC. As CMOS IC and IC which has several power sources may undergo instant flow of rush current at turn-on, attention needs to be paid to the capacitance of power source coupling, power source, and the width and run length of GND wire pattern.

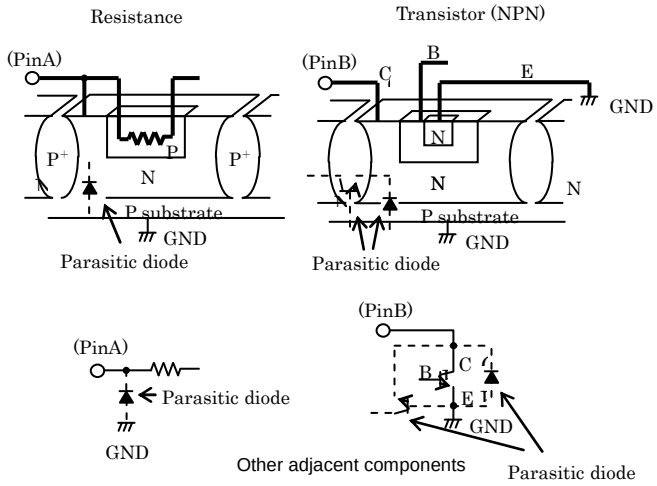
9.) This IC includes temperature protection circuit (TSD circuit). Temperature protection circuit (TSD circuit) strictly aims blockage of IC from thermal runaway, not protection or assurance of IC. Therefore use assuming continuous use and operation after this circuit is worked needs to not be done.

10.) As connection of a capacitor with a pin with low impedance at inspection of a set board may cause stress to IC, discharge needs to be performed every one process. Before a jig is connected to check a process, the power needs to be turned off absolutely. Before the jig is removed, as well, the power needs to be turned off.

11.) This IC is a monolithic IC which has P+ isolation for separation of elements and P board between elements.
A P-N junction is formed in this P layer and N layer of elements, composing various parasitic elements.
For example, a resistance and transistor are connected to a terminal as shown in the figure,

- ○ When GND>(Terminal A) in the resistance and when GND>(Terminal B) in the transistor (NPN), P-N junction operates as a parasitic diode.
- ○ When GND>(Terminal B) in the transistor (NPN), parasitic NPN transistor operates in N layer of other elements nearby the parasitic diode described before.

Parasitic elements are formed by the relation of potential inevitably in the structure of IC. Operation of parasitic elements can cause mutual interference among circuits , malfunction as well as damage. Therefore such use as will cause operation of parasitic elements like application of voltage on the input terminal lower than GND (P board) need to not be done.



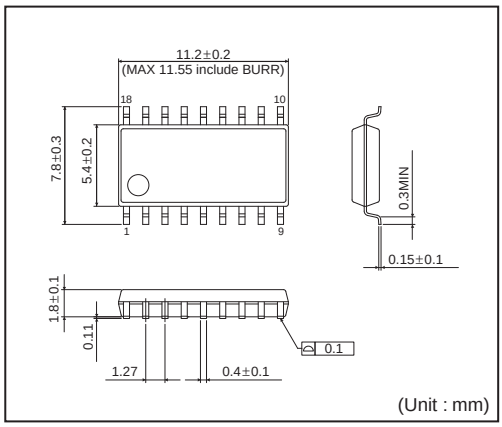
Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority

●Ordering Information

B D 9 2 8 5 F	XX
Part Number	Package F:SOP18
	Packaging and forming specification XX: Please confirm the formal name to our sales.

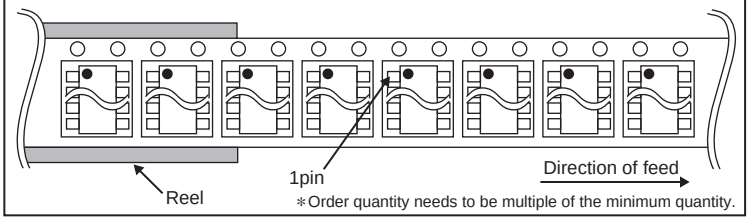
●Physical Dimension Tape and Reel Information

SOP18



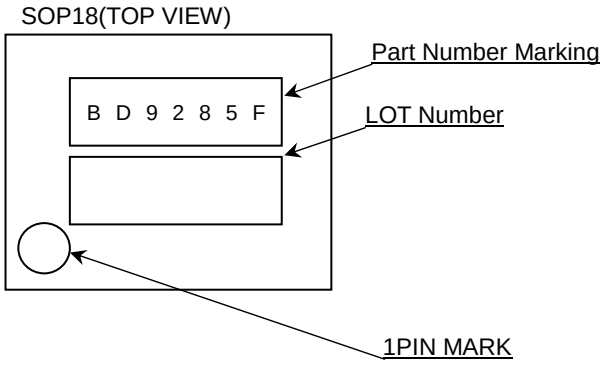
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram (TOP VIEW)



Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data. ROHM shall not be in any way responsible or liable for infringement of any intellectual property rights or other damages arising from use of such information or data.:

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Other Precaution

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General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

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