IS25CQ032

32M-BIT
3V- QUAD SERIAL FLASH MEMORY WITH MULTI-I/O SPI

DATA SHEET

32M-BIT
3V- QUAD SERIAL FLASH MEMORY MULTI- I/O SPI

FEATURES

- **Industry Standard Serial Interface**
  - IS25CQ032: 32M-bit/ 4M-byte
  - 256-bytes per Programmable Page Standard
  - Standard SPI/ Dual SPI/ Quad SPI
- **High Performance Serial Flash (SPI)**
  - 104 MHz SPI/ 80 MHz Dual or Quad SPI
  - 320 MHz equivalent Quad SPI
  - 40MB/S Continuous Data Throughput
  - Supports SPI Modes 0 and 3
  - More than 100,000 erase/program cycles(1)
  - More than 20-year data retention
- **Efficient Read and Program modes**
  - Low Instruction Overhead Operations
  - Continuous data read with Byte Wrap around
  - Allows XIP operations (execute in place)
  - Outperforms X16 Parallel Flash
- **Flexible & Cost Efficient Memory Architecture**
  - Uniform 4K-byte Sector Erase
  - Uniform 64K-byte Block Erase
  - Program from 1 to 256 bytes
  - Erase Suspend and Resume
- **Low Power with Wide Temp. Ranges**
  - Single 2.7V to 3.6V Voltage Supply
  - 10 mA Active Read Current
  - 5 µA Standby Current
  - Temp Grades:
    Extended: -40°C to +105°C

Advanced Security Protection

- Software and Hardware Write Protection
- 64-Byte dedicated area, user-lockable, One Time Programmable Memory (OTP)

- **Industry Standard Pin-out & Pb-Free Packages**
  - JM =16-pin SOIC 300mil
  - JB = 8-pin SOIC 208mil
  - JF = 8-pin VSOP 208mil
  - JK = 8-pin WSON 6x5mm
  - JL = 8-pin WSON 8x6mm
  - JG= 24-TFBGA (call factory)
  - KGD (call factory)

GENERAL DESCRIPTION

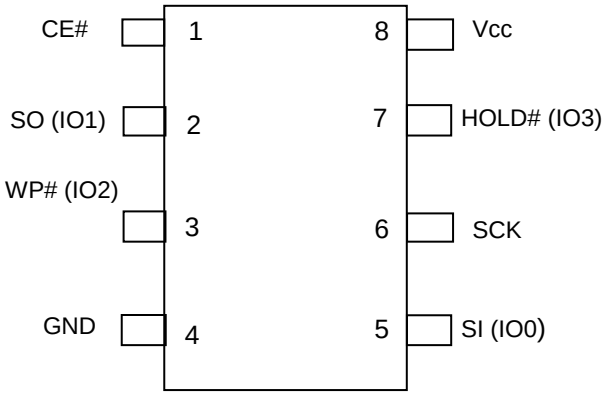
The IS25CQ032 (32M-bit) Serial Flash memory offers a storage solution with flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" is for systems that have limited space, pins, and power. The IS25CQ032 are accessed through a 4-wire SPI Interface consisting of a Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins, which also serve as multi-function I/O pins in Dual and Quad modes (see pin descriptions). The IS25xQ series of flash is ideal for code shadowing to RAM, execute in place (XIP) operations, and storing non-volatile data.

The memory array is organized into programmable pages of 256-bytes each. The IS25CQ032 supports page program mode where 1 to 256 bytes of data can be programmed into the memory with one command. Pages can be erased in groups of 4K-byte sectors, 64K-byte blocks, and/or the entire chip. The uniform 4K-byte sectors and 64K-byte blocks allow greater flexibility for a variety of applications requiring solid data retention.

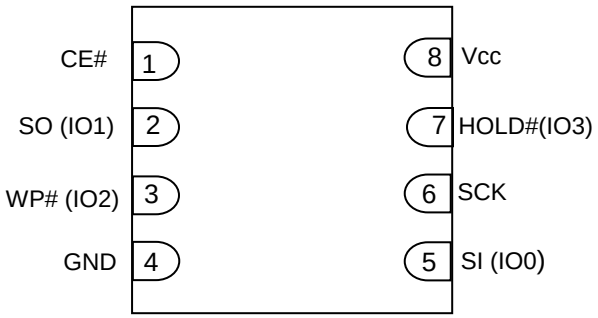
The device supports the standard Serial Peripheral Interface (SPI), Dual/Quad output (SPI), and Dual/Quad I/O (SPI). Clock frequencies of up to 104MHz and 80MHz for Dual/Quad I/O modes allow for equivalent clock rates of up to 320MHz (80MHz x 4) allowing up to 40MB/S of throughput. These transfer rates can outperform 16-bit Parallel Flash memories allowing for efficient memory access for a XIP (execute in place) operation.

The IS25CQ032 is manufactured using industry leading non-volatile memory technology. The devices are offered in industry standard lead-free packages. See Ordering Information for the density and package combinations available.

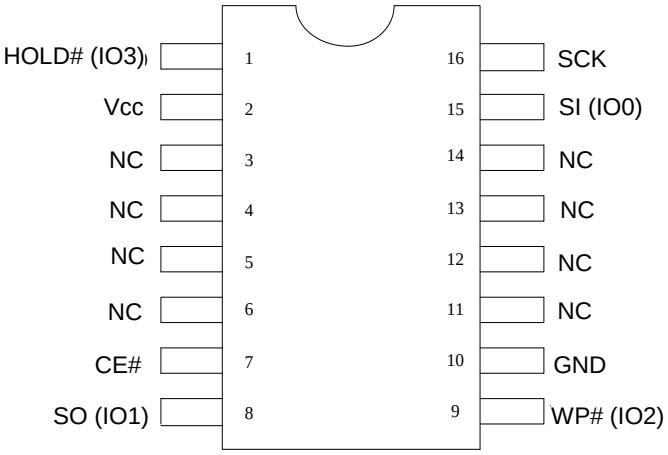
Connection Diagrams



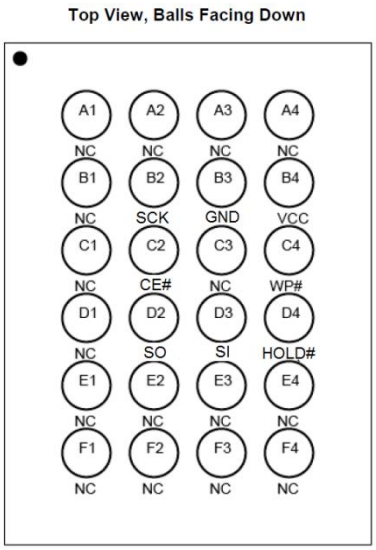
8-pin SOIC 208mil (Package: JB)
8-pin VSOP 208mil (Package: JF)



8-pin WSON 6x5mm (Package: JK)
8-pin WSON 8x6mm (Package: JL)



SOIC-16 300mil (Package: JM)



TFBGA-24 (Package: JG)

PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	**Chip Enable:** The Chip Enable (CE#) pin enables and disables the devices operation. When CE# is high the device is deselected and output pins are in a high impedance state. When deselected the devices non-critical internal circuitries power down to allow minimal levels of power consumption while in a standby state. When CE# is pulled low the device will be selected and brought out of standby mode. The device is considered active and instructions can be written to, data read, and written to the device. After power-up, CE# must transition from high to low before a new instruction will be accepted. Keeping CE# in a high state deselects the device and switches it into its low power state. Data will not be accepted when CE# is high.
SI (IO0), SO (IO1)	INPUT/OUTPUT	**Serial Data Input, Serial Output, and IOs (SI, SO, IO0, and IO1):** This device supports standard SPI, Dual SPI, and Quad SPI operation. Standard SPI instructions use the unidirectional SI (Serial Input) pin to write instructions, addresses, or data to the device on the rising edge of the Serial Clock (SCK). Standard SPI also uses the unidirectional SO (Serial Output) to read data or status from the device on the falling edge of the serial clock (SCK). In Dual and Quad SPI mode, SI and SO become bidirectional IO pins to write instructions, addresses or data to the device on the rising edge of the Serial Clock (SCK) and read data or status from the device on the falling edge of SCK. Quad SPI instructions use the WP# and HOLD# pins as IO2 and IO3 respectively.
WP# (IO2)	INPUT/OUTPUT	**Write Protect**: The WP# pin protects the Status Register from being written. When the WP# is low the status registers are write-protected and vice-versa for high. When the QE bit is set to "1", the WP**#** pin (Write Protect) function is not available since this pin is used for IO2.
HOLD# (IO3)	INPUT/OUTPUT	**Hold:** Pauses serial communication by the master device without resetting the serial sequence. When the QE bit of Status Register is set to "1", HOLD# pin is not available since it becomes IO3. The HOLD# pin allows the device to be paused while it is selected. The HOLD# pin is active low. When HOLD# is in a low state, and CE# is low, the SO pin will be at high impedance. Device operation can resume when HOLD# pin is brought to a high state. When the QE bit of Status Register is set for Quad I/O, the HOLD# pin function is not available and becomes IO3 for Multi-I/O SPI mode.
SCK	INPUT	**Serial Data Clock:** Synchronized Clock for input and output timing operations.
Vcc	POWER	**Power:** Device Core Power Supply
GND	GROUND	**Ground:** Connect to ground when referenced to Vcc
NC	Unused	**NC:** Pins labeled "NC" stand for "No Connect" and should be left uncommitted.

Table 1. Pin Descriptions

BLOCK DIAGRAM

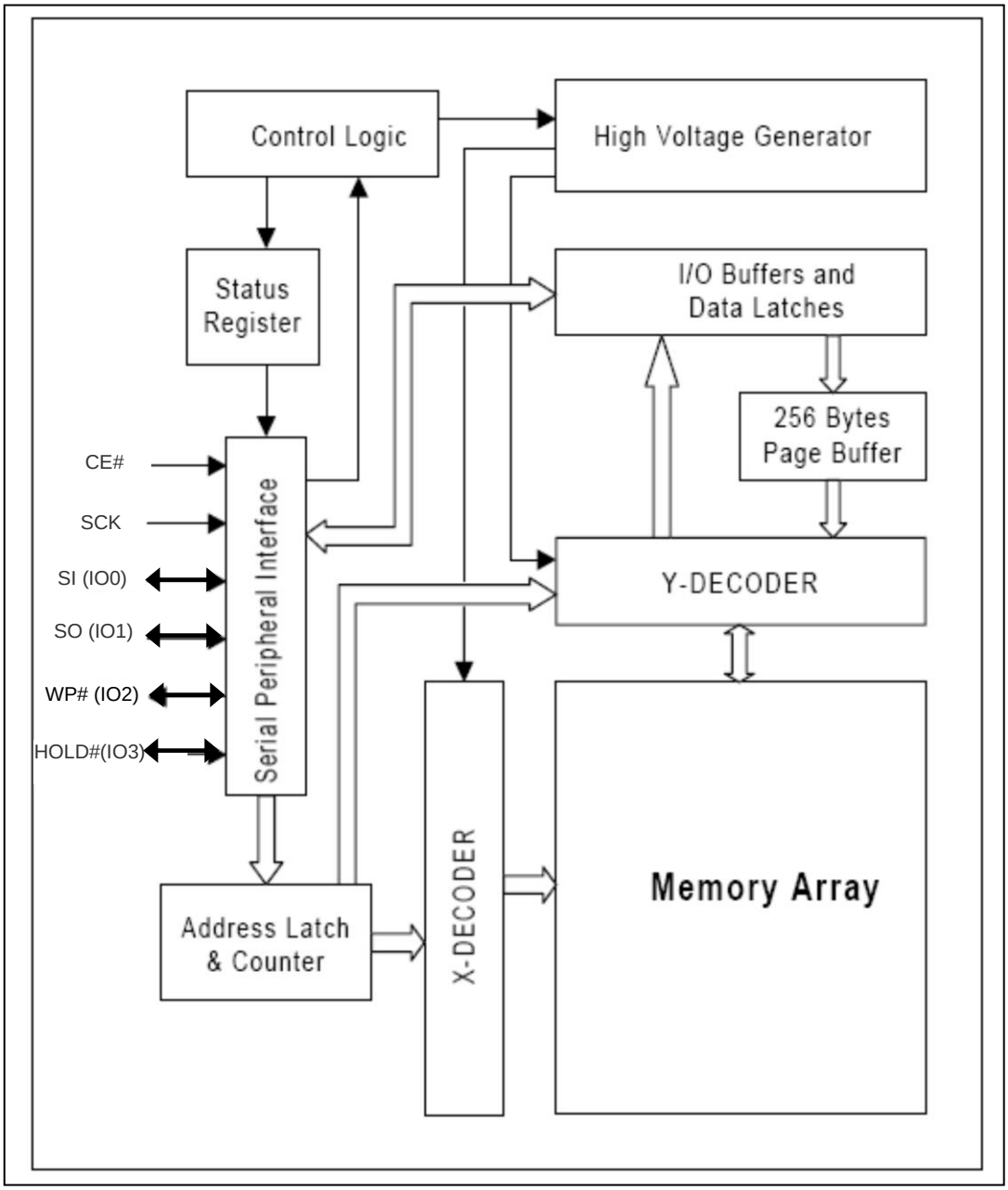


Figure 1. Flash Block Diagram

MEMORY CONFIGURATION

Table 2 below illustrates the memory architecture of the device and its block and sector addresses.

Memory Density	Block No.	Block Size (Kbytes)	Sector No.	Sector Size (Kbytes)	Address Range
32Mbit	Block 0	64	Sector 0	4	000000h - 000FFFh
			Sector 1	4	001000h - 001FFFh
			:	:	:
			Sector 15	4	00F000h - 00FFFFh
	Block 1	64	Sector 16	4	010000h - 010FFFh
			Sector 17	4	011000h - 011FFFh
			:	:	:
			Sector 31	4	01F000h - 01FFFFh
	:	:	:	:	:
	Block 7	64	Sector 127	4	070000h – 07FFFFh
	Block 8	64	Sector 128	4	080000h – 08FFFFh
	:	:	:	:	:
	:	:	:	:	:
	Block 15	64	Sector 255	4	0F0000h – 0FFFFFh
	Block 16	64	Sector 256	4	100000h – 10FFFFh
	:	:	:	:	:
	:	:	:	:	:
	Block 31	64	Sector511	4	1F0000h – 1FFFFFh
	Block 32	64	Sector 512	4	200000h – 20FFFFh
	:	:	:	:	:
	:	:	:	:	:
	Block 63	64	Sector 1023	4	3FF000h – 3FFFFFh

Table 2. Block/Sector Addresses of IS25CQ032

REGISTERS

STATUS REGISTER

Refer to Tables 3 and 4 for Status Register Format and Status Register Bit Definitions.

The BP3, BP2, BP1, BP0, QE, and SRWD are non-volatile memory cells that can be written by a Write Status Register (WRSR) instruction. The default value

of the BP3, BP2, BP1, BP0, QE and SRWD bits are set to “0” from the factory. The Status Register can be read by the Read Status Register (RDSR). Refer to Table 8 for the Instruction Set.

The function of Status Register bits are described as follows:

WIP bit: The Write in Progress (WIP) bit is read-only, and can be used to detect the progress or completion of a program or erase operation. When the WIP bit is “0”, the device is ready for a write status register, program or erase operation. When the WIP bit is “1”, the device is busy.

WEL bit: The Write Enable Latch (WEL) bit indicates the status of the internal write enable latch. When the WEL is “0”, the write enable latch is disabled, and all write operations, including write status register, page program, sector erase, block and chip erase operations are inhibited. When the WEL bit is “1”, write operations are allowed. The WEL bit is set by a Write Enable (WREN) instruction. Each write register, program and erase instruction must be preceded by a WREN instruction. The WEL bit can be reset by a Write Disable (WRDI) instruction. It will automatically reset after the completion of a write instruction.

BP3, BP2, BP1, BP0 bits: The Block Protection (BP3, BP2, BP1 and BP0) bits are used to define which memory portion of the entire memory area should be protected. Refer to Table 5 for the Block Write Protection bit settings. When a defined combination of BP3, BP2, BP1 and BP0 bits are set, the corresponding memory area is protected. Any program or erase operations to that area will be inhibited.

Note: Chip Erase (CHIP_ER) instruction can be executed only if the Block Protection Bits are not set and locked

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SRWD bit: The Status Register Write Disable (SRWD) bits operate in conjunction with the Write Protection (WP#) signal to provide a Hardware Protection Mode. When the SRWD is set to “0”, the Status Register is not write-protected. When the SRWD is set to “1” and the WP# is pulled low (V_{IL}), the bits of Status Register (SRWD, BP3, BP2, BP1, BP0) become read-only, and a WRSR instruction will be ignored. If the SRWD is set to “1” and WP# is pulled high (V_{IH}), the Status Register can be changed by a WRSR instruction.

QE bit: The Quad Enable (QE) is a non-volatile bit in the status register that allows Quad operation. When the QE bit is set to “0”, the pin WP# and HOLD# are enable. When the QE bit is set to “1”, the pin IO2 and IO3 are enable.

WARNING: The QE bit should never be set to a 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground.

Status Register	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	SRWD	QE	BP3	BP2	BP1	BP0	WEL	WIP
Default values	0	0	0	0	0	0	0	0

***** The default value of the SRWD, QE, BP3, BP2, BP1, and BP0 are set to “0” from the factory.
Table 3. Status Register Format

Bit	**Name**	**Definition**	**Read/Write**	**Non-Volatile bit**
Bit 0	WIP	Write In Progress Bit: "0" indicates the device is ready "1" indicates a write cycle is in progress and the device is busy	R	No
Bit 1	WEL	Write Enable Latch: "0" indicates the device is not write enabled (default) "1" indicates the device is write enabled	R/W	No

Bit 2	BP0	Block Protection Bit: (Table 5) "0" indicates the specific blocks are not write-protected (default) "1" indicates the specific blocks are write-protected	R/W	Yes
Bit 3	BP1			
Bit 4	BP2			
Bit 5	BP3			
Bit 6	QE	Quad Enable bit: “0” indicates the Quad output function is disabled (default) “1” indicates the Quad output function is enabled	R/W	Yes
Bit 7	SRWD	Status Register Write Disable: (See Table 3) "0" indicates the Status Register is not write-protected (default) "1" indicates the Status Register is write-protected	R/W	Yes

Table 4. Status Register Bit Definition

Status Register Bits				32 Mbit- Protected Memory Area	
BP3	**BP2**	**BP1**	**BP0**	**Protected Blocks**	**Protected Portion**
0	0	0	0	None	None
0	0	0	1	63	Upper 1/64
0	0	1	0	62 and 63	Upper 1/32
0	0	1	1	60 to 63	Upper 1/16
0	1	0	0	56 to 63	Upper 1/8
0	1	0	1	48 to 63	Upper 1/4
0	1	1	0	32 to 63	Upper 1/2
0	1	1	1	0-63 (ALL)	ALL
1	0	0	0	None	None
1	0	0	1	0	Lower 1/64
1	0	1	0	0 and 1	Lower 1/32
1	0	1	1	0 to 3	Lower 1/16
1	1	0	0	0 to 7	Lower 1/8
1	1	0	1	0 to 15	Lower 1/4
1	1	1	0	0 to 31	Lower 1/2
1	1	1	1	0-63 (ALL)	ALL

Table 5. Block Write Protect Bits for IS25CQ032

PROTECTION MODE

There are two types of write-protection mechanisms: hardware and software. Both are used to prevent incorrect operation in a possibly noisy environment where data integrity cannot be guaranteed.

HARDWARE WRITE-PROTECTION

The devices provide two hardware write-protection features:

a. When inputting a program, erase or write status register instruction, the number of clock pulses is checked to determine whether it is a multiple of eight before executing. Any incomplete instruction command sequence will be ignored.

b. Write inhibit is 2.1V, all write sequence will be ignored when Vcc drops below 2.1V.

c. The Write Protection (WP#) pin provides a hardware write protection method for BP3, BP2,

BP1, BP0 and SRWD in the Status Register. Refer to the STATUS REGISTER description.

SOFTWARE WRITE PROTECTION

There are two types of software write protection features:

a. Before the execution of any program, erase or write status register instruction, the Write Enable Latch (WEL) bit must be enabled by executing a Write Enable (WREN) instruction. If the WEL bit is not enabled first, the program, erase or write register instruction will be ignored.

b. The Block Protection (BP3, BP2, BP1, BP0) bits can control whether the entire memory area or just a partial portion is write-protected.

SRWD	WP#	Status Register
0	Low	Writable
1	Low	Protected
0	High	Writable
1	High	Writable

Table 6. Hardware Write Protection on Status Register

SPI INSTRUCTIONS AND DEVICE OPERATION

The instruction set for controlling the device is located in table 8 and can be fully controlled through the SPI bus. Instructions can be initiated with the falling edge of Chip Enable (CE#). The first byte of data clocked into the SI pin provides the instruction code. Data on the SI pin is sampled by SCKs (serial clock) rising edge with the most significant bit (MSB) read first.

Instructions vary in length (bytes) and may be followed by address bytes, data bytes, and or dummy bytes (don't care). Sometimes the instruction will require a combination of commands to perform the function.

Instructions are read on the rising edge of SCK. A full 8-bits must be clocked with CE# pulled high at the byte boundary before any command is accepted (expect for read).

Read instructions can be completed after any clocked bit. This design feature protects the device from unwanted writes. The timing for each instruction is illustrated in the following figures.

Table 7 contains the Manufacturing and Device IDs.

Product Identification		**Hex Code**
Manufacturer ID	Manufacture ID1	9Dh
	Manufacture ID2	7Fh
Device ID: IS25CQ032	Device ID1	15h
	Device ID2	46h

Table 7. Manufacture and Device Identification

Instruction Name	Hex Code	Operation	Command Cycle*	Maximum Frequency
RDID	ABh	Read Device ID and Release from power down	4 Bytes	80 MHz
JEDEC ID READ	9Fh	JEDEC ID Read- Manufacturer and Device ID	1 Byte	80 MHz
RDMDID	90h	Read Manufacturer and Device ID	4 Bytes	80 MHz
WREN	06h	Write Enable	1 Byte	80 MHz
WRDI	04h	Write Disable	1 Byte	80 MHz
RDSR	05h	Read Status Register	1 Byte	80 MHz
WRSR	01h	Write Status Register	2 Bytes	80 MHz
READ	03h	Read Data Bytes from Memory at Normal Read Mode	4 Bytes	33 MHz
FAST_READ	0Bh	Read Data Bytes from Memory at Fast Read Mode	5 Bytes	104 MHz
FRDO	3Bh	Fast Read Dual Output	5 Bytes	80 MHz
FRDIO	BBh	Fast Read Dual I/O	3 Bytes	80MHz
FRQO	6Bh	Fast Read Quad Output	5 Bytes	80 MHz
FRQIO	EBh	Fast Read Quad I/O	2 Bytes	80MHz
MR	FFh	Mode Reset	2 Byte	80MHz
PAGE_ PROG	02h	Page Program Data Bytes Into Memory	4 Bytes + 256B	80 MHz
SECTOR_ER	D7h/20h	Sector Erase	4 Bytes	80 MHz
BLOCK_ER	D8h	Block Erase	4 Bytes	80 MHz
CHIP_ER	C7h/60h	Chip Erase	1 Byte	80 MHz
Quad page program	32h	Page Program Data Bytes Into Memory with Quad interface	4 Bytes + 256B	80 MHz
Erase suspend	75h	Interrupts the system to pause an erase command	1 Byte	80 MHz
Erase resume	7Ah	Resumes the erase command	1 Byte	80 MHz
PSIR	B1h	Program One Time Programmable Area (OTP)	4 Bytes + 65 bytes	80 MHz
RSIR	4Bh	Read One Time Programmable Area (OTP)	4 Bytes	33 MHz

Table 8. Instruction Set

***Note 1. Command Cycle includes Instruction Byte**

HOLD OPERATION

The HOLD# pin In SPI and Dual SPI mode allow an operation to be paused while it is actively selected (CE# is low).

The HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. See example below, Configuring Multiple SPI Devices and Modes (0 or 3).

The HOLD function is only available for SPI and Dual SPI operations. To initiate a HOLD operation, the device must be selected (CE# set low) and HOLD# pin pulled low. The HOLD operation will activate on the falling edge of the HOLD# signal if SCK is already low. If the SCK is not already low the HOLD condition will begin at the next falling edge of SCK. Inputs to SI will be ignored and SO will be in a high impedance state. The HOLD condition will terminate on the rising edge of the HOLD# signal if SCK signal is already low, if not, HOLD condition will terminate at the next SCK falling edge. The paused operation can now continue.

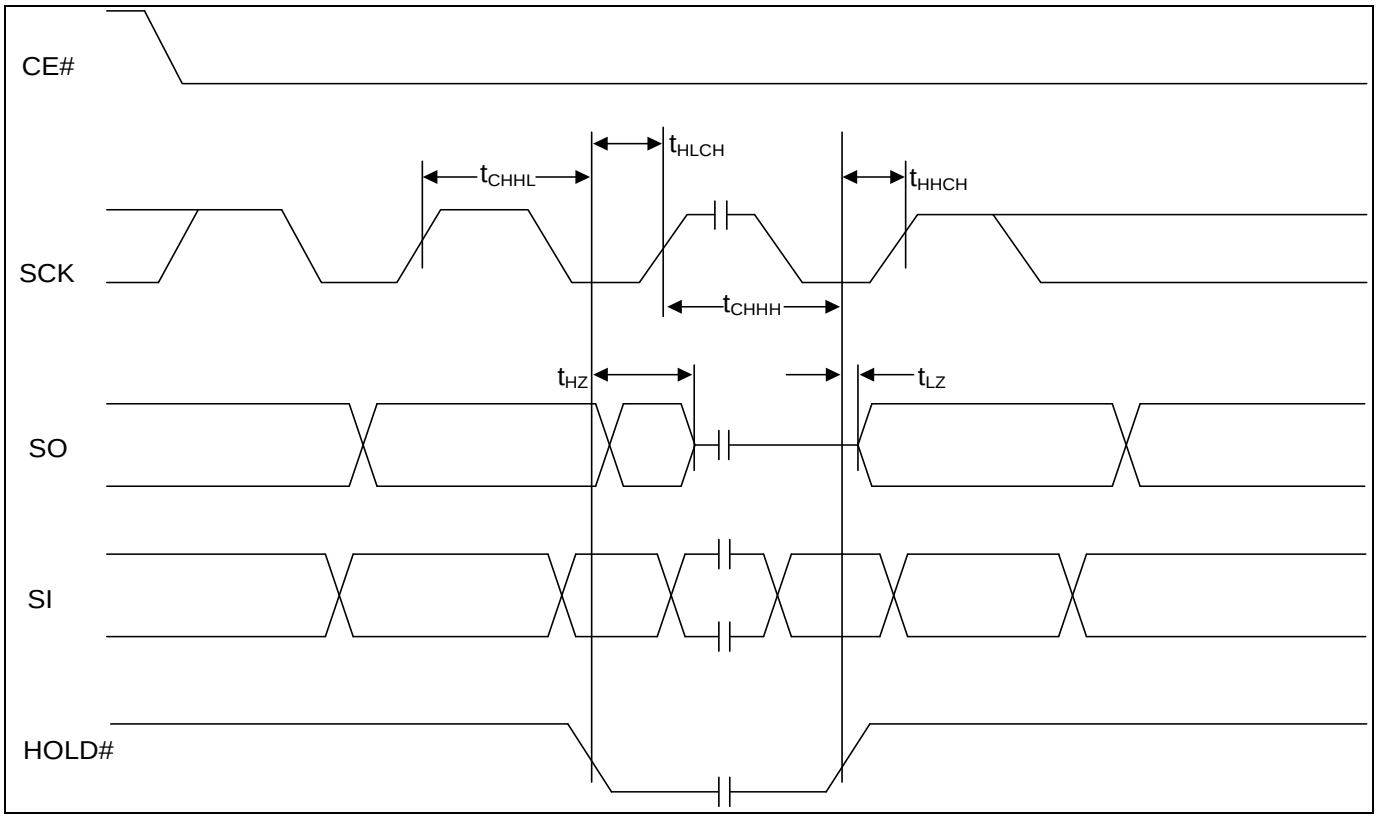


Figure 2. HOLD Timing Diagram

CONFIGURING MULTIPLE SPI DEVICES & MODE 0 AND 3 COMPATIBLE

Multiple devices can be connected together on the SPI serial bus and controlled by a SPI Master controller. Figures 3 and 4 shows how a microcontroller can be connected to control multiple SPI devices.

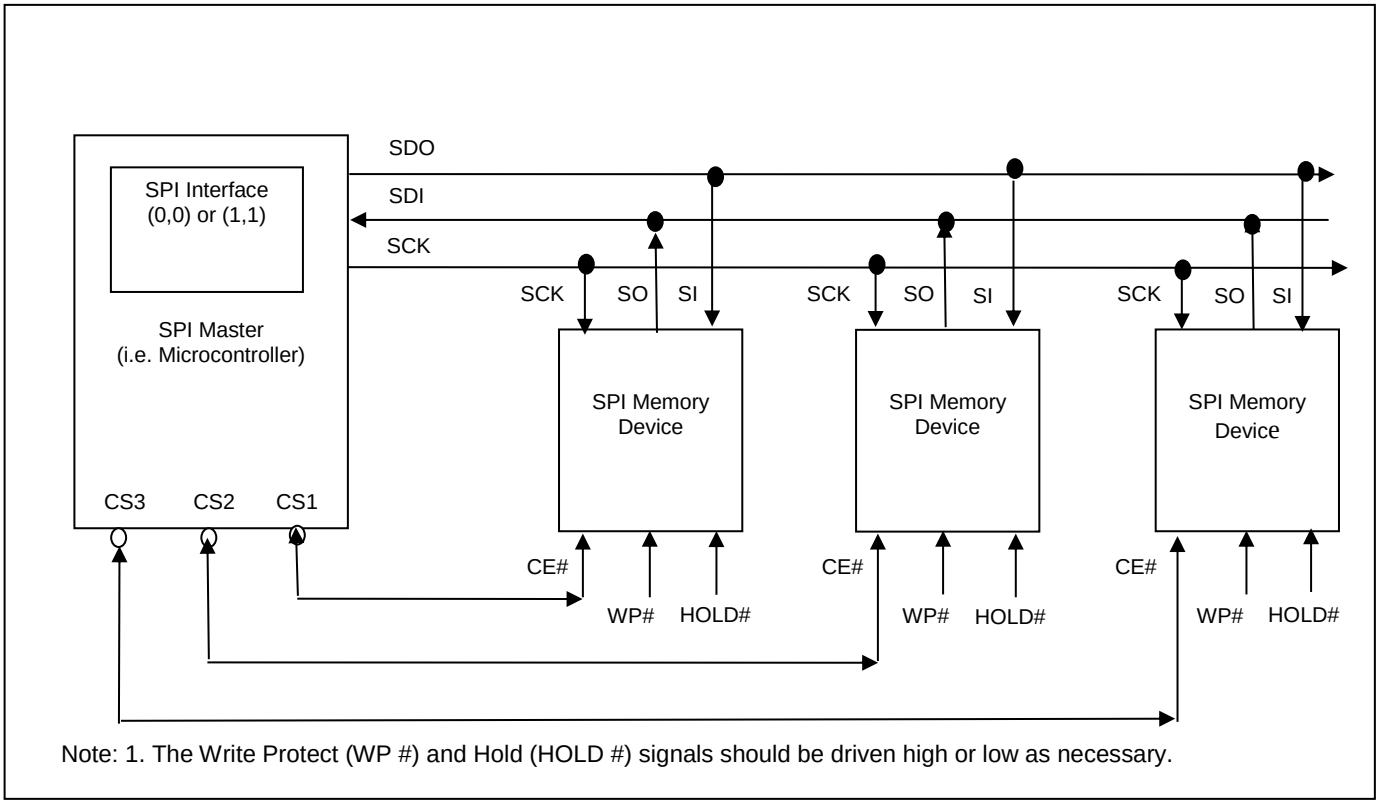
SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 is the normal state of the SCK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash.

For Mode 0 the CLK signal is normally low on the falling and rising edges of CE#. For Mode 3 the CLK signal is normally high on the falling and rising edges of CE#. The serial clock remains at “0” (SCK = 0) for Mode 0 and for Mode 3 the clock remains at “1” (SCK = 1).

Refer to Figure 3 and 4.

In both modes, the input data is latched on the rising edge of Serial Clock (SCK), and the output data is available from the falling edge of SCK.

These devices are designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of any controller equipped with a SPI interface.



Note: 1. The Write Protect (WP #) and Hold (HOLD #) signals should be driven high or low as necessary.

Figure 3. Conceptual Diagram using an SPI Master with Multiple SPI Flash Memory Devices

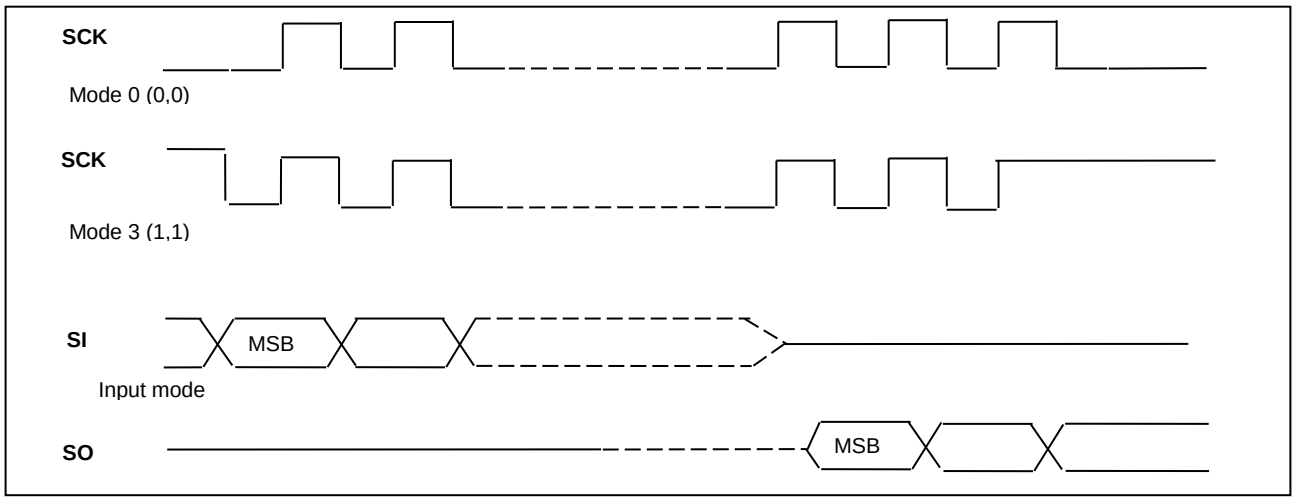


Figure 4. SPI Mode 0 and 3

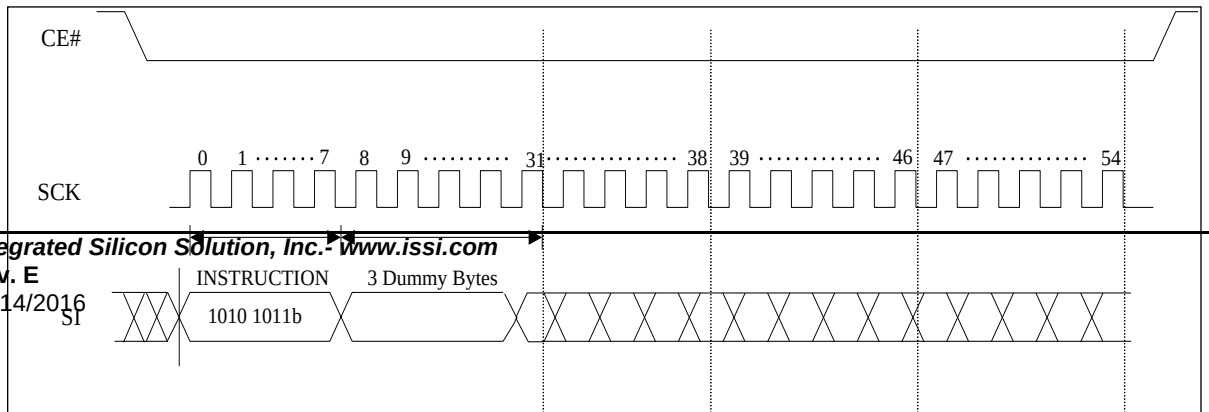
RDID (ABh): READ DEVICE ID AND RELEASE FROM POWER-DOWN

The read device identification (RDID) instruction is for reading out an 8-bit Electronic Signature whose value is shown in Table 7 as Device ID1. The RDID instruction code is followed by three dummy bytes, for a total of four command cycles, each bit being latched-in on SI during the rising edge of SCK. Then Device ID1 is shifted out on SO with the MSB first, each bit being shifted out during the falling edge of SCK. The RDID instruction is ended when CE# goes high. Device ID1 outputs repeatedly if clock cycles continue on SCK and CE# is held low. To release the device from the RDID instruction, drive CE# high as shown in figure 5.

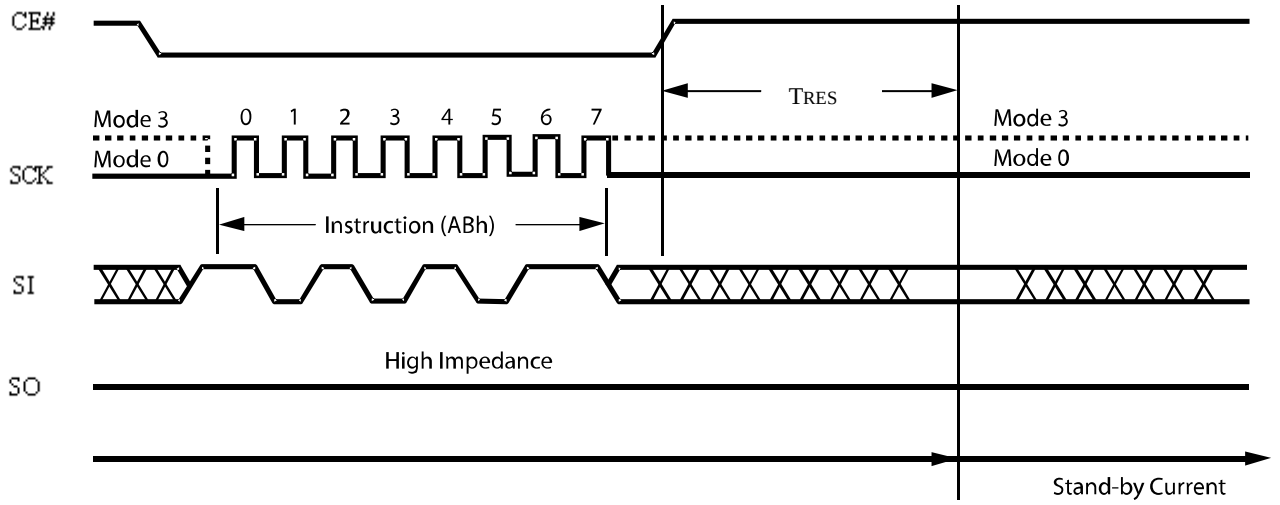
The RDID instruction can also release the device from the power-down state. It is a multi-purpose instruction. To release the device from the power-down state, the instruction is issued by driving the CE# pin low and shifting the instruction code “ABh” and driving CE# high. The CE# pin must remain high during the t_{RES} time duration before the device will resume normal operation and other instructions are accepted.

If the Release from Power-down instruction is issued while an Erase, Program or Write cycle is in process the instruction is ignored and will not have any effects on the current cycle.

The JEDEC ID read instruction is recommended for new designs.



Read Device ID



Release from Power-Down

Figure 5. Read Device ID (Top Diagram) and Release from Power-Down (Bottom Diagram)

JEDEC ID READ (9Fh): Read Manufacture Product Identification by JEDEC ID

For compatibility reasons several instructions are available for electronically obtaining the identity of the device. The JEDEC ID read command was adopted to allow compatibility and identification.

This instruction is initiated by driving the CE# pin low and shifting the instruction code “9Fh”. The JEDEC ID READ instruction allows the user to read Manufacturer

ID1, Manufacturer ID2, and Device ID2.
The command shifts out the most significant bit on the falling edge of SCK.

If CE# stays low after the last bit of Device ID2 the electronic identification is repeated continuously until CE# is pulled high.

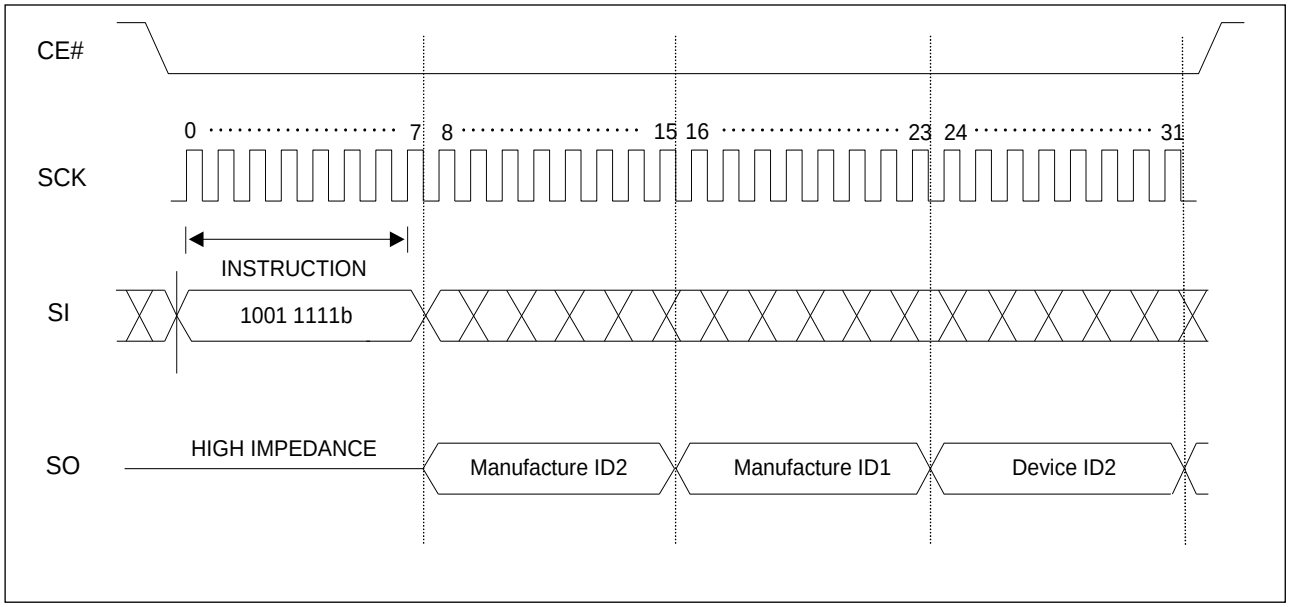


Figure 6. Read Product Identification by JEDEC ID READ Sequence

RDMDID (90h): READ DEVICE MANUFACTURER AND DEVICE ID OPERATION

The Read Device Manufacturer and Device ID instruction is very similar to the RDID instruction. The RDMDID instruction is initiated by driving the CE# pin low and shifting the instruction code “90h” followed by three bytes. Two dummy bytes plus one address byte (A7~A0), each bit being latched-in on SI during the rising edge of SCK.

The Manufacture and Device ID can be read continuously, alternating from one to the others. The instruction is completed by driving CE# high.

If the last bit (A7~A0) is initially set to 0, then Manufacture ID1 -> Device ID1 -> Manufacture ID2 is shifted out on SO with the MSB first. Each bit shifted out during the falling edge of SCK. If A0 = 1, then the output sequence becomes Device ID1 -> Manufacture ID1 -> Manufacture ID2.

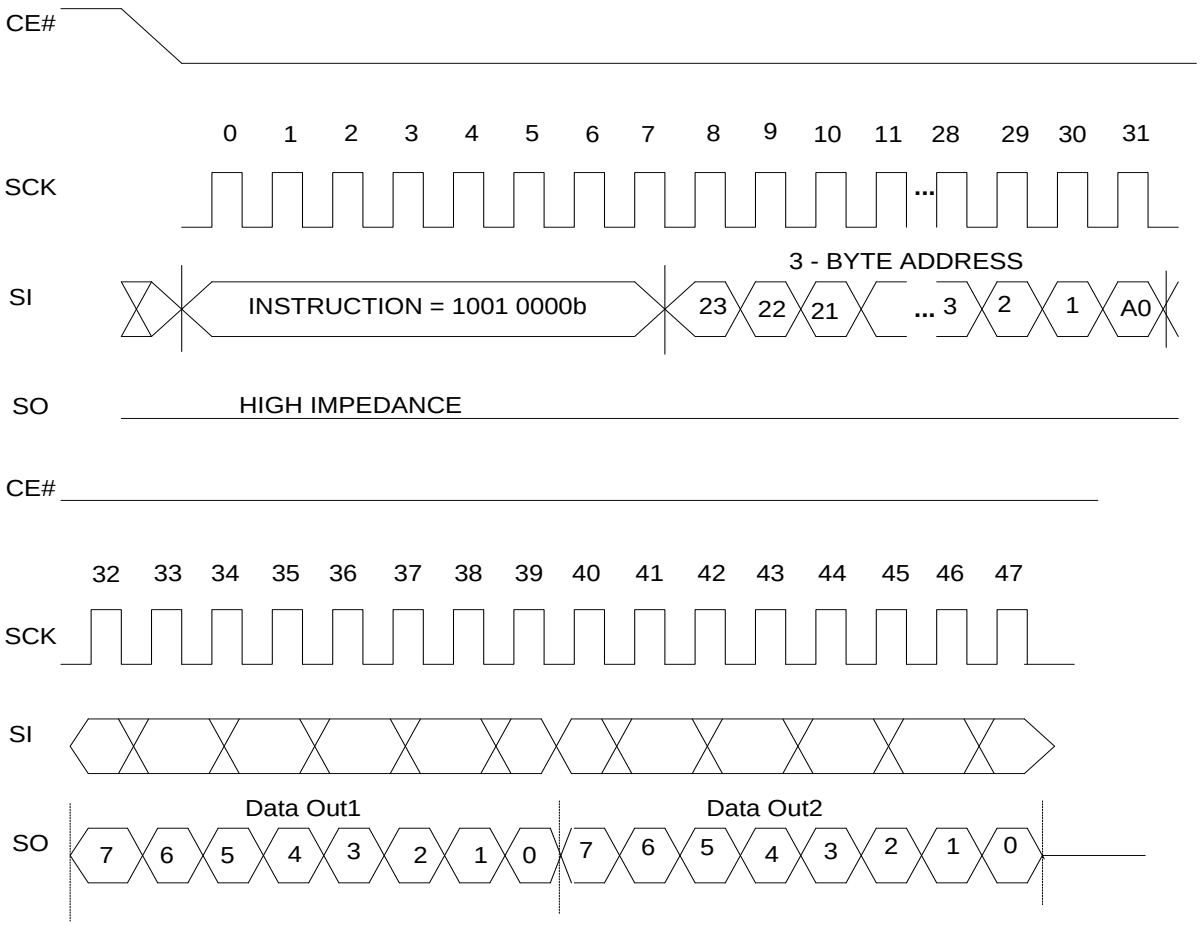


Figure 7. Read Product Identification by RDMDID READ Sequence

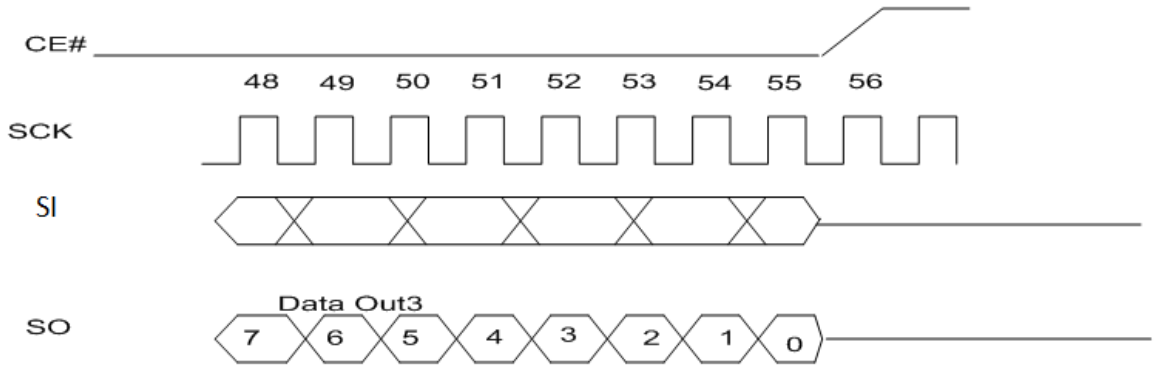


Figure 7. (cont.) Read Product Identification by RDMDID READ Sequence

Note : 1. ADDRESS A0 = 0, will output the Manufacture ID1 -> Device ID1 -> Manufacture ID2
2. ADDRESS A0 = 1, will output the Device ID1 -> Manufacture ID1 -> Manufacture ID2

WREN (06h): WRITE ENABLE OPERATION

The Write Enable (WREN) instruction is used to set the Write Enable Latch (WEL) bit. The WEL bit is reset to the write protected state after power-up. The WEL bit must be write enabled before any write operation, including sector, block erase, chip erase, page program, and write status register. The WEL bit will be reset to the write-protect state automatically upon completion of a write operation. The WREN instruction is required before any above operation is executed.

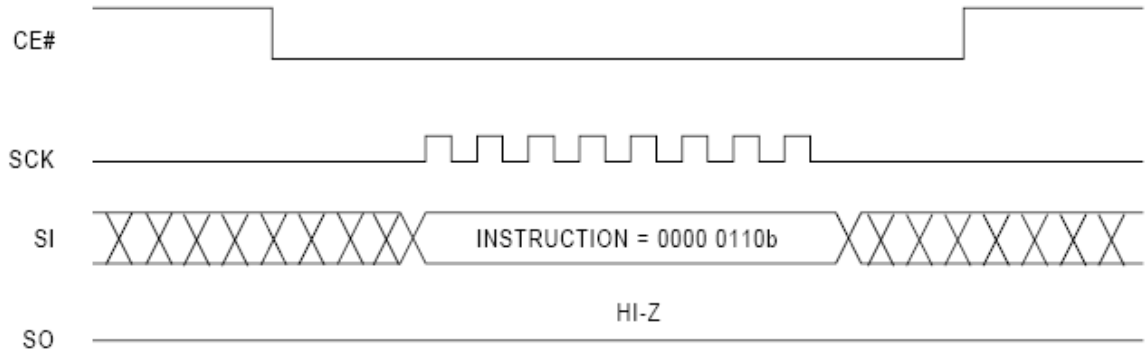


Figure 8. Write Enable Sequence

WRDI (04h): WRITE DISABLE OPERATION

The Write Disable instruction resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving CE# low, shifting the instruction code “04h” into the SI pin and then driving CE# high. The WEL bit is automatically reset after power-up and upon completion of the Write Status Register, Page Program, Quad Page Program, Sector Erase, Block Erase and Chip Erase.

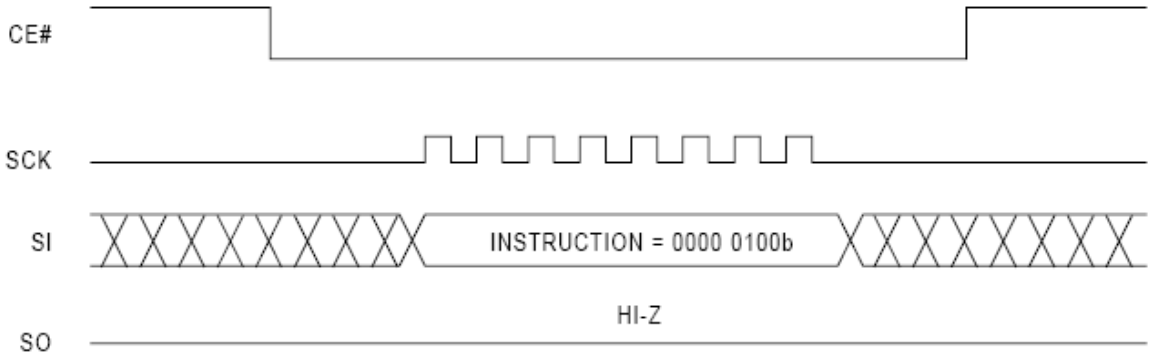


Figure 9. Write Disable Sequence

RDSR (05h): READ STATUS REGISTER OPERATION

The Read Status Register (RDSR) instruction provides access to the Status Register. During the execution of a program, erase or write status register operation, all other instructions will be ignored except the RDSR instruction, which can be used to check the progress or completion of an operation by reading the WIP bit of the Status Register.

The instruction is entered by driving CE# low and shifting the instruction code “05h”into the SI pin on the rising edge of SCK. The status register bits are then shifted out on the SO pin at the falling edge of SCK with most significant bit (MSB) first.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the WIP status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously. The instruction is completed by driving CE# high.

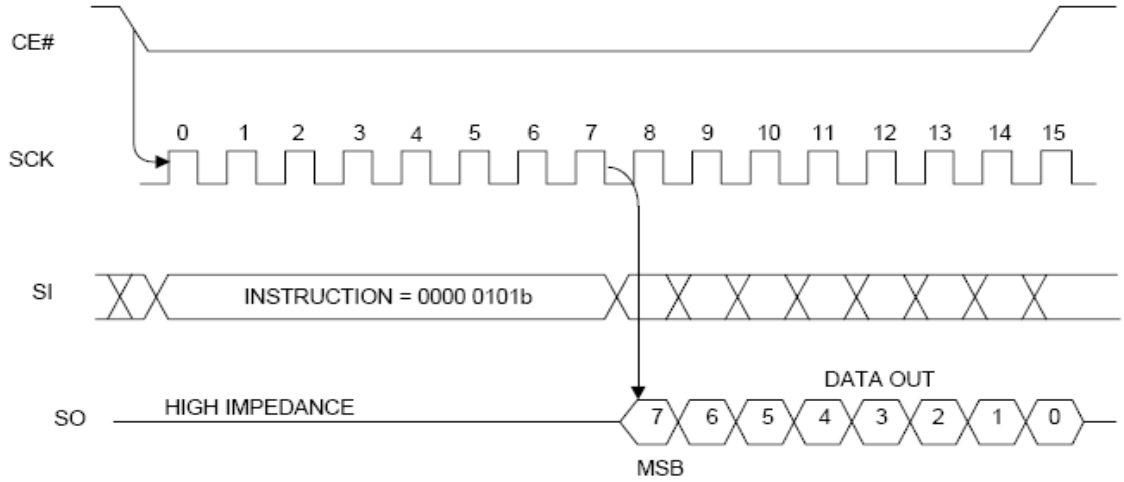


Figure 10. Read Status Register Sequence

WRSR (01h): WRITE STATUS REGISTER OPERATION

The Write Status Register (WRSR) instruction allows the Status Register to be written. A Write Enable instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving CE# low, sending the instruction code “01h”, and then writing the status register data into the non-volatile BP3, BP2, BP1, BP0, QE, and SRWD bits. The user can enable or disable the block protection and status register write protection features by writing “0”s or “1”s.

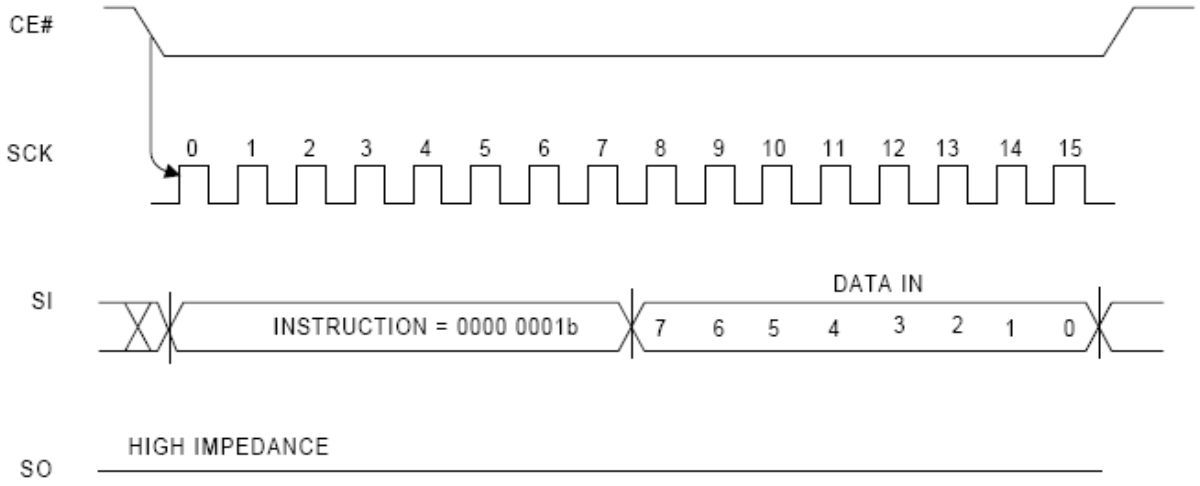


Figure 11. Write Status Register Sequence

READ (03h): READ DATA OPERATION

The READ instruction code is transmitted via the SI line, followed by three address bytes (A23 - A0) of the first memory location to be read. A total of 24 address bits are shifted in, but only A_{MS} (most significant address) - A0 are decoded. The remaining bits (A23 – A_{MS}) are ignored. The first byte addressed can be at any memory location. Upon completion, any data on the SI pin will be ignored. Refer to Table 9 for the related Address Key.

The first byte data (D7 - D0) addressed is then shifted out on the SO line, MSB first. A single byte of data, or up to the whole memory array, can be read out in one READ instruction. The address is automatically incremented after each byte of data is shifted out. The read operation can be terminated at any time by driving CE# high (VIH). When the highest address of the devices is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read in one continuous READ instruction.

If a Read Data instruction is issued while an Erase, Program, or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle.

The Read Data instruction allows clock rates from D.C. to a maximum of f_C (see AC Electrical Characteristics).

Address	IS25CQ032
A_N (A_{MS} – A_0)	A21 - A0
Don't Care Bits	A23 – A22

Table 9. Address Key

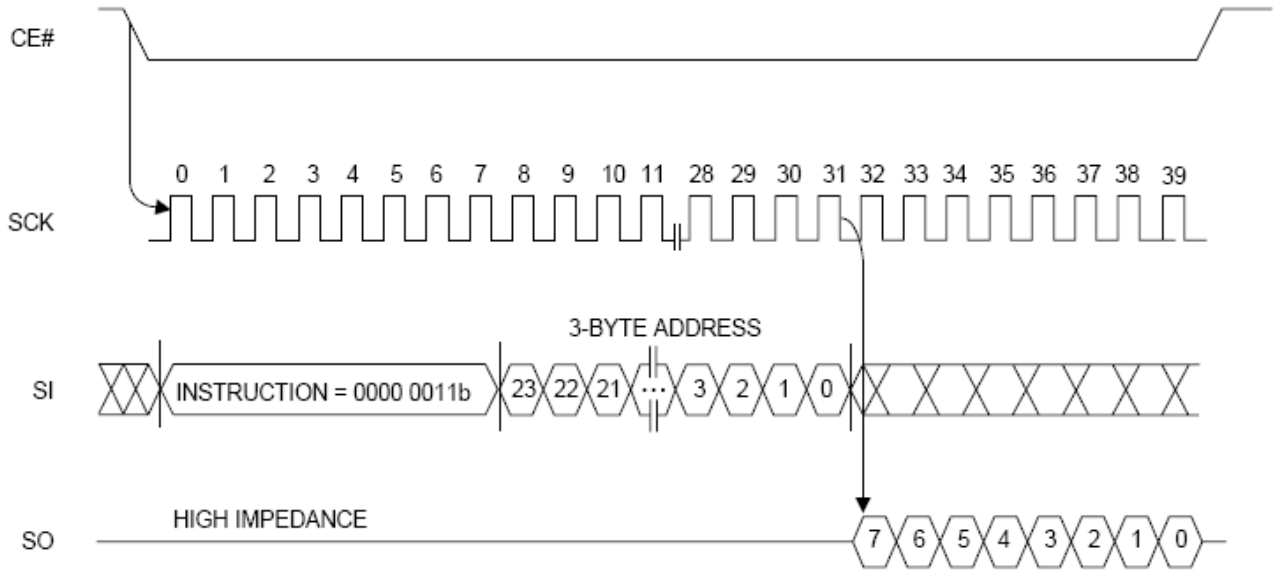


Figure 12. Read Data Sequence

FAST_READ (0Bh): FAST READ DATA OPERATION

The FAST_READ instruction code is followed by three address bytes (A23 - A0) and a dummy byte (8 clocks), transmitted via the SI line, with each bit latched-in during the rising edge of SCK. The dummy byte allows the devices internal circuits additional time for setting up the initial address. During the dummy cycle the data value on the SI pin is a “don’t care”.

The FAST_READ instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of f_{CT} (see AC Electrical Characteristics).

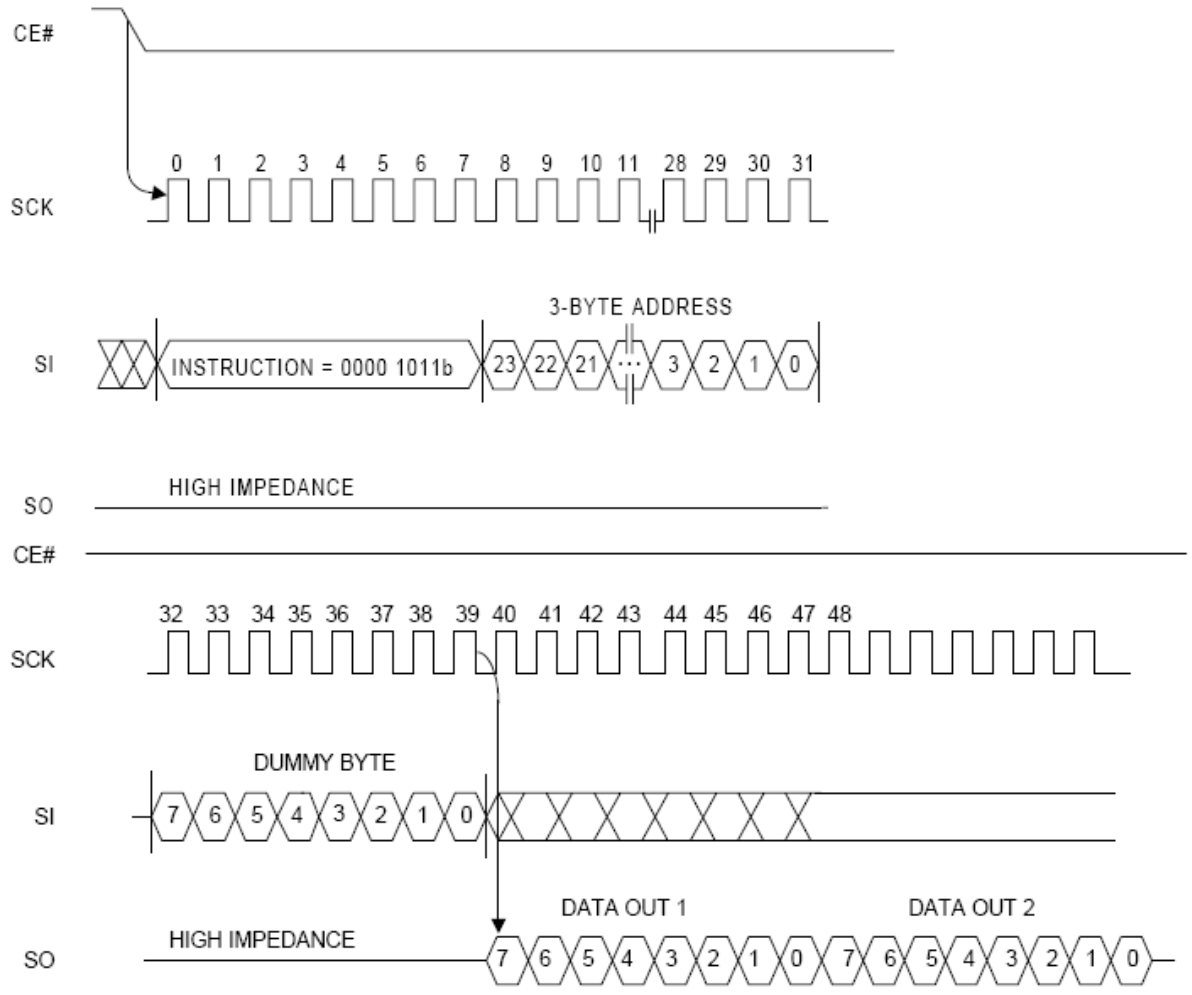


Figure 13. Fast Read Data Sequence

FRDO (3Bh): FAST READ DUAL OUTPUT OPERATION

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast_Read (0Bh) instruction except that data is output on two pins. This allows data to be transferred from the device at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code. Similar to the Fast_Read instruction, FRDO instruction can operate at the highest possible frequency of f_{CT} (see AC Electrical Characteristics).

This is accomplished by adding 1 dummy byte after the 24-bit address as. The dummy cycle allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy byte is "don't care".

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDO instruction. FRDO instruction is terminated by driving CE# high (VIH). If a FRDO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle

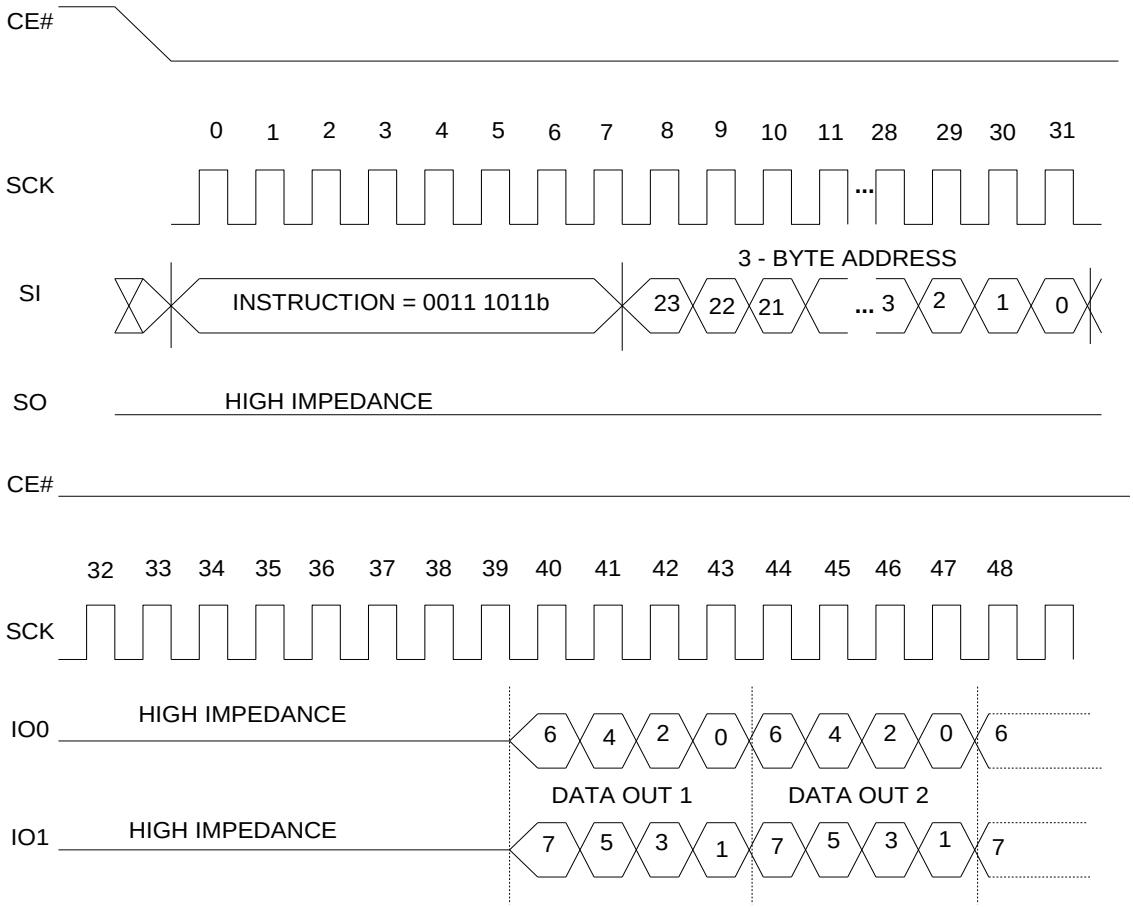


Figure 14. Fast Read Dual-Output Sequence

FRDIO (BBh): FAST READ DUAL I/O OPERATION

The FRDIO instruction is similar to the FRDO instruction, but allows the address bits to be input two bits at a time. This may allow for code to be executed directly from the SPI in some applications (XIP).

The FRDIO instruction code is followed by three address bytes (A23 – A0) and a mode byte, transmitted via the IO0 and IO1 lines, with each pair of bits latched-in during the rising edge of SCK. The address MSB is input on IO1, the next bit on IO0, and continues to shift in alternating on the two pins. The mode byte contains the value Ax, where x is a "don't care" value.

The first data byte addressed is shifted out on the IO1 and IO0 lines, with each pair of bits shifted out at a maximum frequency f_{CT}, during the falling edge of SCK. The MSB is output on IO1, while simultaneously the next bit is output on IO0.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDIO instruction. FRDIO instruction is terminated by driving CE# high (V_{IH}).

The device remains in this mode until it receives a Mode Reset (FFh) command. In subsequent FRDIO execution, the command code is not input, saving timing cycles. If a FRDIO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle

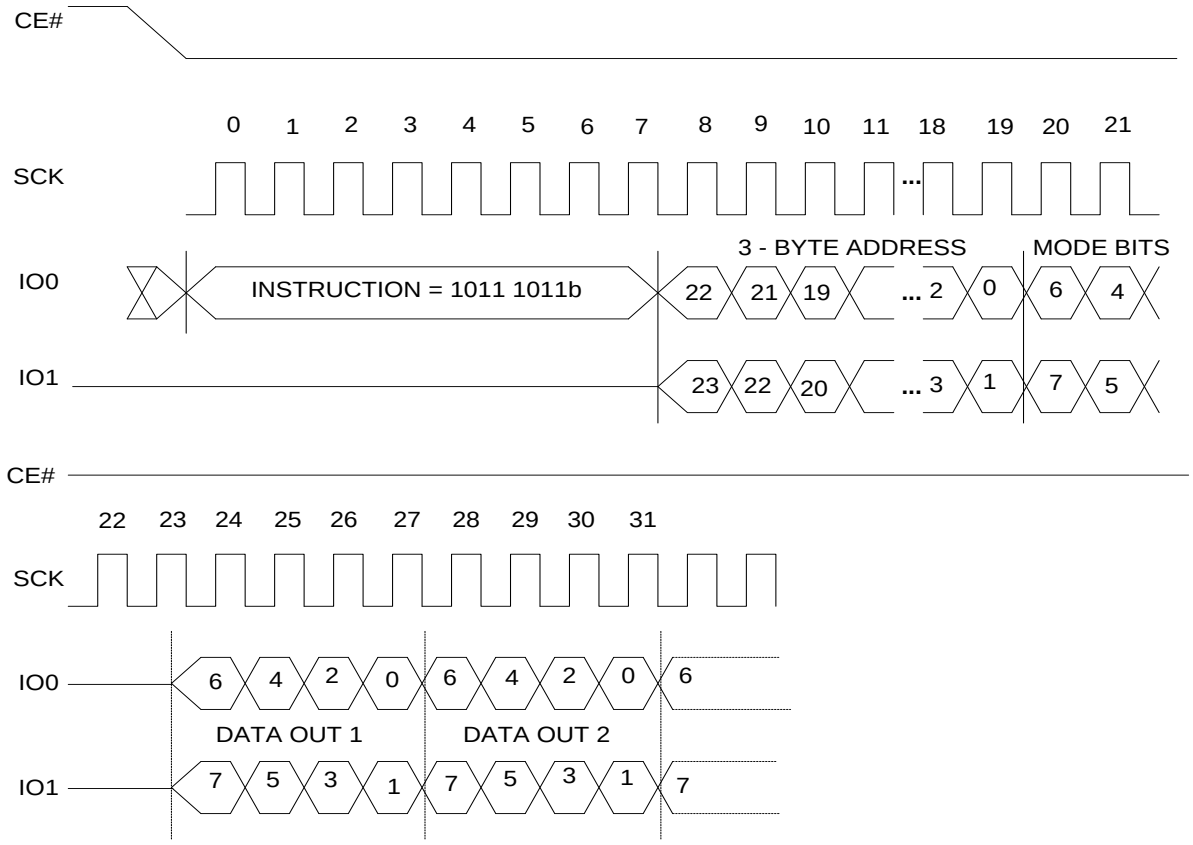


Figure 15. Fast Read Dual I/O Sequence (with command decode cycles)

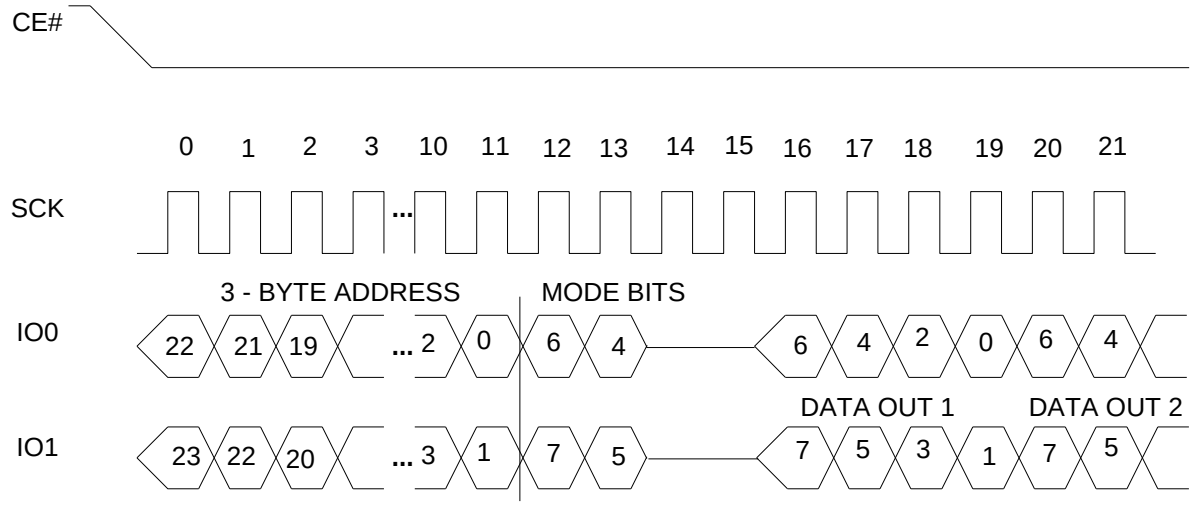


Figure 16. Fast Read Dual I/O Sequence (without command decode cycles)

FRQO (6Bh): FAST READ QUAD OUTPUT OPERATION

The FRQO instruction code is followed by three address bytes (A23 – A0) and a dummy byte (8 clocks), transmitted via the SI line, with each bit latched-in during the rising edge of SCK. The first data byte addressed is shifted out on the IO3, IO2, IO1 and IO0 lines, with each group of four bits shifted out at a maximum frequency f_{CT}, during the falling edge of SCK. The first bit (MSB) is output on IO3, while simultaneously the second bit is output on IO2, and the third bit is output on IO1, etc.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRQO instruction. FRQO instruction is terminated by driving CE# high (VIH). If a FRQO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle.

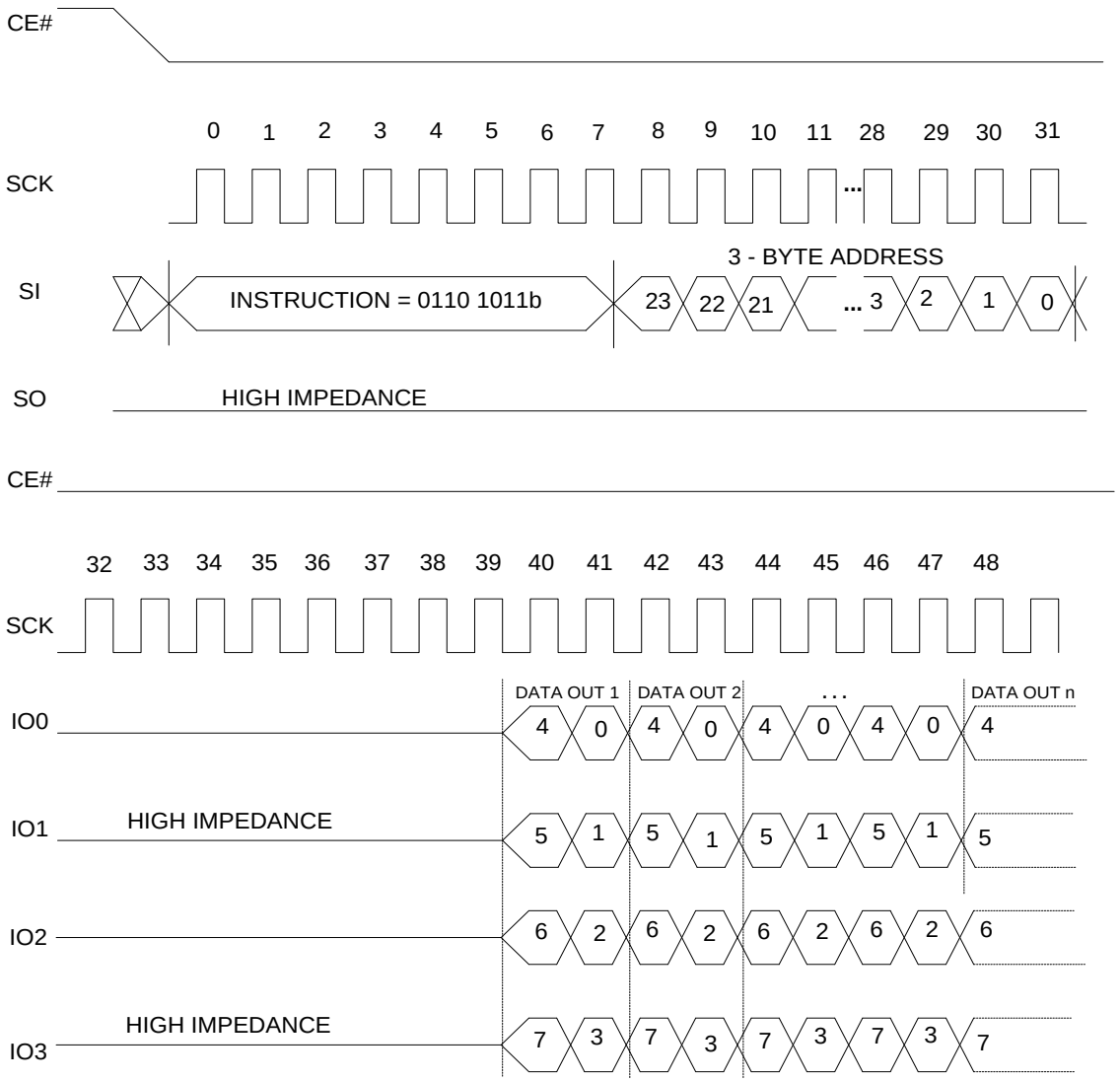


Figure 17. Fast Read Quad-Output Sequence

FRQIO (EBh): FAST READ QUAD I/O OPERATION

The FRQIO instruction is similar to the FRQO instruction, but allows the address bits to be input four bits at a time. This may allow for code to be executed directly from the device in some applications (XIP).

The FRQIO instruction code is followed by three address bytes (A23 – A0) and a mode byte, transmitted via the IO0, IO1, IO2, and IO3 lines, with each group of four bits simultaneously latched-in during the rising edge of SCK. The mode byte contains the value Ax, where x is a "don't care" value. After four dummy clocks, the first data byte addressed is shifted out. Each group of four bits are shifted out at a maximum frequency f_{CT} during the falling edge of SCK. Figure 18 illustrates the timing sequence.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRQIO instruction. FRQIO instruction is terminated by driving CE# high.

The device expects the next operation to be another FRQIO and will remain in this mode until it receives a Mode Reset (FFh) command. In subsequent FRDIO execution, the command code does not need to be entered thus reducing the overhead for fast data readout. See Figure 19.

If a FRQIO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle.

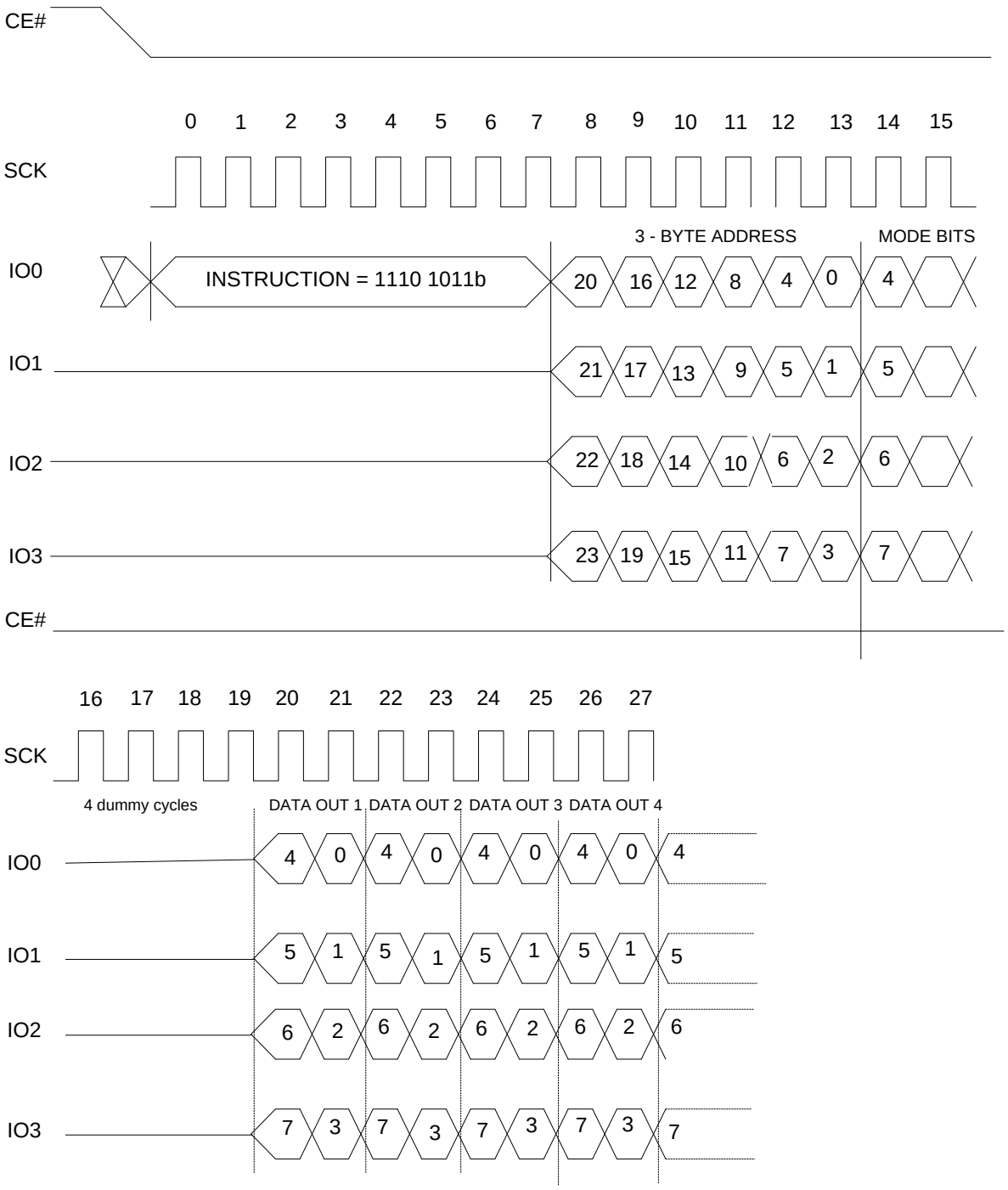


Figure 18. Fast Read Quad I/O Sequence (with command decode cycles)

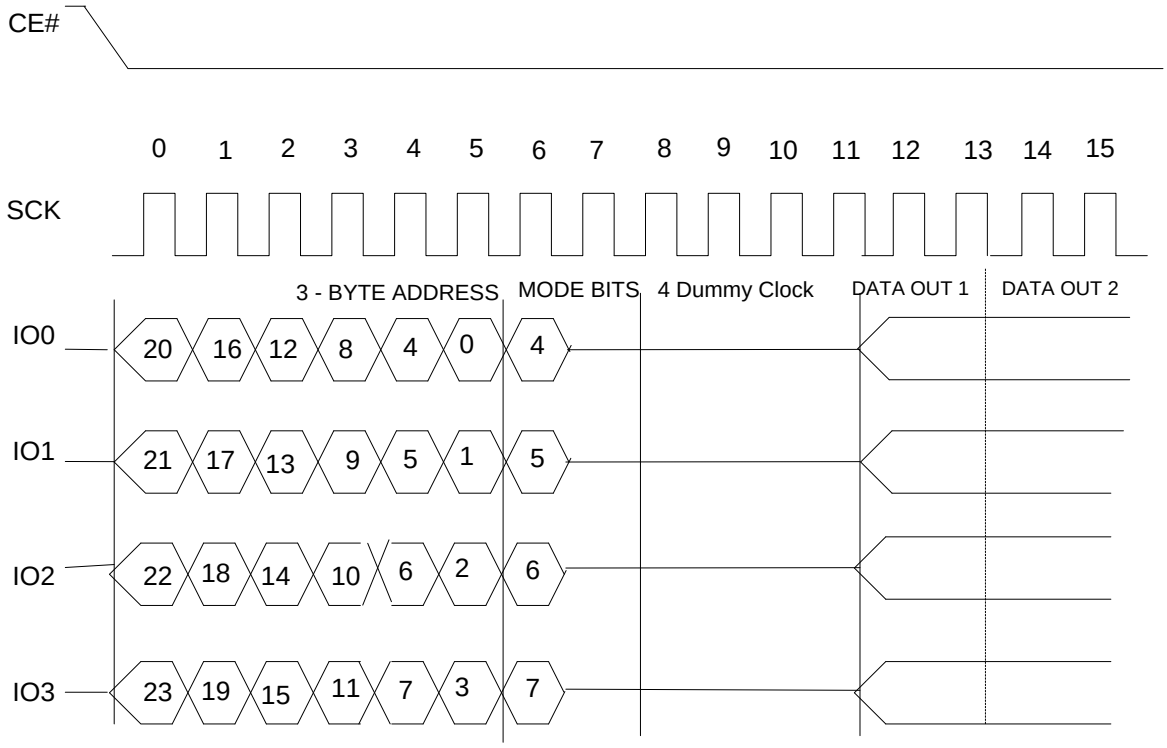


Figure 19. Fast Read Quad I/O Sequence (without command decode cycles)

MR (FFh): MODE RESET OPERATION

The Mode Reset command is used to conclude subsequent FRDIO and FRQIO operations. It resets the Mode bits to a value that is not Ax. It should only be executed after an FRDIO or FRQIO operation and is recommended as the first command after a system reset.

Figure 20 illustrates the difference in timing sequence for a Mode Reset issued after the FRDIO or FRQIO operation.

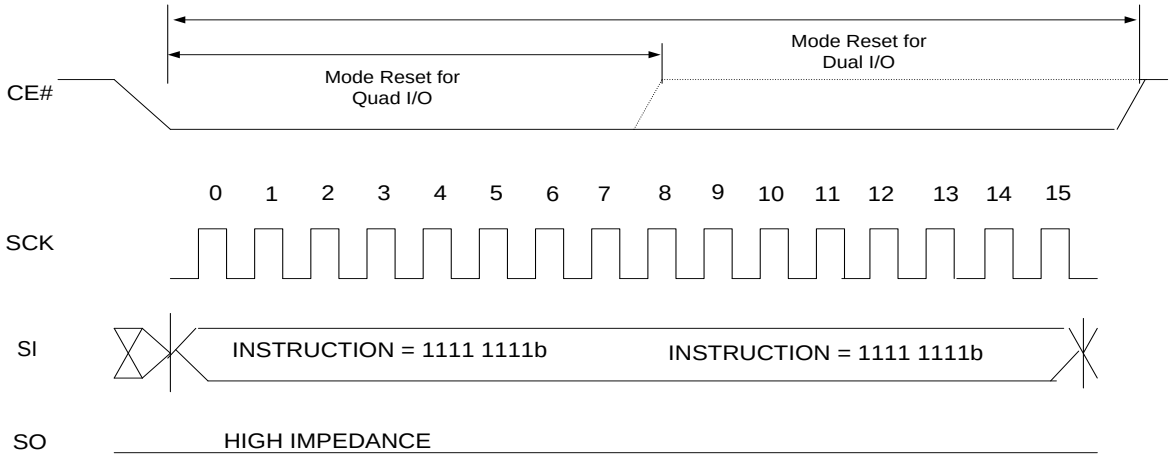


Figure 20. Mode Reset Command

PAGE_PROG (02h): PAGE PROGRAM OPERATION

The Page Program (PAGE_PROG) instruction allows from 1 to 256 bytes of data to be programmed into the device with a single operation. Memory areas protected by the Block Protection bits (BP3, BP2, BP1, and BP0) cannot be programmed. A PAGE_PROG instruction which attempts to program into a page that

is write-protected will be ignored. The Write Enable Latch (WEL) bit must be set to 1 before the execution of a PAGE_PROG instruction.

Once the device is selected (CE# = low) the PAGE_PROG instruction code, three address bytes, and program data (1 to 256 bytes) are input via the SI line. Program operation will start immediately after CE# is pulled high.

If more than 256 bytes of data are sent to a page, the address counter rolls over within the same page, and any previously latched in data is overwritten.

The Page Program operation does not need to start at any specific address and can be used to partially write a page. If the end of the page is reached, the address will wrap around to the beginning of the page and any previous data will be overwritten.

During a program operation, all instructions will be ignored except the RDSR instruction. The progress or completion of the program operation can be determined by reading the WIP bit of the Status Register via a RDSR instruction. If the WIP bit is "1", the program operation is still in progress. If WIP bit is "0", the program operation has completed.

Note: A program operation can alter "1"s into "0"s, but an erase operation is required to change "0"s back to "1"s. A byte cannot be reprogrammed without first erasing the whole sector or block.

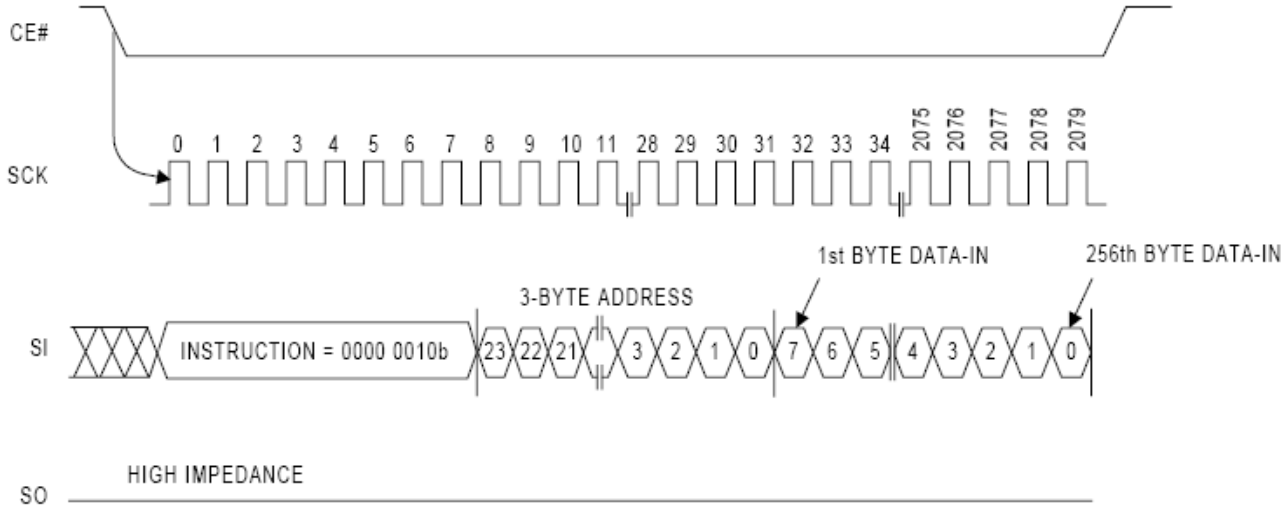


Figure 21. Page Program Sequence

Quad Page Program (32h): Quad Input Page Program Operation

The Quad Page Program instruction allows from 1 to 256 bytes of data to be programmed into the device with a single operation. Memory areas protected by the Block Protection bits (BP3, BP2, BP1, and BP0) cannot be programmed. A Quad Page Program instruction which attempts to program into a page that is write-protected will be ignored. Before the execution of the Quad Page Program instruction, the QE bit in the status register must be set to "1", and the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction.
.

Once the device is selected (CE# = low) the Quad Page Program instruction code, three address bytes, and program data (1 to 256 bytes) via the four pins (IO0, IO1, IO2 and IO3). Program operation will start immediately after CE# is pulled high.

If more than 256 bytes of data are sent to a page, the address counter rolls over within the same page, and any previously latched in data is overwritten.

The Quad Page Program operation does not need to start at any specific address and can be used to partially write a page. If the end of the page is reached, the address will wrap around to the beginning of the page and any previous data will be overwritten.

During a program operation, all instructions will be ignored except the RDSR instruction. The progress or completion of the program operation can be determined by reading the WIP bit of the Status Register via a RDSR instruction. If the WIP bit is “1”, the program operation is still in progress. If the WIP bit is “0”, the program operation has completed.

Note: A program operation can alter “1”s into “0”s, but an erase operation is required to change “0”s back to “1”s. A byte cannot be reprogrammed without first erasing the whole sector or block.

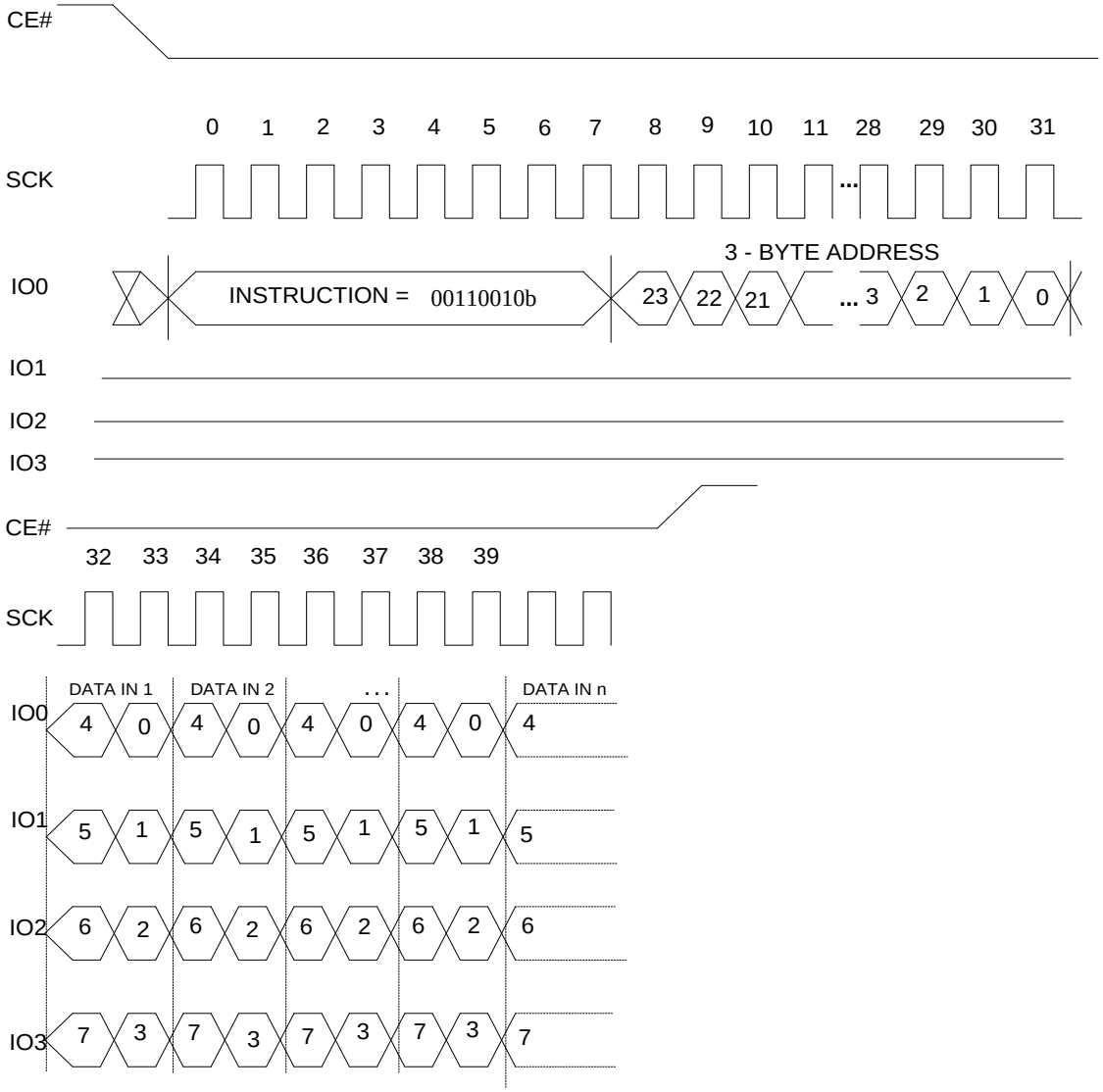


Figure 22. Quad Page Program Sequence

ERASE OPERATION

The memory array is organized into uniform 4 Kbyte sectors or 64 Kbyte uniform blocks (a block consists of sixteen adjacent sectors).

Before a byte can be reprogrammed, the sector or block that contains the byte must be erased (erasing sets bits to "1"). In order to erase the devices, there are three erase instructions available: Sector Erase (SECTOR_ER), Block Erase (BLOCK_ER) and Chip Erase (CHIP_ER). A sector erase operation allows any individual sector to be erased without affecting the data in other sectors. A block erase operation erases any individual block. A chip erase operation erases the whole memory array of a device. A sector erase, block erase, or chip erase operation can be executed prior to any programming operation.

During an erase operation all instruction will be ignored except the Read Status Register (RDSR) instruction. The progress or completion of the erase operation can be determined by reading the WIP bit in the Status Register using a RDSR instruction. If the WIP bit is "1", the erase operation is still in progress. If the WIP bit is "0", the erase operation has been completed.

SECTOR_ER (D7h/20h):

SECTOR ERASE OPERATION
The SECTOR_ER instruction supports dual instructions of D7h or 20h and erases a 4 Kbyte sector. Before the execution of a SECTOR_ER instruction the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL bit is reset automatically after the completion of an erase operation.

The SECTOR_ER instruction is entered after CE# is pulled low to select the device and stays low during the entire instruction sequence. The SECTOR_ER instruction code and three address bytes are input via SI. Erase operation will start immediately after CE# is pulled high. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 23 for Sector Erase Sequence.

BLOCK_ER (D8h):

BLOCK ERASE OPERATION
The Block Erase (BLOCK_ER) instruction erases a 64 Kbyte block. Before the execution of a BLOCK_ER instruction the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL is reset automatically after the completion of a block erase operation.

A BLOCK_ER instruction is entered after CE# is pulled low to select the device and stays low during the entire instruction sequence. The BLOCK_ER instruction code and three address bytes are input via SI. Erase operation will start immediately after CE# is pulled high. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 24 for Block Erase Sequence.

CHIP_ER COMMAND (C7h/60h):

CHIP ERASE OPERATION
The CHIP_ER instruction supports dual instructions of C7h or 60h. Before the execution of CHIP_ER instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL is reset automatically after completion of a chip erase operation.

The CHIP_ER instruction is entered after CE# is pulled low to select the device and stays low during the entire instruction sequence. The CHIP_ER instruction code is input via SI. Erase operation will start immediately after CE# is pulled high. The internal control logic

automatically handles the erase voltage and timing.
Refer to Figure 25 for Chip Erase Sequence.

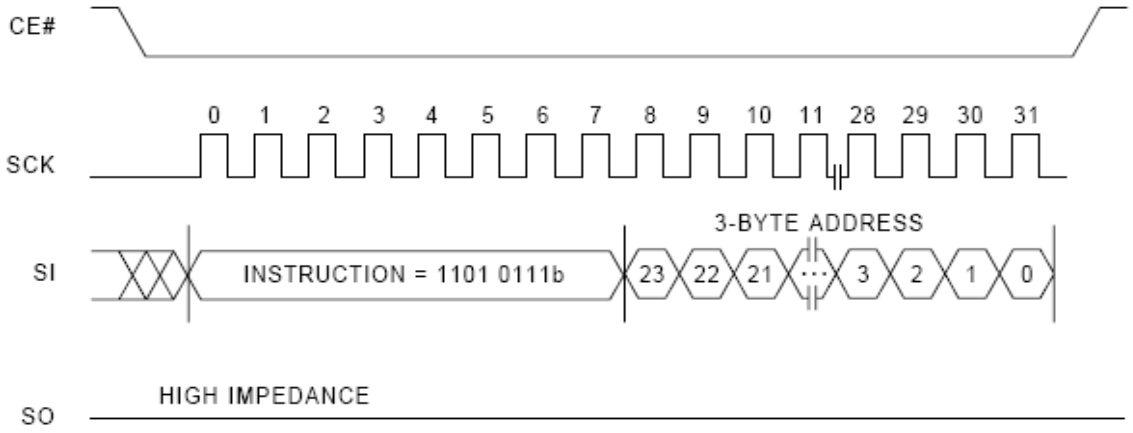


Figure 23. Sector Erase Sequence

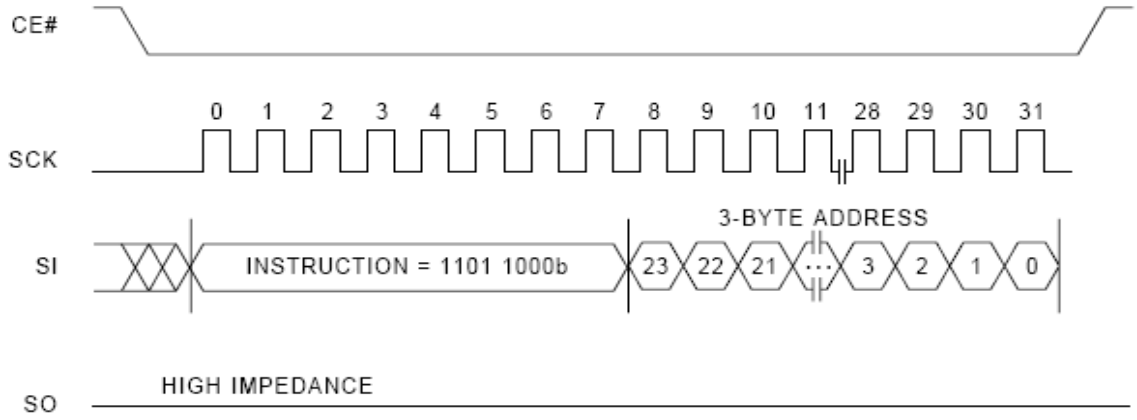


Figure 24. Block Erase Sequence

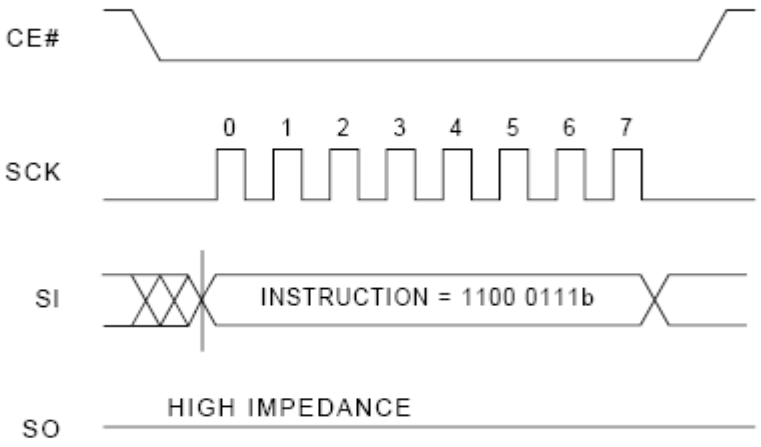


Figure 25. Chip Erase Sequence

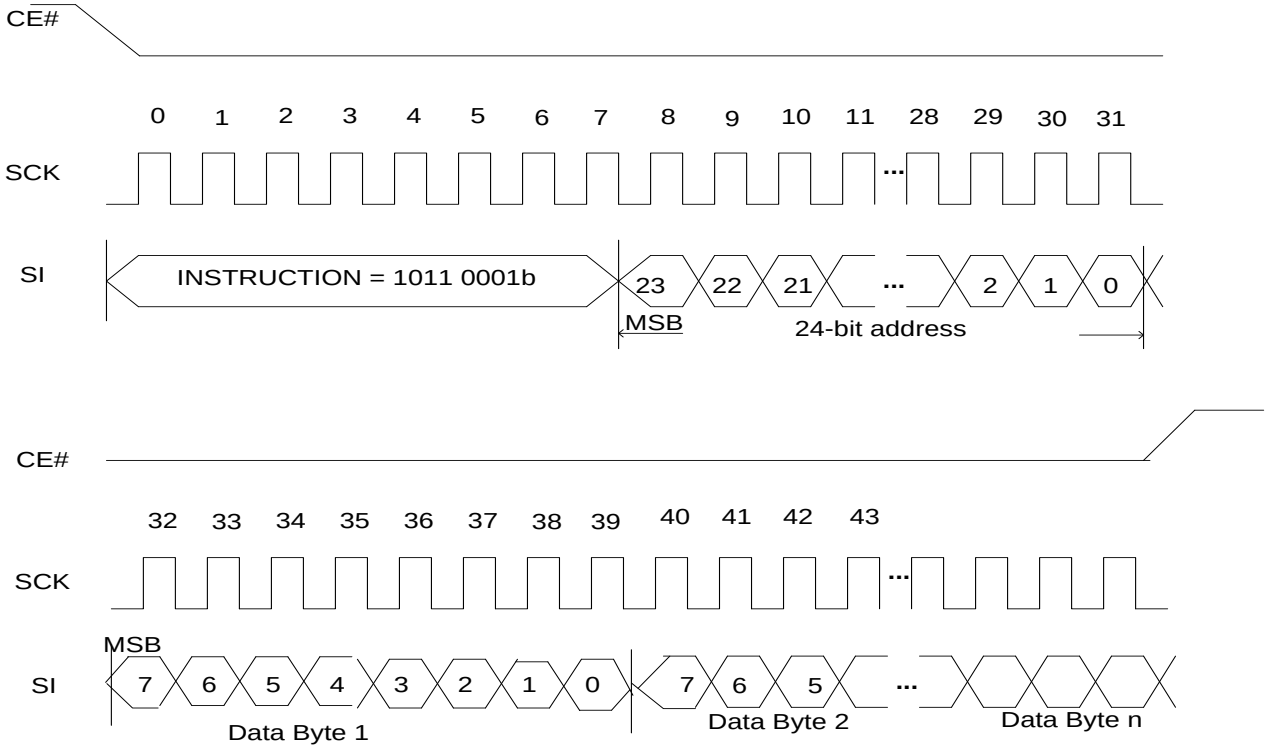
One Time Programmable Secure Area (OTP) : 64 Bytes of OTP + 1 Control Byte

PSIR (B1h): Program Security Information instruction

The PSIR command is used to program the 64 Bytes (plus one additional control Byte) of secured memory area set aside for one time programmable security area. Information can be stored in the array but not altered. Passcodes, Unique IDs, Identifiers, etc. can be stored in this area to prevent counterfeiting or even unwanted access. Before instructions can be accepted a write enable (WREN) instruction must have been previously executed to set the write enable latch (WEL) bit. Once the device has been selected via the CE# pin, the instruction code is followed by three address bytes to program the secured area and up to 64 bytes of data (plus 1 control Byte) to the SI line. CE# pin must be pulled high after the eighth bits of the last data byte has been latched in, otherwise the instruction is not executed. If more than 64 bytes of data + 1 Control Byte is sent to the secured area the address counter may roll over and re-write the secured information.

Warning: Do not attempt to write more than the 64 Bytes of OTP + 1 Control Byte

After CE# pin is driven high, the self-timed page program cycle (whose duration is t_{potp}) is initiated. While the program PSIR cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed program cycle, and it is 0 when it is completed. At some unspecified time before the cycle is complete, the write enable latch (WEL) bit is reset.



Note: 1. $1 \leq n \leq 65$
2. The security area is from 080000h to 08003Fh.
3. The protection lock bit is in the address 080040h.

Figure 26. Program Security Information Row Sequence

Locking the Secure (OTP) Memory

Bit 0 of byte 65 is used to permanently lock the OTP memory array.

1. When bit 0 of byte 65 = ’1’, the 64 bytes of the OTP memory array can be programmed.
2. When bit 0 of byte 65 = ‘0’, the 64 bytes of the OTP memory array is read-only and cannot be programmed anymore.

Once bit 0 of the control byte has been programmed to ‘0’, it can no longer be set to ‘1’. Therefore, as soon as bit 0 of byte 65 (control byte) is set to ‘0’, the 64 bytes of the OTP memory array permanently become read-only.

Any program instruction issued while an erase, program, or write cycle is in progress is rejected without having any effect on the current instruction.

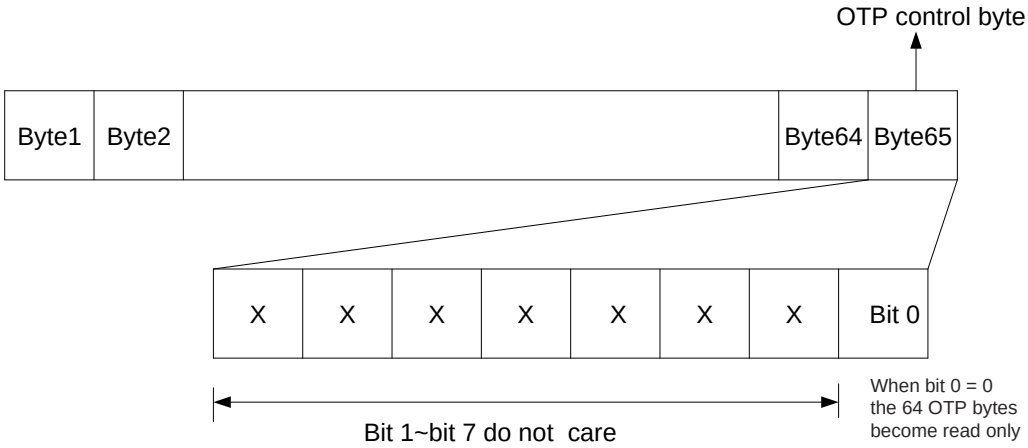
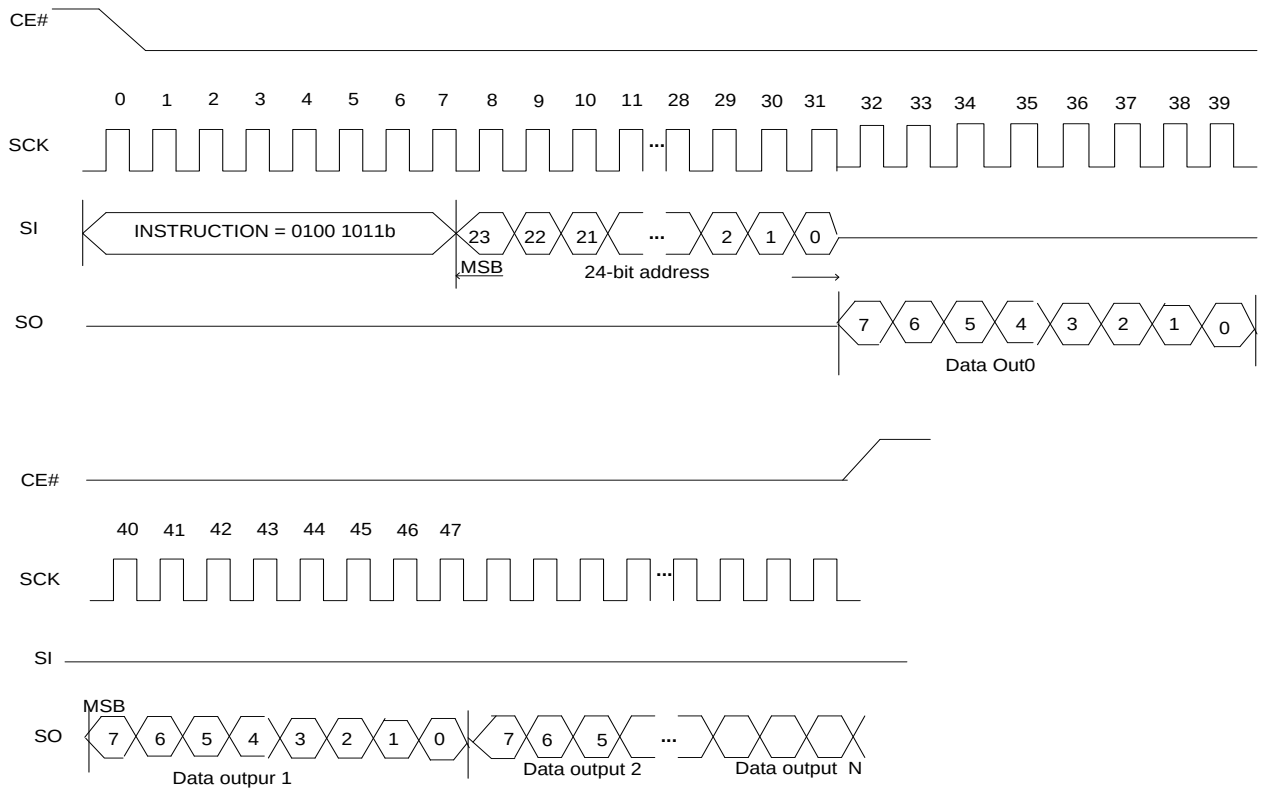


Figure 27. Control Byte to lock security memory

RSIR (4Bh): Read Security Information Area

The RSIR instruction reads the security memory. There is no rollover mechanism while reading the secured area. The read instruction must be sent with the maximum of 65 bytes to read, once the 65th byte has been read, the same (65th) byte continues being read on the SO pin revealing the locked or unlocked status of the Control Byte.



Note: 1. $1 \leq n \leq 65$
2. The security area is from 080000h to 08003Fh.
3. The protection lock bit is in the address 080040h.

Figure 28. Read Security information instruction

Erase Suspend (75h)

The Erase Suspend instruction (75h) allows the system to interrupt a Sector or Block Erase operation. Erase instructions (20h, D7h, D8h, C7h, 60h) are not allowed during the Erase Suspend instruction. Erase Suspend is valid only during the Sector or Block erase operation. If Erase Suspend is issued during a chip erase operation it will be ignored. A maximum time of Tws (See AC Characteristics) is required to elapse before any new read or program instructions are issued. The WEL bit in the Status Register will clear to 0 after an Erase Suspend instruction.

Unexpected power off during the Erase suspend state will reset the device and release the suspend state. The data within the page, sector, or block that was being suspended may become corrupted.

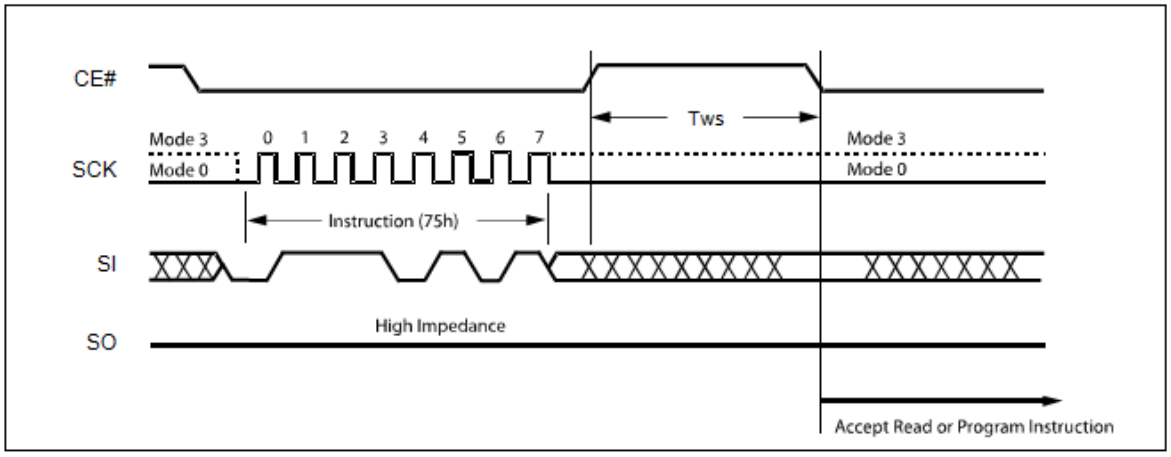


Figure 29. Erase Suspend Instruction

Erase Resume (7Ah)

The Erase Resume instruction must be written to resume the Sector or Block Erase operation after an Erase Suspend operation. Poll the WIP bit in the Status register or wait the specified time TSE and TBE. The total time before and after a suspend function will not exceed TSE or TBE when resuming a sector erase or block erase respectively. Resume instructions will be ignored if an Erase Suspend operation is still active.

Resume instruction is ignored if the previous Erase Suspend operation was interrupted by an unexpected power off.

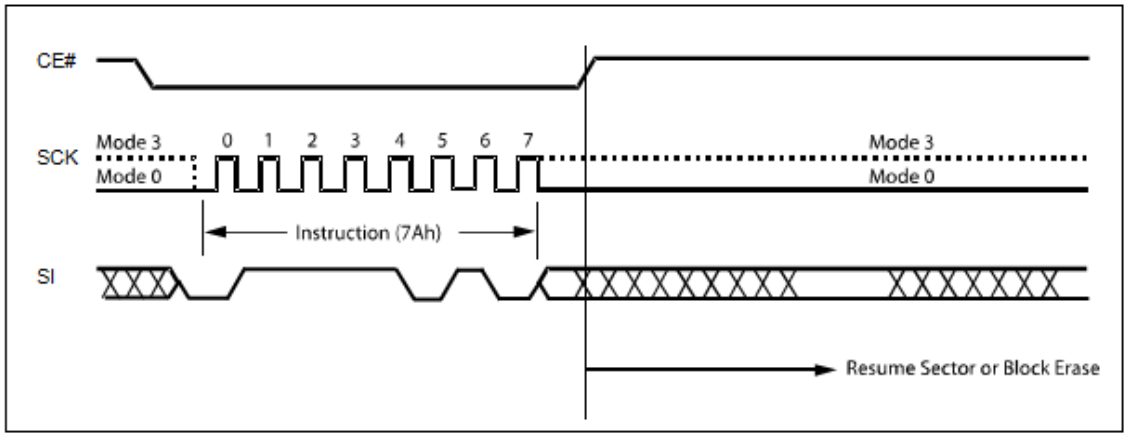


Figure 30. Erase Resume Instruction

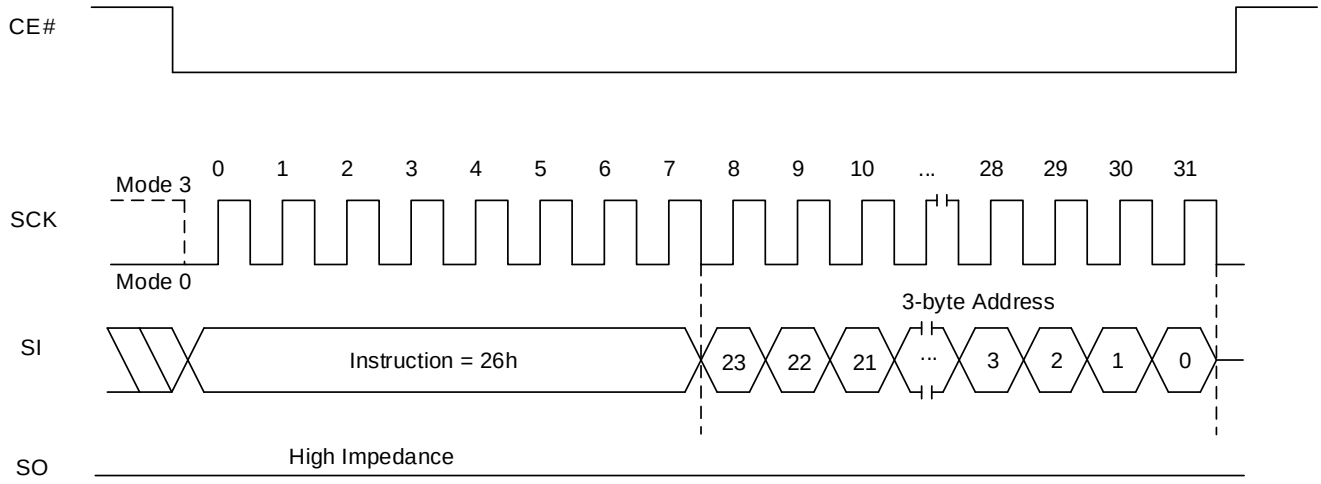
*Note:
1. 500ns delay needed from write command to suspend command
2. 1ms delay needed from Erase Resume to Erase Suspend

SECTOR LOCK/UNLOCK FUNCTIONS

SECTOR UNLOCK OPERATION (SECUNLOCK, 26h)

The Sector Unlock command allows the user to select a specific sector to allow program and erase operations. This instruction is effective when the blocks are designated as write-protected through the BP0, BP1, BP2, and BP3 bits in the Status Register. Only one sector can be enabled at any time. If many SECUNLOCK commands are input, only the last sector designated by the last SECUNLOCK command will be unlocked. The instruction code is followed by a 24-bit address specifying the target sector, but A0 through A11 are not decoded. The remaining sectors within the same block remain as read-only.

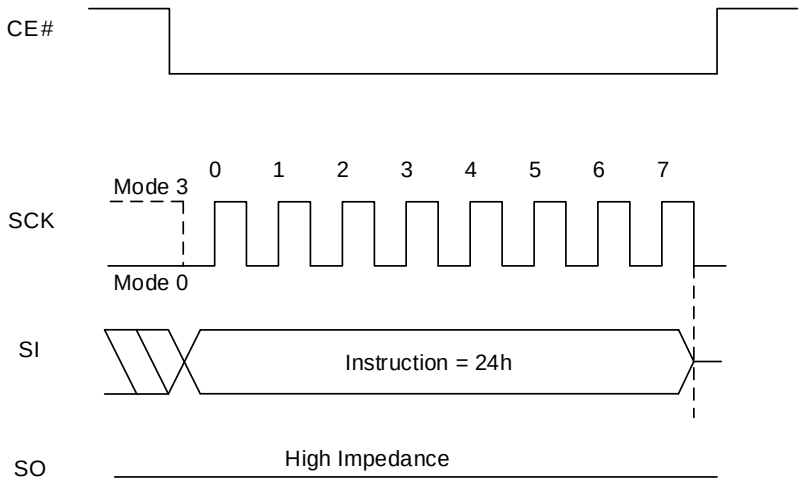
Figure 8.30 Sector Unlock Sequence



SECTOR LOCK OPERATION (SECLOCK, 24h)

The Sector Lock command relocks a sector that was previously unlocked by the Sector Unlock command. The instruction code does not require an address to be specified, as only one sector can be enabled at a time. The remaining sectors within the same block remain in read-only mode.

Figure 8.31 Sector Lock Sequence



ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature		-55°C to +125°C
Surface Mount Lead Soldering Temperature	Standard Package	240°C for 3 Seconds
	Lead-free Package	260°C for 3 Seconds
Input Voltage with Respect to Ground on All Pins (2)		-0.5 V to VCC + 0.5 V
All Output Voltage with Respect to Ground		-0.5 V to VCC + 0.5 V
VCC (2)		-0.5 V to +6.0 V

Table 10. Absolute Max Ratings

Notes:
1. Applied conditions greater than those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. The functional operation of the device conditions that exceed those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

2. Maximum DC voltage on input or I/O pins is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot V_{CC} by + 2.0 V for a period of time not to exceed 20 ns. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may undershoot GND by -2.0 V for a period of time not to exceed 20 ns.

DC AND AC OPERATING RANGE

Part Number		**IS25CQ032**
Operating Temperature	Extended Grade	-40°C to 105°C
Vcc Power Supply		2.70 V – 3.60 V

Table 11. Voltage and Temperature Ratings

DC CHARACTERISTICS

Applicable over recommended operating range from:
T_{AC} = -40°C to +105°C, V_{CC} = 2.70 V to 3.60 V (unless otherwise noted).

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{CC1}	Vcc Active Read Current	V_{CC} = 3.60V at 33 MHz, SO = Open			10	15	mA
I_{CC2}	Vcc Program/Erase Current	V_{CC} = 3.60V at 33 MHz, SO = Open			15	25	mA
I_{SB1}	Vcc Standby Current CMOS	V_{CC} = 3.60V, CE# = V_{CC}			5	50	µA
I_{SB2}	Vcc Standby Current TTL	V_{CC} = 3.60V, CE# = V_{IH} to V_{CC}				3	mA
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}				1	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}, T_{AC} = 0ºC to 130ºC				1	µA
V_{IL}	Input Low Voltage			-0.5		0.3Vcc	V
V_{IH}	Input High Voltage			0.7V_{CC}		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	2.70V < V_{CC} < 3.60V	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage		I_{OH} = -100 µA	V_{CC} – 0.2			V

Table 12. DC Characteristics Table

AC CHARACTERISTICS

Applicable over recommended operating range from T_A = -40°C to +105°C, V_{CC} = 2.70 V to 3.60 V
C_L = 1 TTL Gate and 30 pF (unless otherwise noted).

Symbol	Parameter		Min	Typ	Max	Units
f_{CT}	Clock Frequency for fast read mode	SPI	0		104	MHz
		Dual/Quad SPI	0		80	
f_C	Clock Frequency for read mode		0		33	MHz
t_{RI}	Input Rise Time				8	ns
t_{FI}	Input Fall Time				8	ns
t_{CKH}	SCK High Time		4			ns
t_{CKL}	SCK Low Time		4			ns
t_{CEH}	CE# High Time		25			ns
t_{CS}	CE# Setup Time		10			ns
t_{CH}	CE# Hold Time		5			ns
t_{DS}	Data In Setup Time		2			ns
t_{DH}	Data in Hold Time		2			ns
t_{HS}	Hold Setup Time		15			ns
t_{HD}	Hold Time		15			ns
t_V	Output Valid				8	ns
t_{OH}	Output Hold Time Normal Mode		0			ns
t_{LZ}	Hold to Output Low Z				200	ns
t_{HZ}	Hold to Output High Z				200	ns
t_{DIS}	Output Disable Time				100	ns
t_{SE}	Sector Erase Time			75	450	ms
t_{BE}	Block Erase Time			300	1500	ms
t_{CE}	Chip Erase Time (32Mb)			9	20	s
t_{PP}	Page Program Time			1	4	ms
t_{VCS}	V_{CC} Set-up Time		50			µs
t_{res}	Time required after release from Power Down				3	µs
t_w	Write Status Register time			5	50	ms
T_{WS}	CE# High to next Instruction after Suspend				20	µs

Table 13. AC Characteristics Table

AC CHARACTERISTICS (CONTINUED)

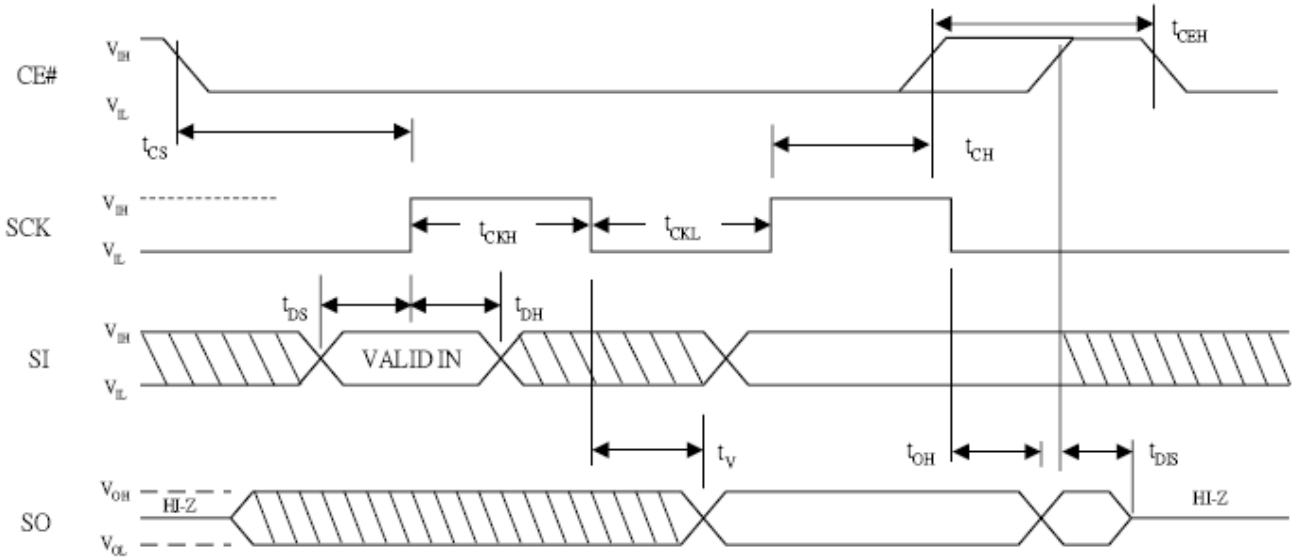


Figure 31. SERIAL INPUT/OUTPUT TIMING (1)

Note: 1. For SPI Mode 0 (0,0)

AC CHARACTERISTICS (CONTINUED)

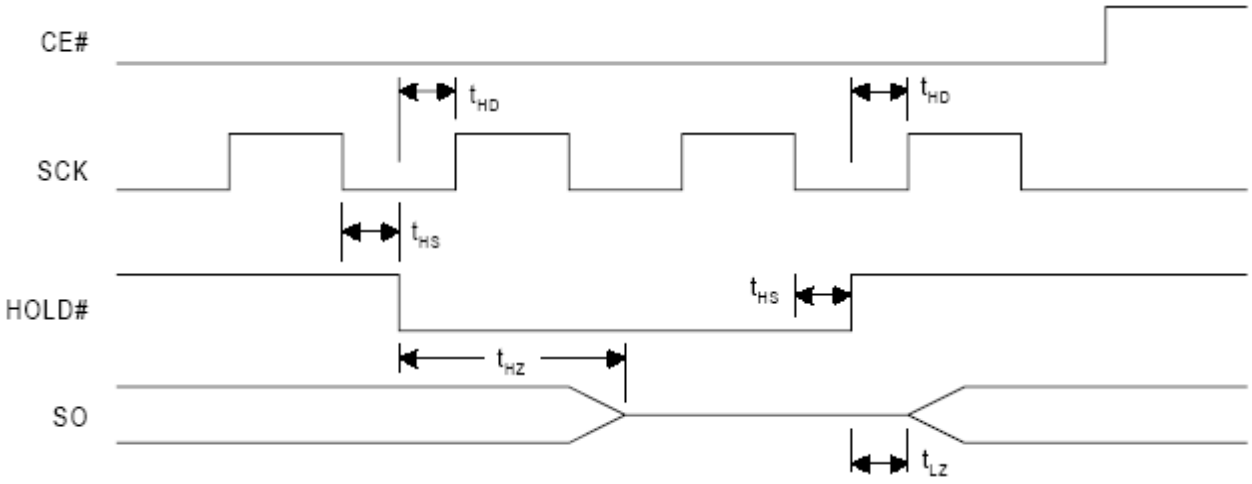


Figure 32. HOLD TIMING

PIN CAPACITANCE (f = 1 MHz, T = 25°C)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: These parameters are characterized but not 100% tested.
Table. 14 Pin Capacitance

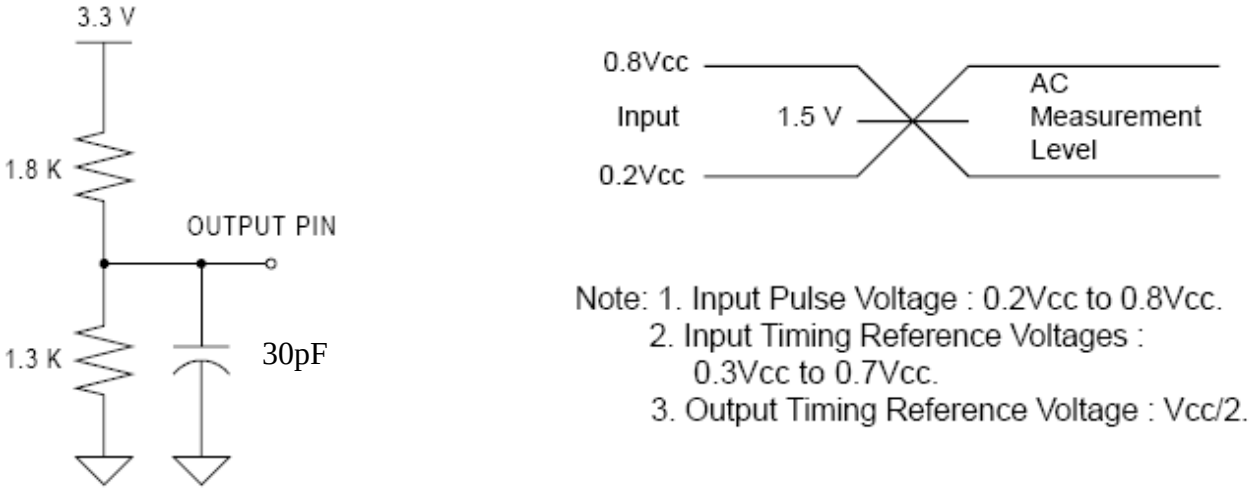


Figure 33. Output load test and input test waveform and measurement levels

POWER-UP AND POWER-DOWN

At Power-up and Power-down, the device must not be selected until Vcc reaches Vcc(min) during power-up and tVCE has elapsed or Vcc has reached Vss at Power-down.

For most applications it is recommended that a simple pull-up resistor on CE# can be used to insure safe and proper Power-up and Power-down sequences.

To avoid data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is incorporated. The logic inside the device holds reset while Vcc is less than the POR threshold value (Vwi) during power up, the device does not respond to
any instruction until a time delay of tPUW has elapsed after the moment that Vcc rises above the VWI threshold. However, the correct operation of the device is not guaranteed if, by this time, Vcc is still below Vcc(min). No instructions should be sent until:
- Vcc passes the VWI threshold and tPUW delay has elapsed
- Vcc passed the Vcc(min) level and tVCE delay has elapsed

At Power-up, the device is in the following state:
- The device is in the Standby mode
- The Write Enable Latch (WEL) bit is reset

At Power-down, when Vcc drops from the operating voltage to below the Vwi, all write operations are disabled and the device does not respond to any instructions.

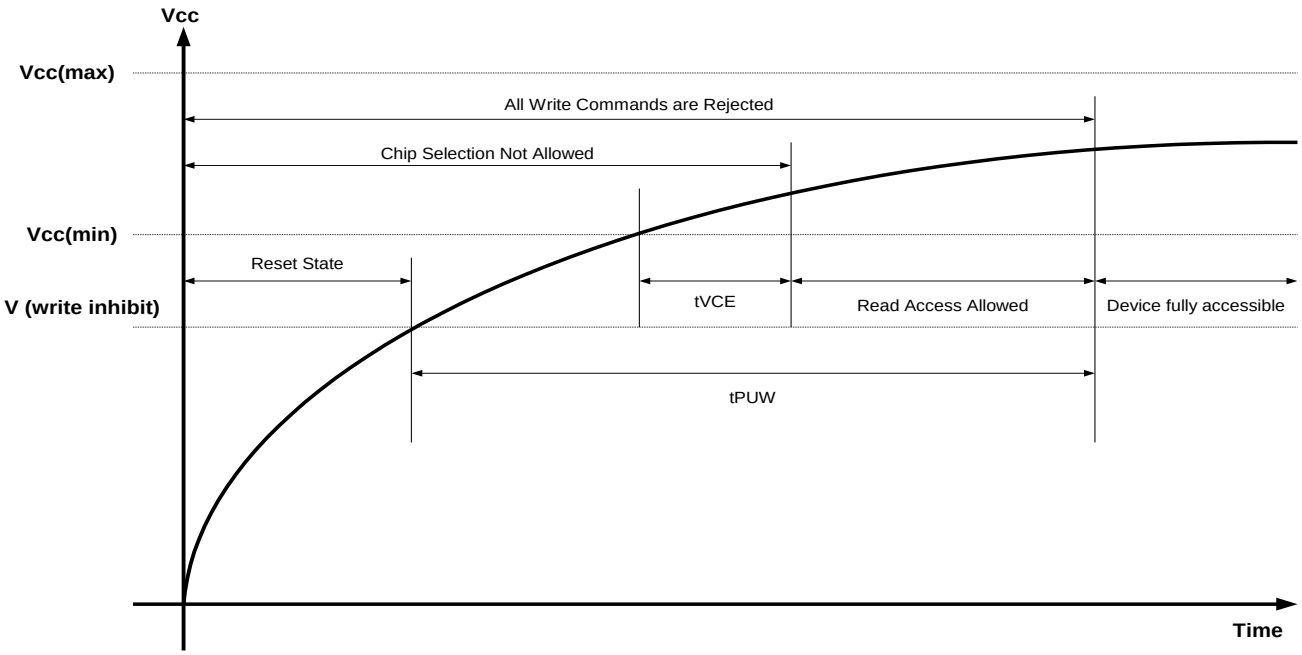


Figure 34. Power up Sequence

PROGRAM/ERASE PERFORMANCE

Parameter	Typ	Max	Unit	Remarks
Sector Erase Time	75	450	ms	From writing erase command to erase completion
Block Erase Time	300	1500	ms	From writing erase command to erase completion
Chip Erase Time	9	20	s	From writing erase command to erase completion
Page Programming Time	1	4	ms	From writing program command to program completion
Byte Program	8	25	us	

Note: These parameters are characterized and are not 100% tested.

RELIABILITY CHARACTERISTICS(1)

Endurance(2)	100,000 Cycles	JEDEC Standard A117
Data Retention	20 Years	JEDEC Standard A103
ESD – Human Body Model	2,000 Volts	JEDEC Standard A114
ESD – Machine Model	200 Volts	JEDEC Standard A115
Latch-Up	100 + I_{CC1} mA	JEDEC Standard 78

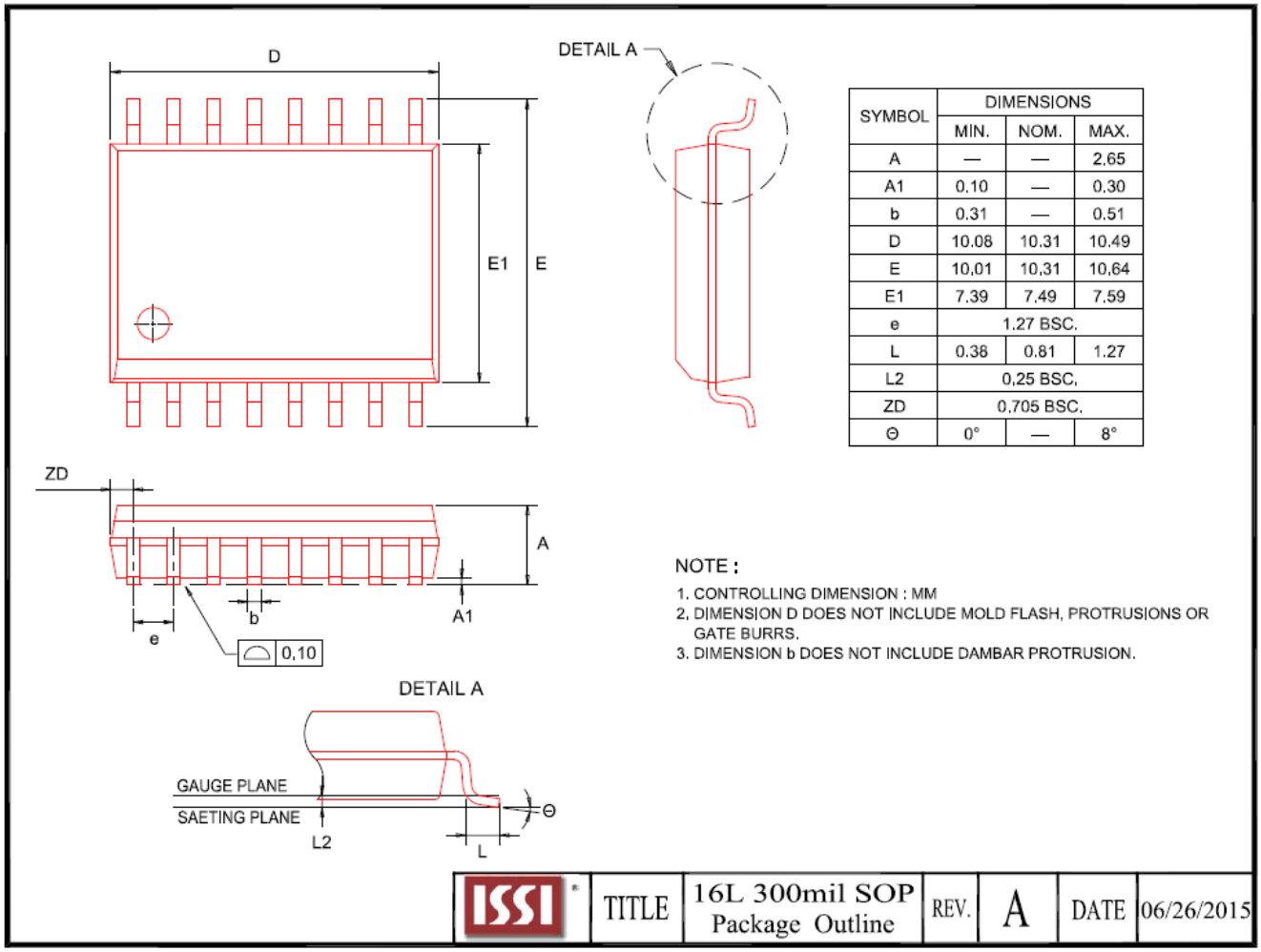
Note: These parameters are characterized and are not 100% tested

(2) 100,000 Continuous Chip and Block cycling, 100,000 Continuous Sector cycling

Table 14. Program/Erase and Reliability data

PACKAGE TYPE INFORMATION

16-Pin JEDEC 300mil Small Outline Integrated Circuit (SOIC) Package (JM)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	2.65
A1	0.10	—	0.30
b	0.31	—	0.51
D	10.08	10.31	10.49
E	10.01	10.31	10.64
E1	7.39	7.49	7.59
e	1.27 BSC.		
L	0.38	0.81	1.27
L2	0.25 BSC.		
ZD	0.705 BSC.		
Θ	0°	—	8°

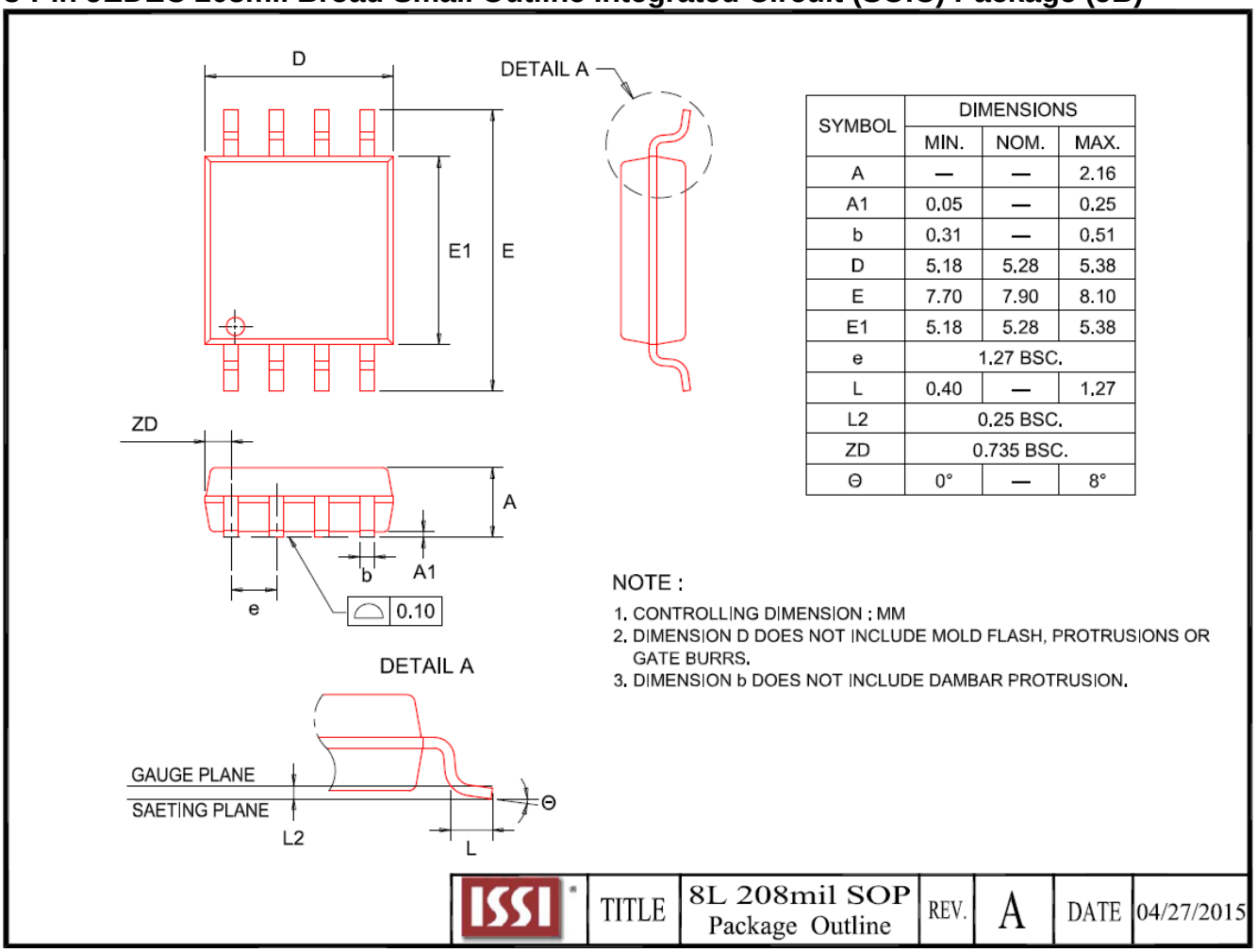
NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

ISSI	TITLE	16L 300mil SOP Package Outline	REV.	A	DATE	06/26/2015

Note: Lead co-planarity is 0.08mm.

8-Pin JEDEC 208mil Broad Small Outline Integrated Circuit (SOIC) Package (JB)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	2.16
A1	0.05	—	0.25
b	0.31	—	0.51
D	5.18	5.28	5.38
E	7.70	7.90	8.10
E1	5.18	5.28	5.38
e	1.27 BSC.		
L	0.40	—	1.27
L2	0.25 BSC.		
ZD	0.735 BSC.		
Θ	0°	—	8°

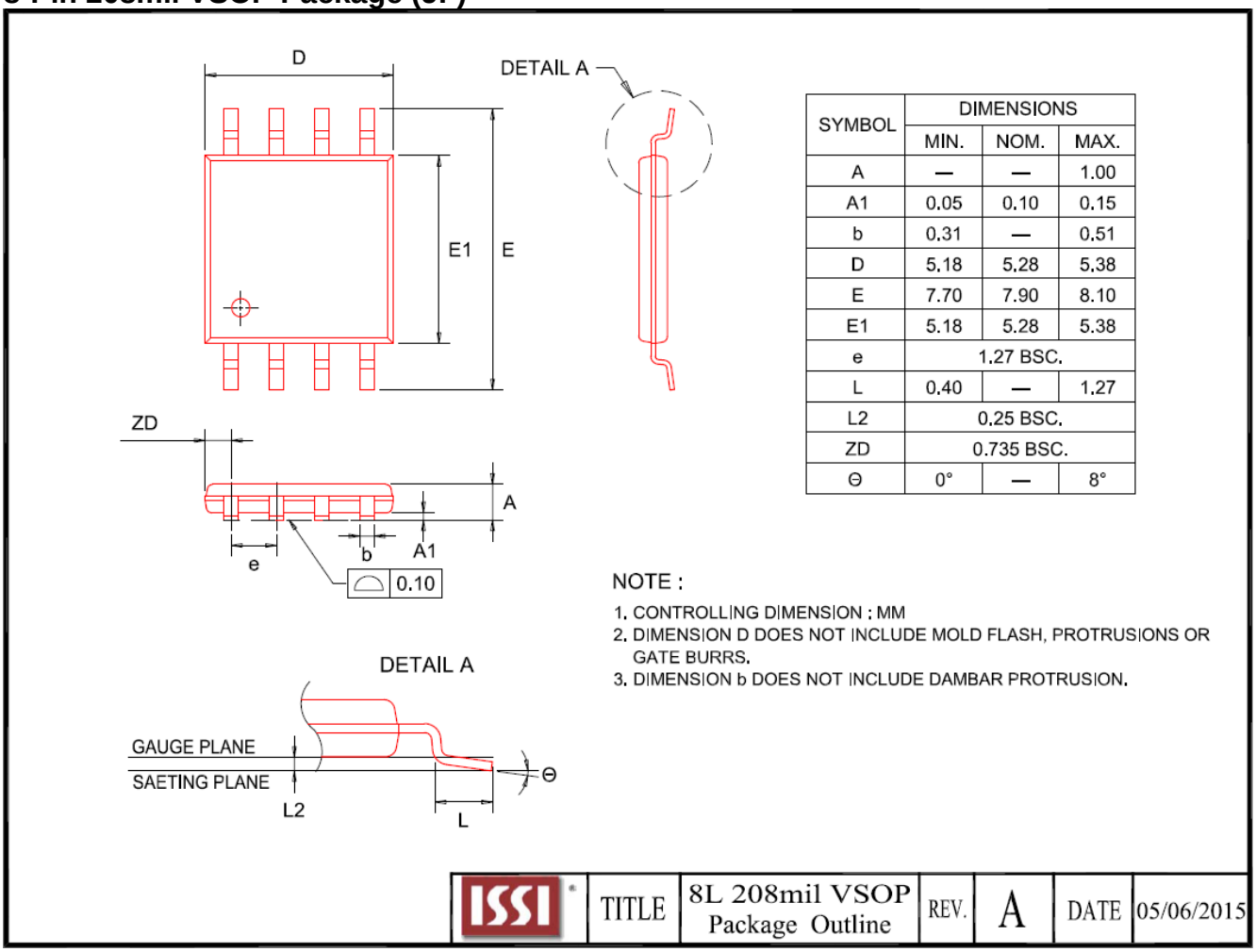
NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

ISSI	TITLE	8L 208mil SOP Package Outline	REV.	A	DATE	04/27/2015

Note: Lead co-planarity is 0.1mm.

8-Pin 208mil VSOP Package (JF)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.00
A1	0.05	0.10	0.15
b	0.31	—	0.51
D	5.18	5.28	5.38
E	7.70	7.90	8.10
E1	5.18	5.28	5.38
e	1.27 BSC.		
L	0.40	—	1.27
L2	0.25 BSC.		
ZD	0.735 BSC.		
Θ	0°	—	8°

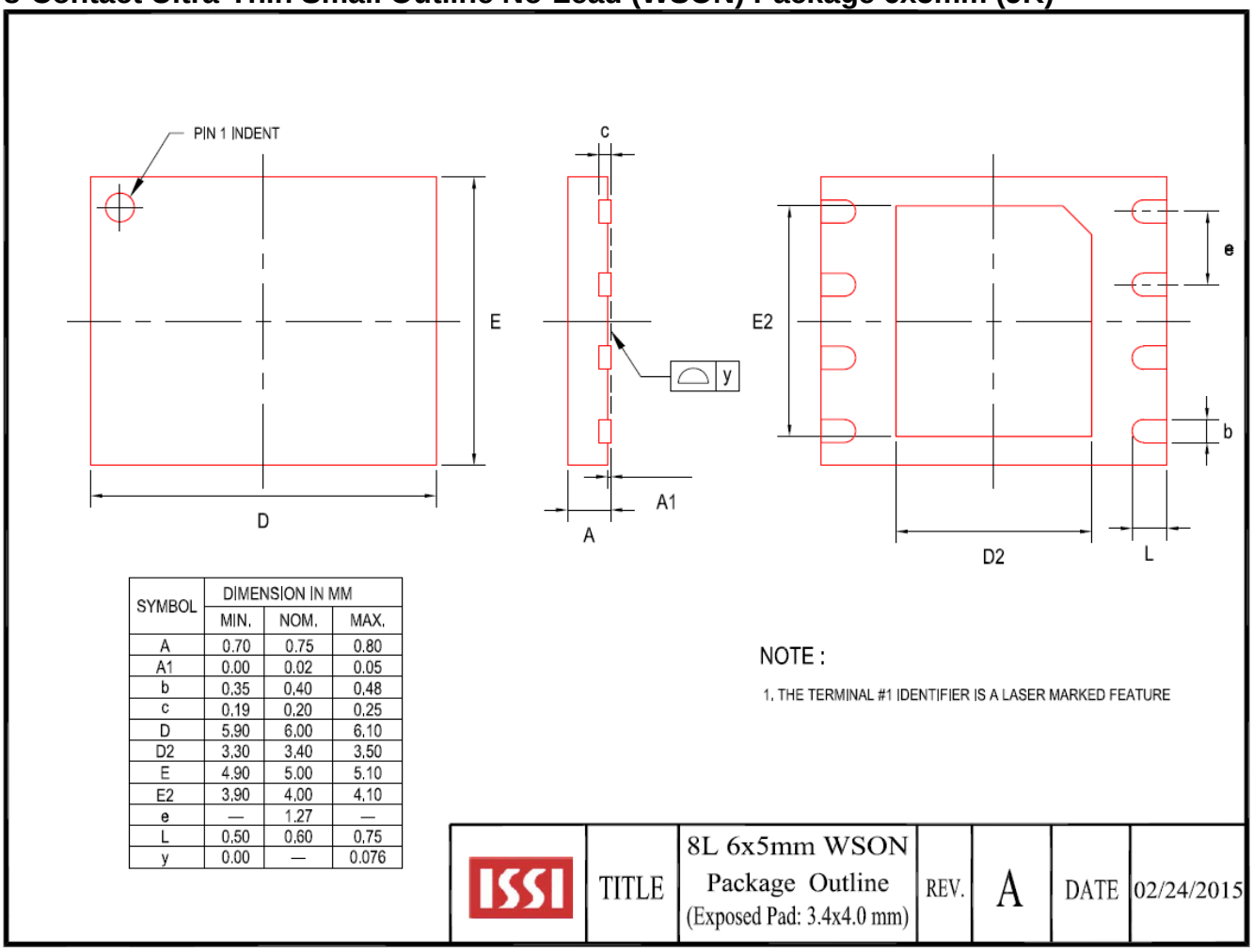
NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

ISSI	TITLE	8L 208mil VSOP Package Outline	REV.	A	DATE	05/06/2015

Note: Lead co-planarity is 0.1mm.

8-Contact Ultra-Thin Small Outline No-Lead (WSON) Package 6x5mm (JK)



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.35	0.40	0.48
c	0.19	0.20	0.25
D	5.90	6.00	6.10
D2	3.30	3.40	3.50
E	4.90	5.00	5.10
E2	3.90	4.00	4.10
e	—	1.27	—
L	0.50	0.60	0.75
y	0.00	—	0.076

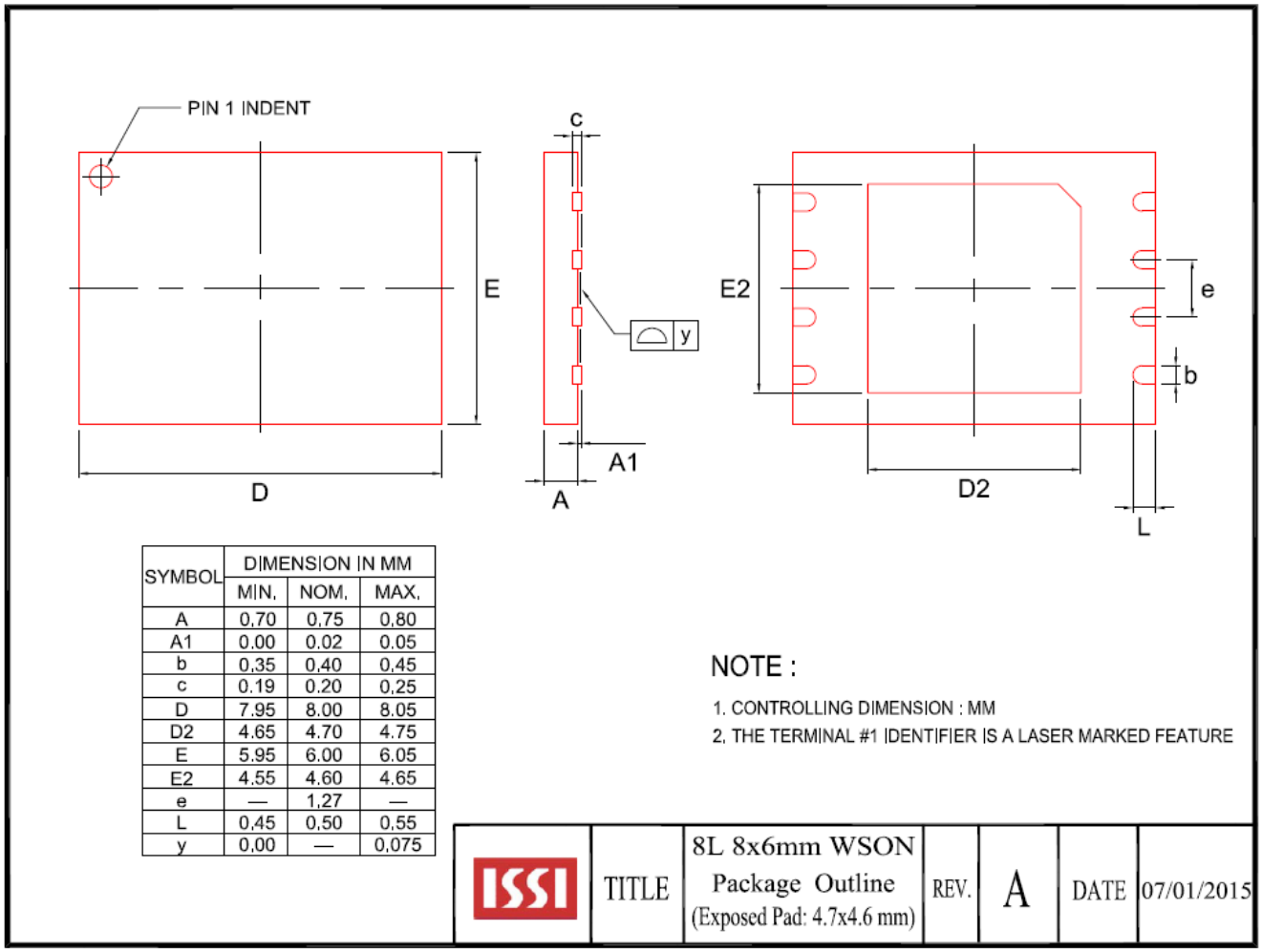
NOTE :

1. THE TERMINAL #1 IDENTIFIER IS A LASER MARKED FEATURE

ISSI	TITLE	8L 6x5mm WSON Package Outline (Exposed Pad: 3.4x4.0 mm)	REV.	A	DATE	02/24/2015

Note: Lead co-planarity is 0.08mm.

8-Contact Ultra-Thin Small Outline No-Lead (WSON) Package 8x6mm (L)



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.35	0.40	0.45
c	0.19	0.20	0.25
D	7.95	8.00	8.05
D2	4.65	4.70	4.75
E	5.95	6.00	6.05
E2	4.55	4.60	4.65
e	—	1.27	—
L	0.45	0.50	0.55
y	0.00	—	0.075

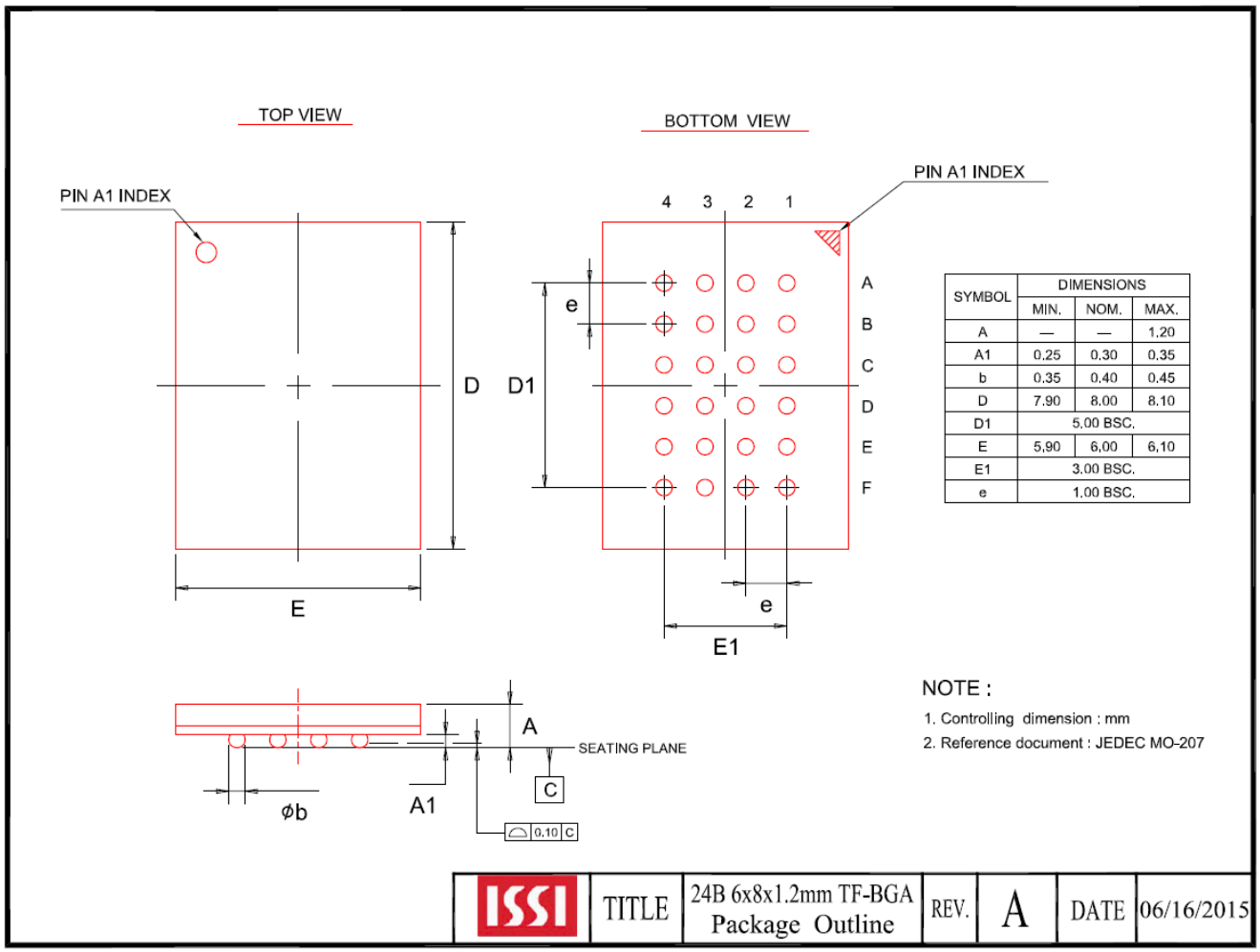
NOTE :

1. CONTROLLING DIMENSION : MM
2. THE TERMINAL #1 IDENTIFIER IS A LASER MARKED FEATURE

ISSI	TITLE	8L 8x6mm WSON Package Outline (Exposed Pad: 4.7x4.6 mm)	REV.	A	DATE	07/01/2015

Note: Lead co-planarity is 0.08mm.

24-Ball Thin Profile Fine Pitch BGA 6x8mm 4x6 array (JG)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.25	0.30	0.35
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1		5.00 BSC.	
E	5.90	6.00	6.10
E1		3.00 BSC.	
e		1.00 BSC.	

Note: Lead co-planarity is 0.08mm.

ORDERING INFORMATION:

Density	Frequency (MHz)	Temperature Range	Order Part Number	*Package
32M	104	-40°C to +105°C	IS25CQ032-JMLE	16-pin SOIC 300mil
			IS25CQ032-JBLE	8-pin SOIC 208mil
			IS25CQ032-JFLE	8-pin VSOP 208mil
			IS25CQ032-JKLE	8-pin WSON (6x5mm)
			IS25CQ032-JLLE	8-pin WSON (8x6mm)
			IS25CQ032-JGLE	24-BGA (Call Factory)
		Call Factory	KGD	KGD (Call Factory)

* Call Factory for other Package options available.

Extended Grade = E	-40^{o}C to 105^{o}C