

### General Description

- Trench Power AlphaSGT™ technology
- Low  $R_{DS(ON)}$
- Logic Driven
- RoHS and Halogen-Free Compliant

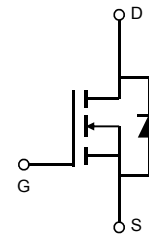
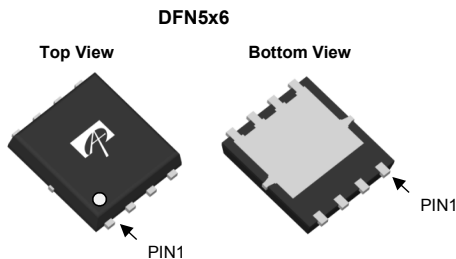
### Applications

- Synchronous Rectification for Quick Charger 3.0
- Synchronous Rectification for AC/DC adapter and DC/DC brick power

### Product Summary

$V_{DS}$	100V
$I_D$ (at $V_{GS}=10V$ )	48A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 6.2m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=4.5V$ )	< 7.4m $\Omega$

100% UIS Tested  
 100% Rg Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AON6220	DFN 5x6	Tape & Reel	3000

### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>G</sup>	$T_C=25^\circ\text{C}$	48	A
	$T_C=100^\circ\text{C}$	48	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	185	
Continuous Drain Current	$T_A=25^\circ\text{C}$	22	A
	$T_A=70^\circ\text{C}$	17.5	
Avalanche Current <sup>C</sup>	$I_{AS}$	44	A
Avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AS}$	97	mJ
$V_{DS}$ Spike	$V_{SPIKE}$	120	V
Power Dissipation <sup>B</sup>	$T_C=25^\circ\text{C}$	113.5	W
	$T_C=100^\circ\text{C}$	45.5	
Power Dissipation <sup>A</sup>	$T_A=25^\circ\text{C}$	6.2	W
	$T_A=70^\circ\text{C}$	4.0	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup> $t \leq 10\text{s}$	$R_{\theta JA}$	15	20	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A,D</sup> Steady-State		40	50	$^\circ\text{C/W}$
Maximum Junction-to-Case Steady-State	$R_{\theta JC}$	0.8	1.1	$^\circ\text{C/W}$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	100			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.3	1.75	2.3	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		5.1	6.2	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		9.3	11.3	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		100		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.68	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				48	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =50V, f=1MHz		4525		pF
C <sub>oss</sub>	Output Capacitance			345		pF
C <sub>riss</sub>	Reverse Transfer Capacitance			22.5		pF
R <sub>g</sub>	Gate resistance	f=1MHz	0.5	1.1	1.8	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =20A		65	95	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			30	45	nC
Q <sub>gs</sub>	Gate Source Charge			10		nC
Q <sub>gd</sub>	Gate Drain Charge			9		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, R <sub>L</sub> =2.5Ω, R <sub>GEN</sub> =3Ω		10		ns
t <sub>r</sub>	Turn-On Rise Time			6		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			51		ns
t <sub>f</sub>	Turn-Off Fall Time			9		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, di/dt=500A/μs		32		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, di/dt=500A/μs		162		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

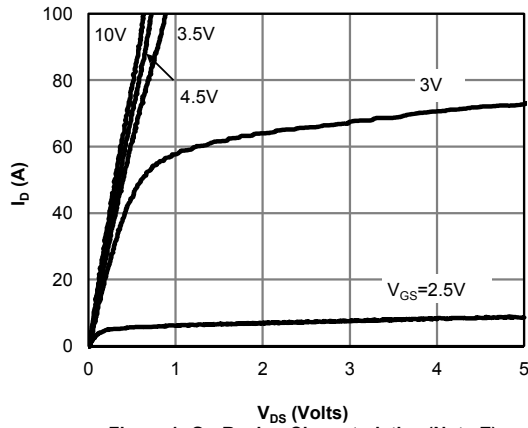
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

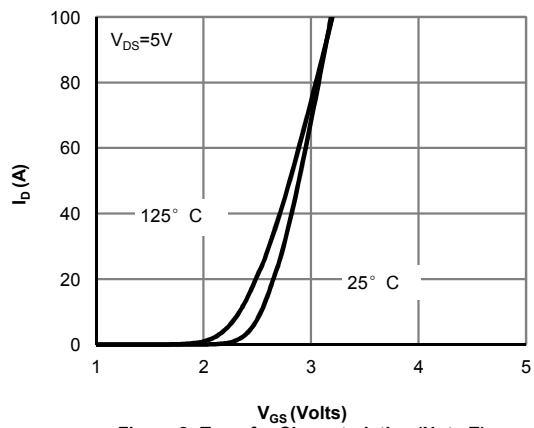
H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

APPLICATIONS OR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN,FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

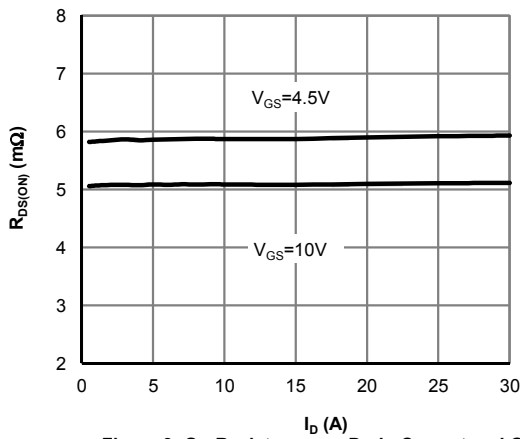
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



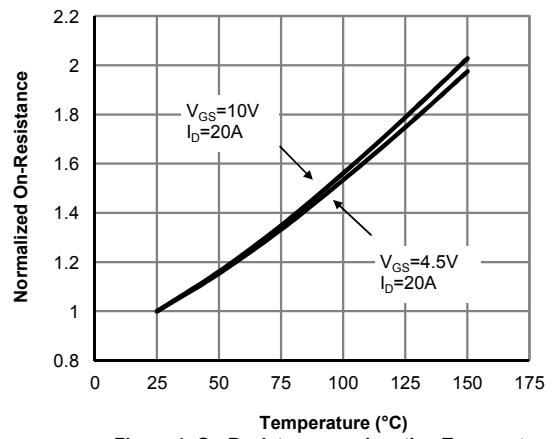
**Figure 1: On-Region Characteristics (Note E)**



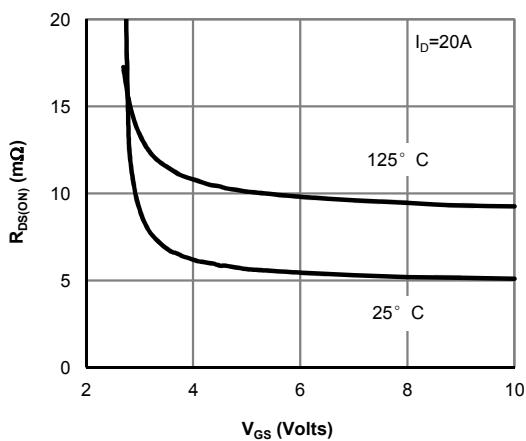
**Figure 2: Transfer Characteristics (Note E)**



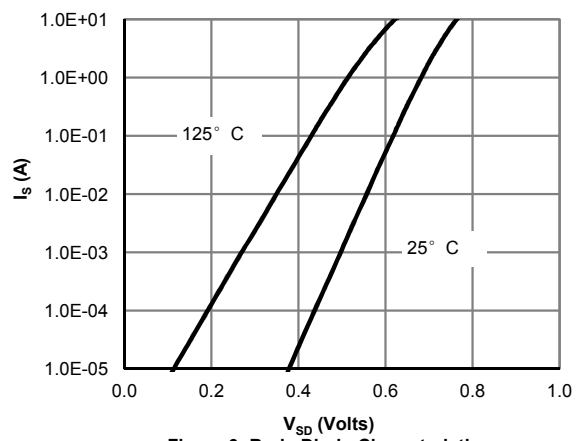
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

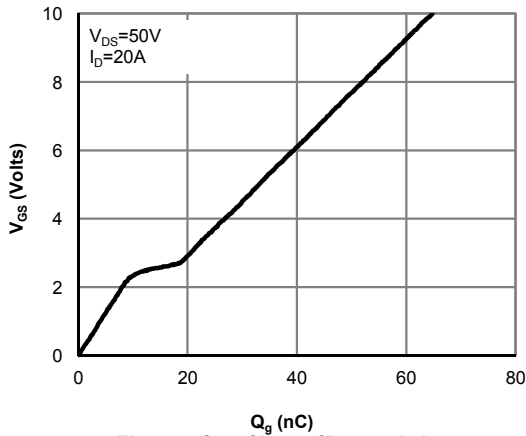


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

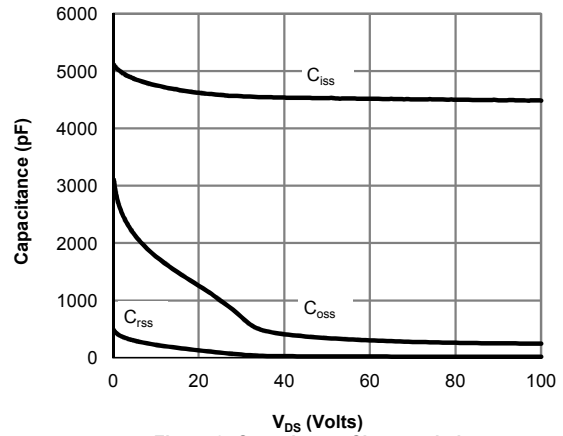


**Figure 6: Body-Diode Characteristics (Note E)**

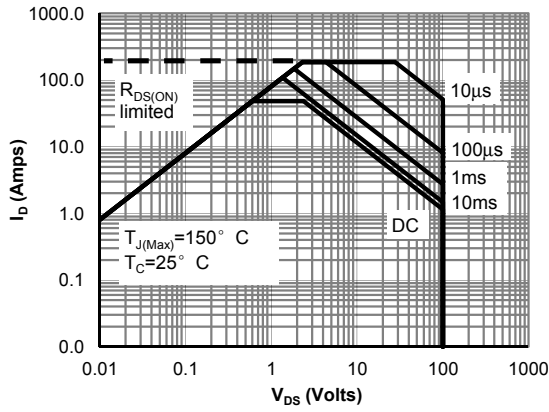
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



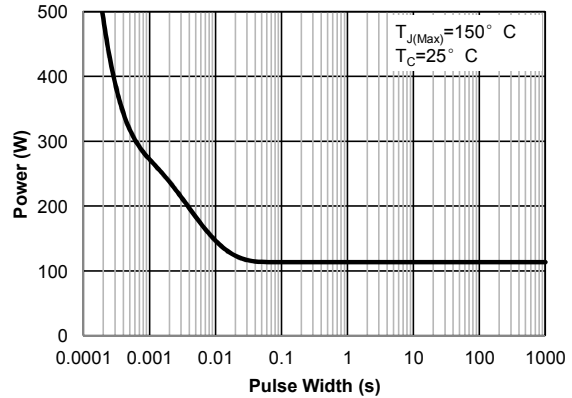
**Figure 7: Gate-Charge Characteristics**



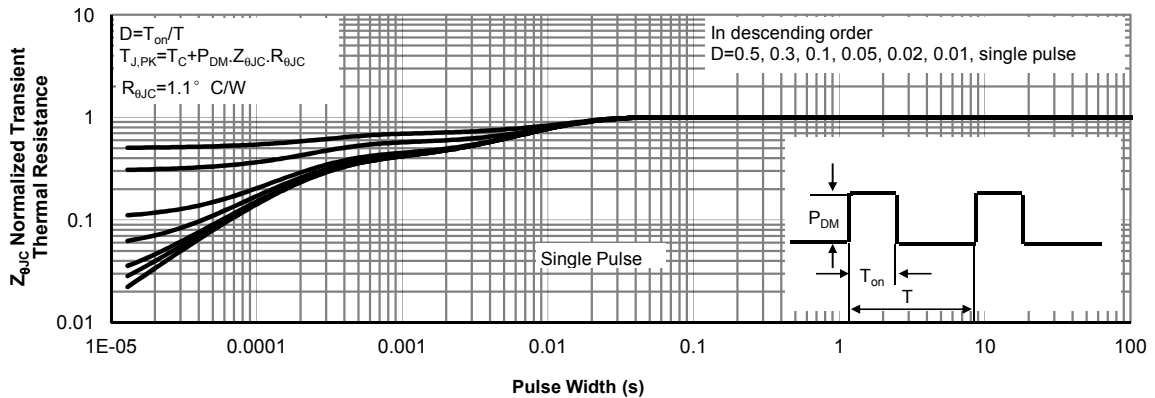
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

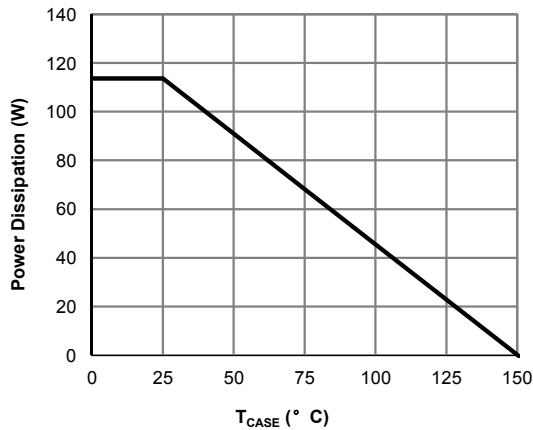


Figure 12: Power De-rating (Note F)

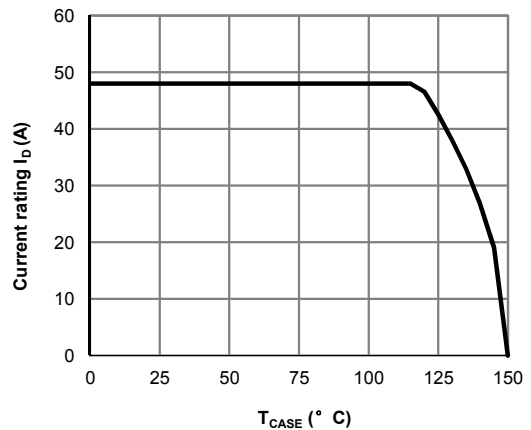


Figure 13: Current De-rating (Note F)

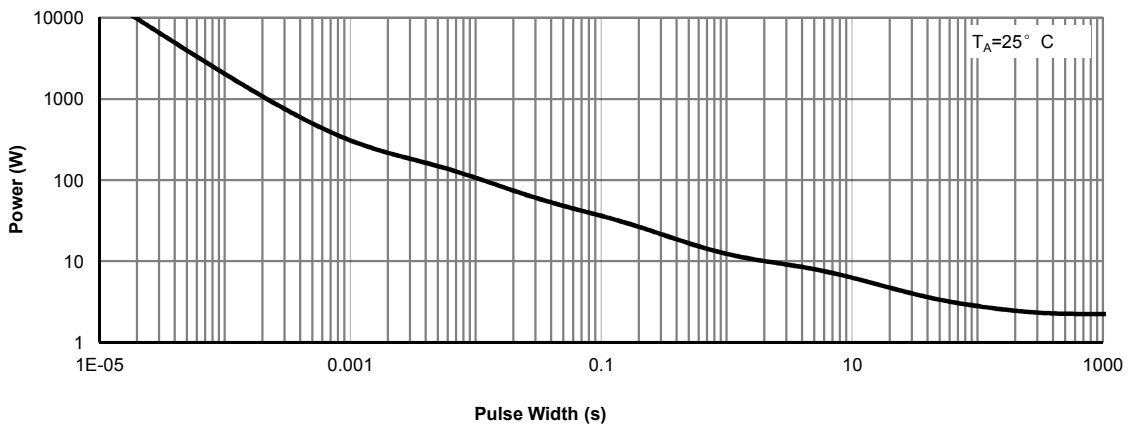


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

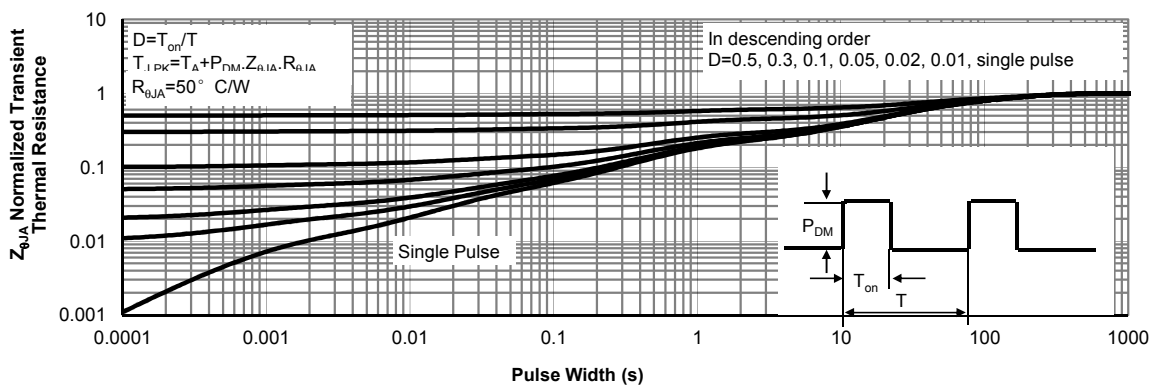


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

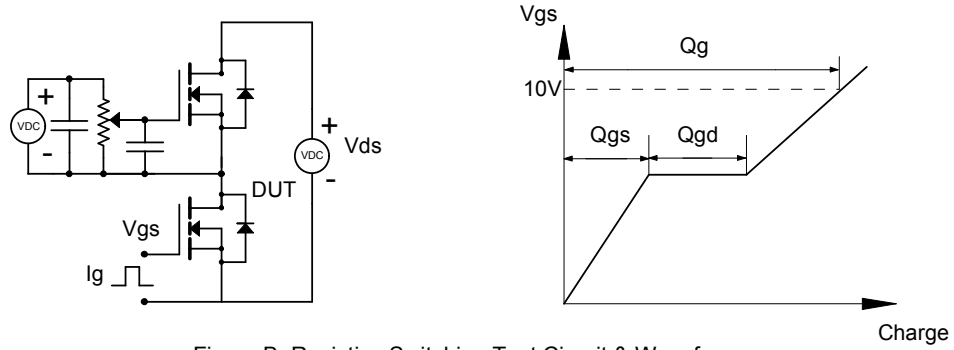


Figure B: Resistive Switching Test Circuit & Waveforms

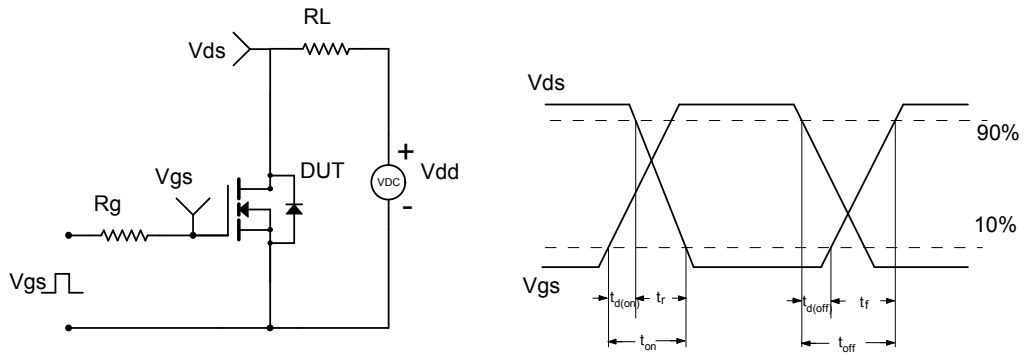


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

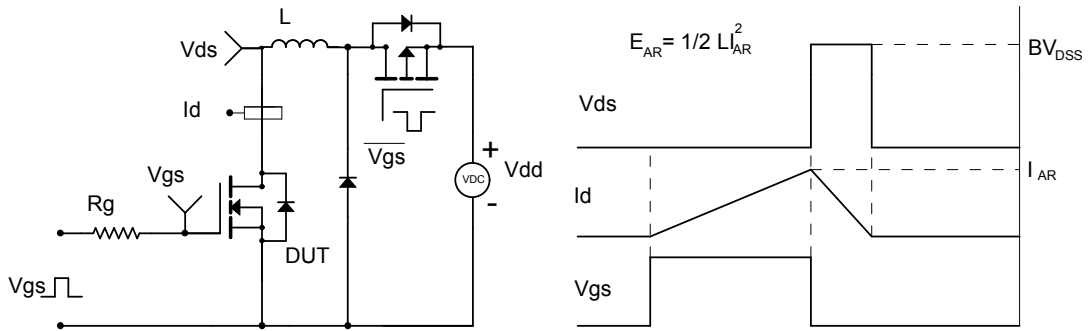


Figure D: Diode Recovery Test Circuit & Waveforms

