MJF122, MJF127

Complementary Power Darlingtons

For Isolated Package Applications

Designed for general−purpose amplifiers and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

Features

- Electrically Similar to the Popular TIP122 and TIP127
- 100 $V_{CEO(sus)}$
- 5.0 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High DC Current Gain − 2000 (Min) @ I_C = 3 Adc
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation
- Pb−Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
RMS Isolation Voltage (Note 1) (t = 0.3 sec, R.H. ≤ 30%, T_A = 25°C) Per Figure 14	V_{ISOL}	4500	V_{RMS}
Collector Current − Continuous Peak	I_C	5 8	Adc
Base Current	I_B	0.12	Adc
Total Power Dissipation (Note 2) @ T_C = 25°C Derate above 25°C	P_D	30 0.24	W W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 0.016	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	I_C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction−to−Case (Note 2)	$R_{\theta JC}$	4.1	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Proper strike and creepage distance must be provided.
2. Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.

ON Semiconductor®

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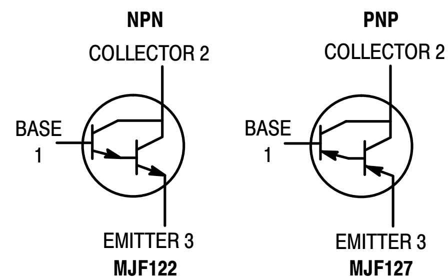
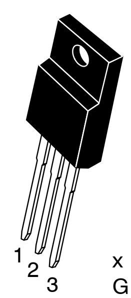
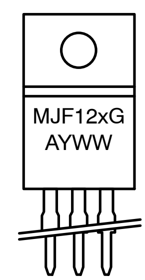
COMPLEMENTARY SILICON POWER DARLINGTONS
5.0 A, 100 V, 30 W



MARKING DIAGRAM





TO−220
CASE 221D−02
STYLE 2

x	=	2 or 7
G	=	Pb−Free Package
A	=	Assembly Location
Y	=	Year
WW	=	Work Week

ORDERING INFORMATION

Device	Package	Shipping†
MJF122	TO−220	50 Units / Rail
MJF122G	TO−220 (Pb−Free)	50 Units / Rail
MJF127	TO−220	50 Units / Rail
MJF127G	TO−220 (Pb−Free)	50 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	–	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	–	10	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	–	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	–	2	mAdc
ON CHARACTERISTICS (Note 3)				
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3 Vdc) (I_C = 3 Adc, V_{CE} = 3 Vdc)	h_{FE}	1000 2000	– –	–
Collector−Emitter Saturation Voltage (I_C = 3 Adc, I_B = 12 mAdc) (I_C = 5 Adc, I_B = 20 mAdc)	$V_{CE(sat)}$	– –	2 3.5	Vdc
Base−Emitter On Voltage (I_C = 3 Adc, V_{CE} = 3 Vdc)	$V_{BE(on)}$	–	2.5	Vdc
DYNAMIC CHARACTERISTICS				
Small−Signal Current Gain (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 MHz)	h_{fe}	4	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJF127 MJF122	C_{ob}	– –	300 200	pF

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

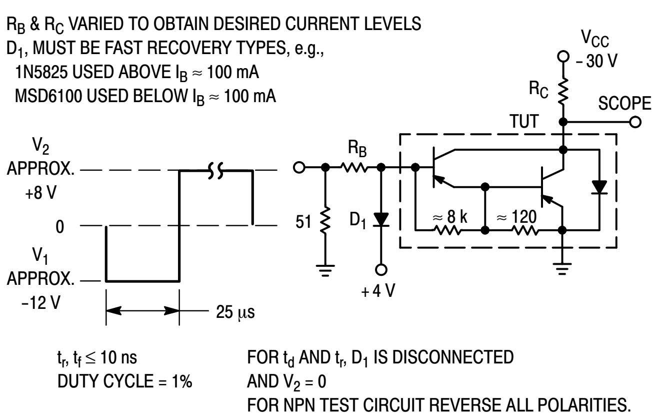


Figure 1. Switching Times Test Circuit

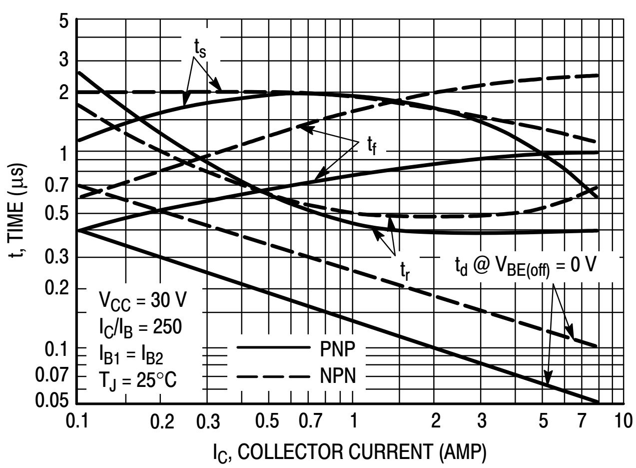


Figure 2. Typical Switching Times

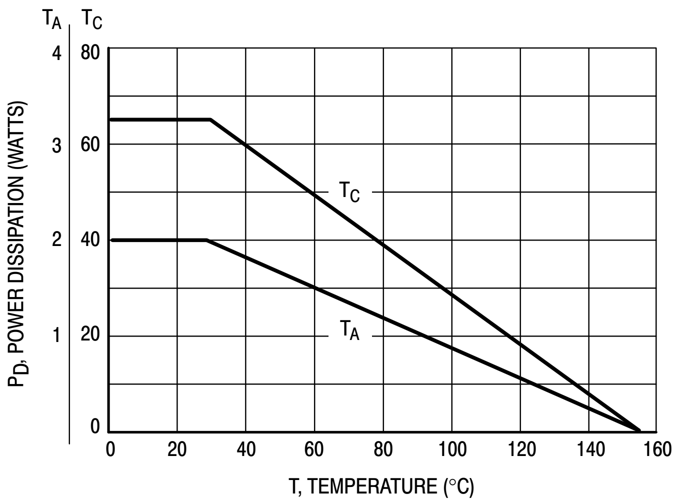


Figure 3. Maximum Power Derating

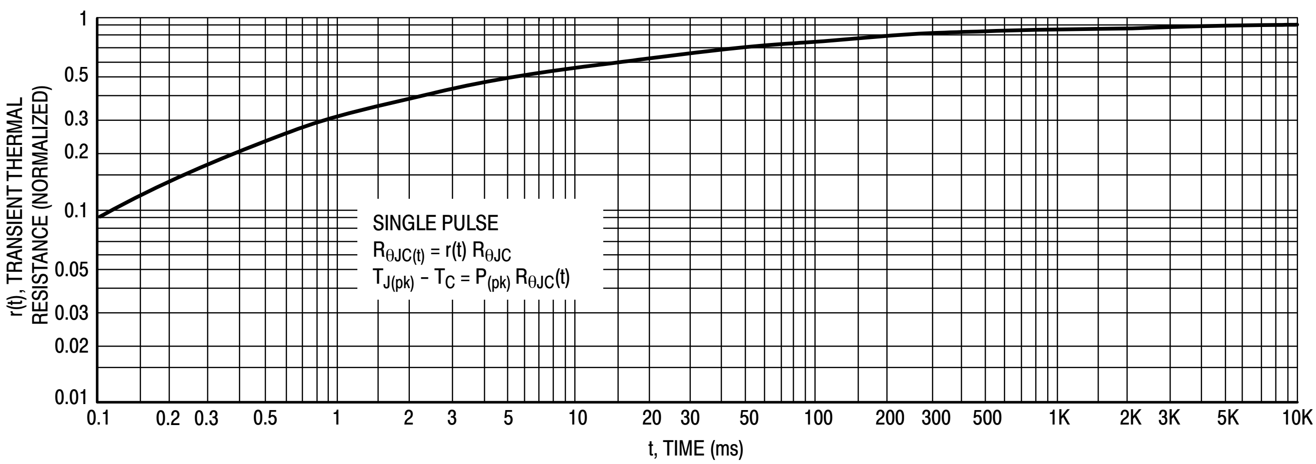


Figure 4. Thermal Response

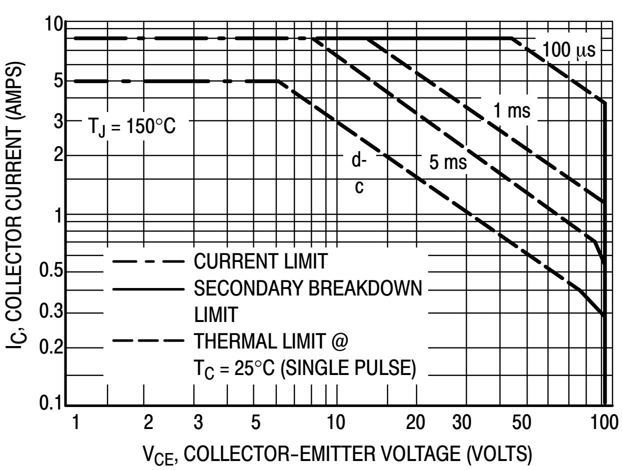


Figure 5. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

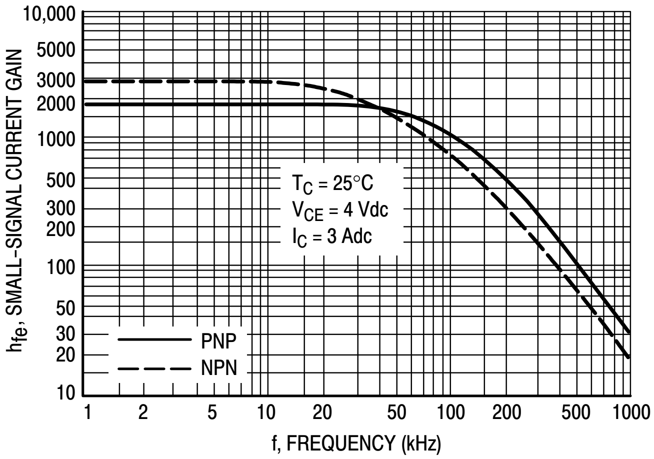


Figure 6. Typical Small−Signal Current Gain

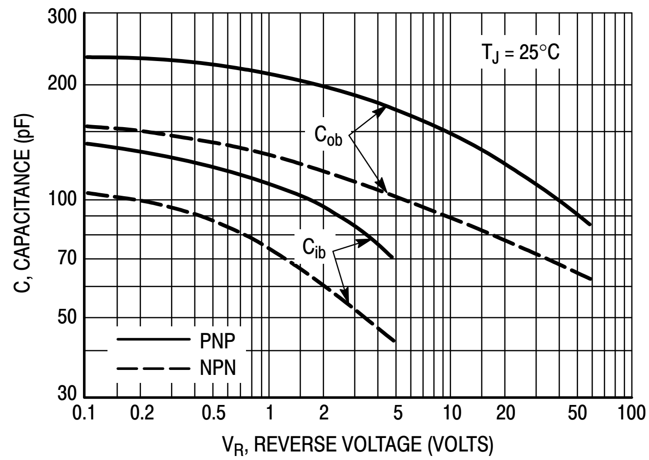
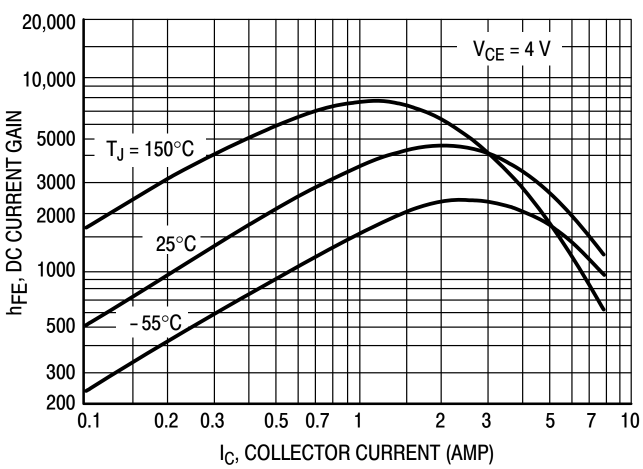


Figure 7. Typical Capacitance

NPN
MJF122



PNP
MJF127

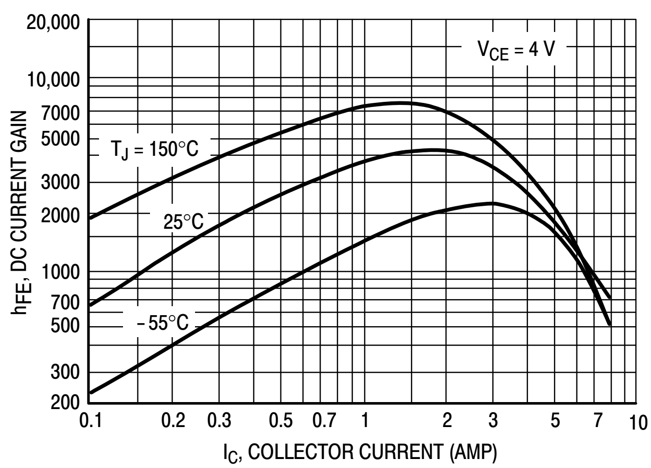
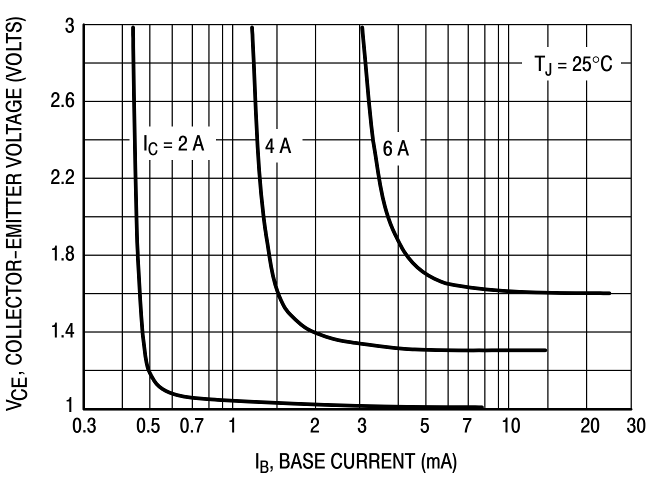


Figure 8. Typical DC Current Gain



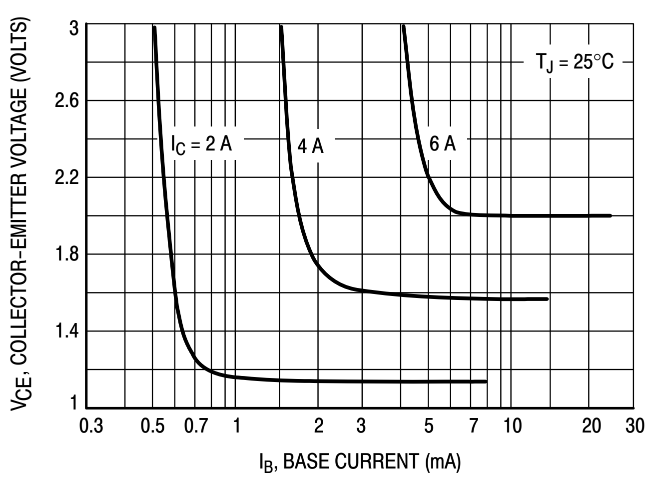


Figure 9. Typical Collector Saturation Region

NPN
MJF122

PNP
MJF127

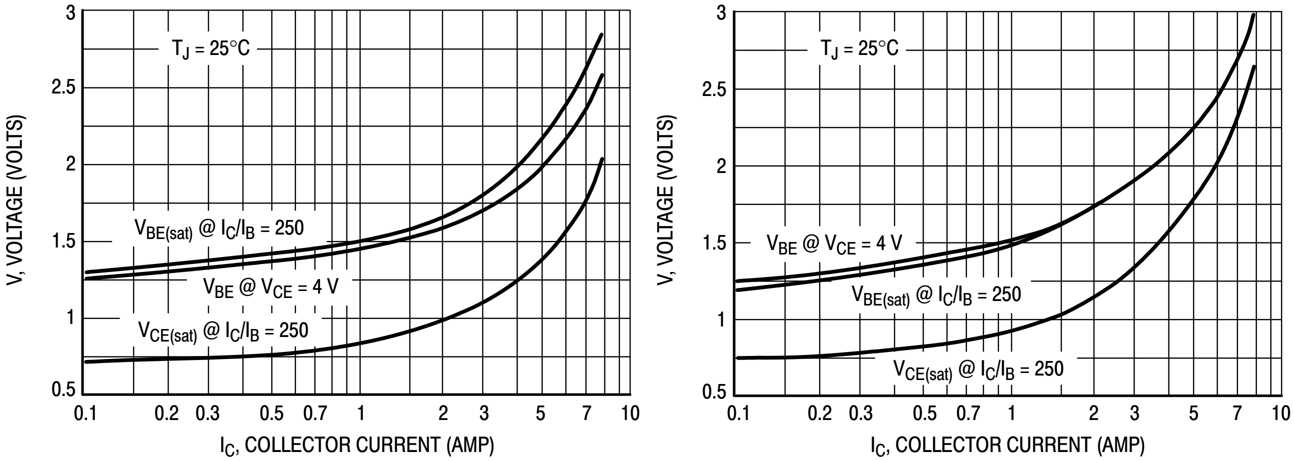


Figure 10. Typical "On" Voltages

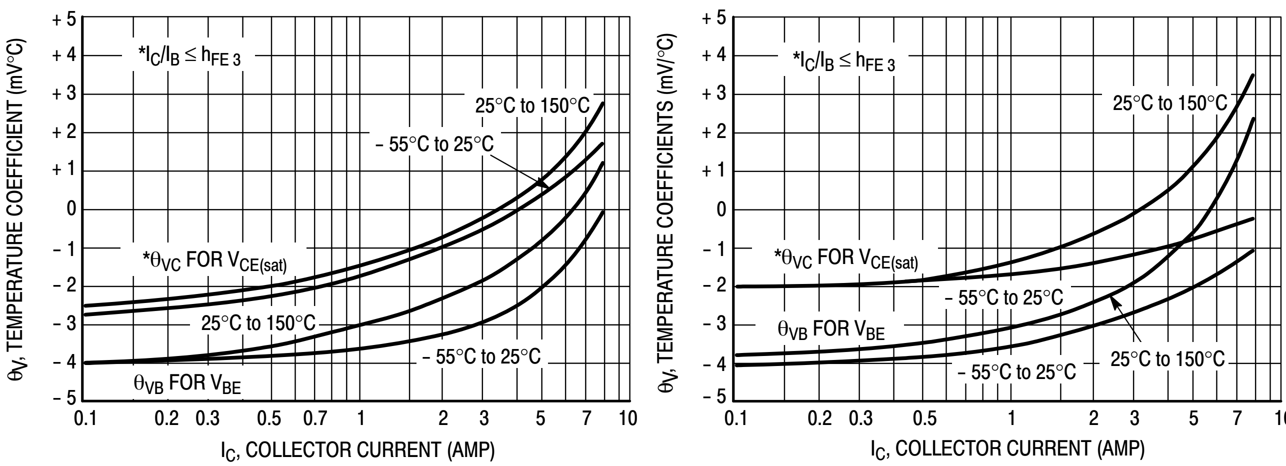


Figure 11. Typical Temperature Coefficients

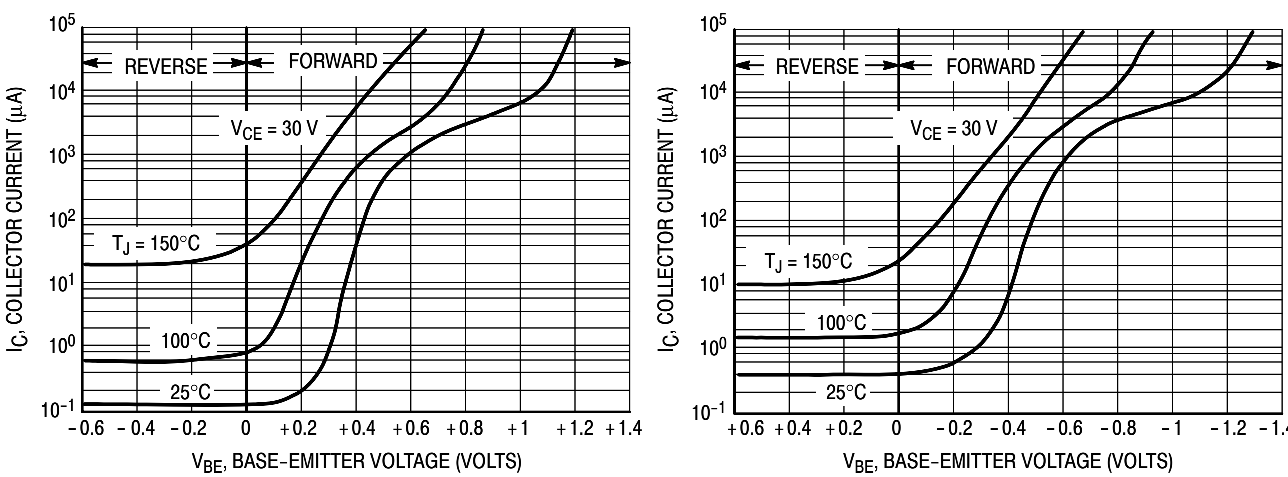


Figure 12. Typical Collector Cut−Off Region

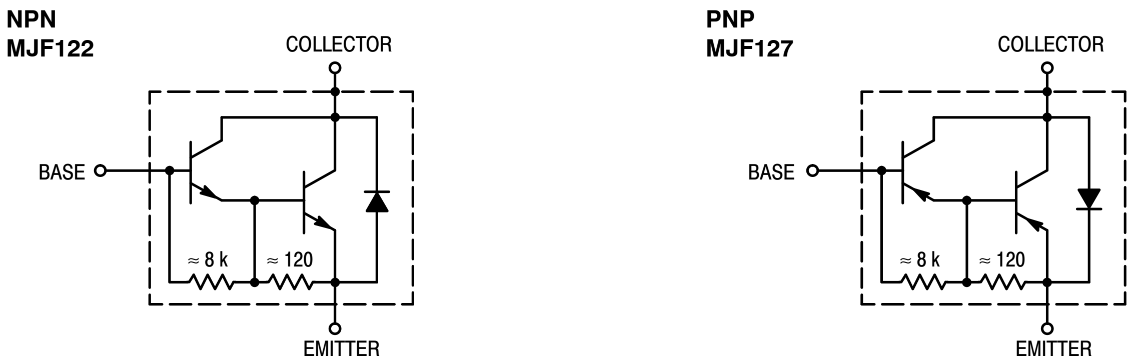


Figure 13. Darlington Schematic

TEST CONDITIONS FOR ISOLATION TESTS*

FULLY ISOLATED PACKAGE

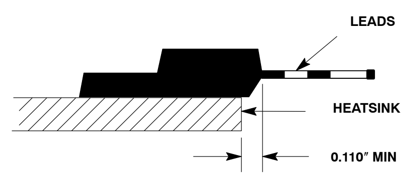


Figure 14. Mounting Position

*Measurement made between leads and heatsink with all leads shorted together.

MOUNTING INFORMATION

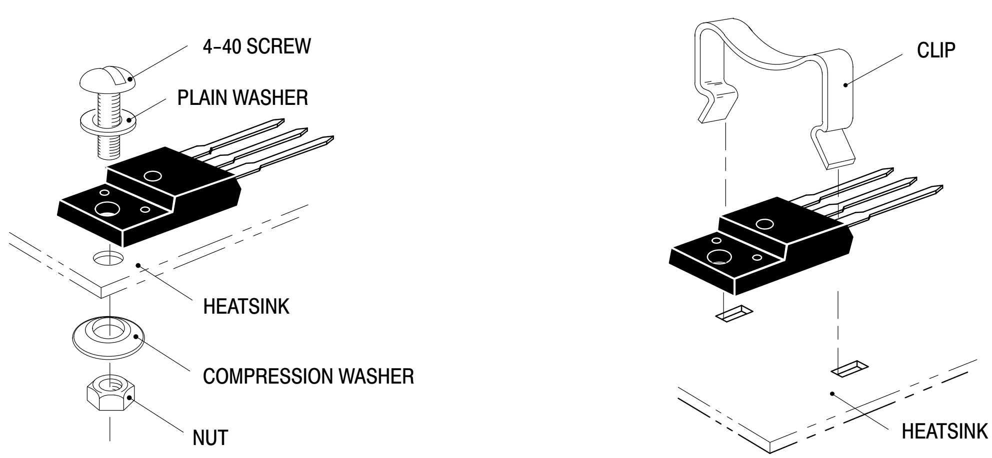


Figure 15. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

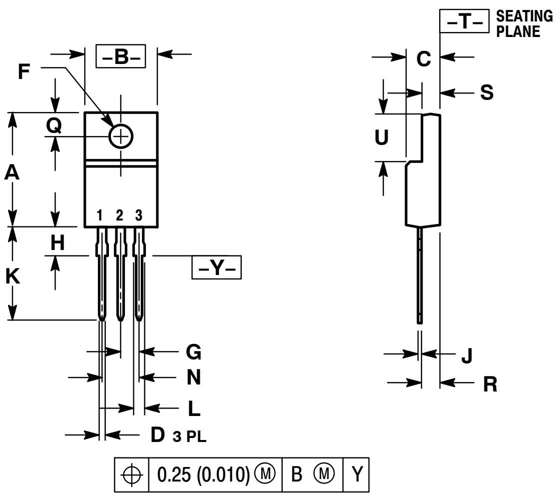
Destructive laboratory tests show that using a hex head 4−40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4−40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

PACKAGE DIMENSIONS

TO−220
CASE 221D−03
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D−01 THRU 221D−02 OBSOLETE, NEW STANDARD 221D−03.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

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