



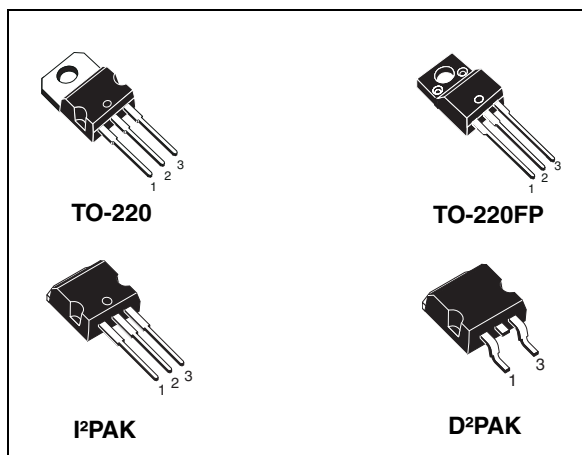
STB20NM50 - STB20NM50-1 STP20NM50 - STP20NM50FP

N-channel 500V - 0.20Ω - 20A - TO220/FP-D²PAK-I²PAK
MDmesh™ Power MOSFET

General features

Type	V _{DSS} (@T _{Jmax})	R _{DS(on)}	I _D
STB20NM50	550V	< 0.25Ω	20A
STB20NM50-1	550V	< 0.25Ω	20A
STP20NM50	550V	< 0.25Ω	20A
STP20NM50FP	550V	< 0.25Ω	20A

- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Description

The MDmesh™ is a new revolutionary Power MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics and dynamic performances.

Applications

- Switching applications

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB20NM50	B20NM50	D ² PAK	Tape & reel
STB20NM50-1	B20NM50-1	I ² PAK	Tube
STP20NM50	P20NM50	TO-220	Tube
STP20NM50FP	P20NM50FP	TO-220FP	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK / I ² PAK TO-220	TO-220FP	
V _{DS}	Drain source voltage	500		V
V _{GS}	Gate-source voltage	± 30		V
I _D	Drain current (continuous) at T _C = 25°C	20	20 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100°C	12.6	12.6 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	80	80 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25°C	192	45	W
	Derating factor	1.54	0.36	W/°C
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s; T _C =25°C)	--	2500	V
T _j T _{stg}	Operating junction temperature Storage temperature	-65 to 150		°C

- Limited only by maximum temperature allowed
- Pulse width limited by safe operating area
- I_{SD} ≤ 20A, di/dt ≤ 400A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ T_{JMAX}

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK / I ² PAK TO-220	TO-220FP	
R _{thj-case}	Thermal resistance junction-case max	0.65	2.8	°C/W
R _{thj-amb}	Thermal resistance junction-amb max	62.5		°C/W
T _l	Maximum lead temperature for soldering purpose	300		°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _j max)	10	A
E _{AS}	Single pulse avalanche energy (starting T _j =25°C, I _D = 5A, V _{DD} = 50V)	650	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 30V$			± 100	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V, I_D = 10 A$		0.20	0.25	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(ON)} \times R_{DS(ON)max},$ $I_D = 10A$		10		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1 \text{ MHz},$ $V_{GS} = 0$		1480 285 34		pF pF pF
$C_{oss \text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0V \text{ to } 400V$		130		pF
Rg	Gate input resistance	f=1MHz Gate DC Bias=0 Test Signal Level=20mV Open Drain		1.6		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 400V, I_D = 20A$ $V_{GS} = 10V$ (see Figure 15)		40 13 19	56	nC nC nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%
2. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=250\text{ V}$, $I_D=10\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 14)		24		ns
t_r	Rise time			16		ns
$t_{d(off)}$	Turn-off delay time			40		ns
t_f	Fall time			12		ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD}=400\text{ V}$, $I_D=20\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 16)		9		ns
t_f	Fall time			8.5		ns
t_c	Cross-over time				23	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current				20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				80	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=20\text{ A}$, $V_{GS}=0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD}=20\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$, $V_{DD}=100\text{ V}$, $T_j=25^\circ\text{C}$ (see Figure 16)		350		ns
Q_{rr}	Reverse recovery charge			4.6		μC
I_{RRM}	Reverse recovery current			26		A
t_{rr}	Reverse recovery time	$I_{SD}=20\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$, $V_{DD}=100\text{ V}$, $T_j=150^\circ\text{C}$ (see Figure 16)		435		ns
Q_{rr}	Reverse recovery charge			5.9		μC
I_{RRM}	Reverse recovery current			27		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration 300 μs duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220/D²PAK/I²PAK

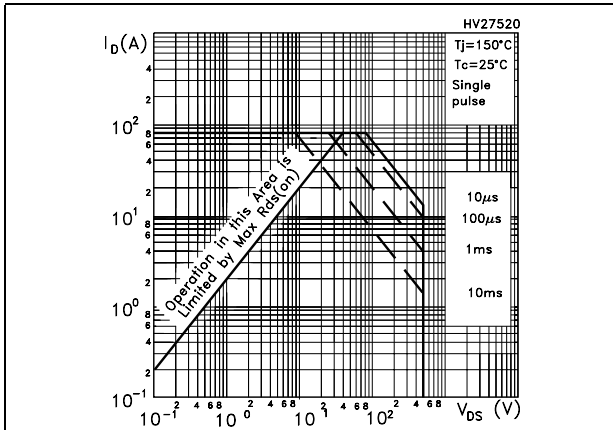


Figure 2. Thermal impedance for TO-220/D²PAK/I²PAK

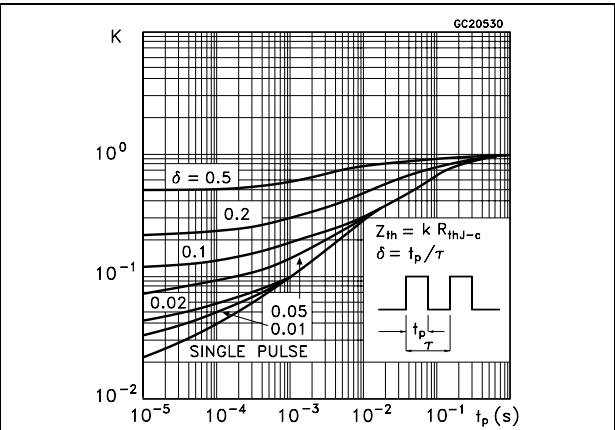


Figure 3. Safe operating area for TO-220FP

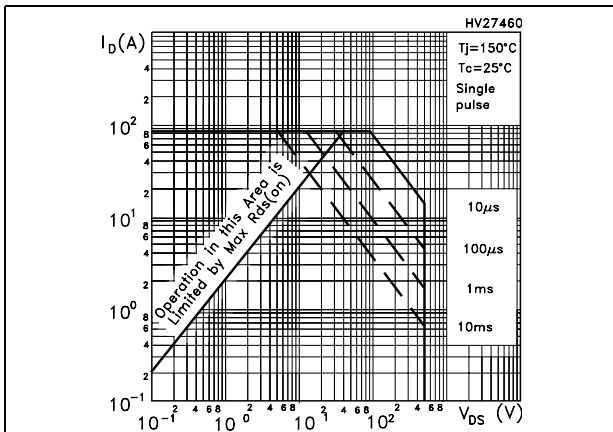


Figure 4. Thermal impedance for TO-220FP

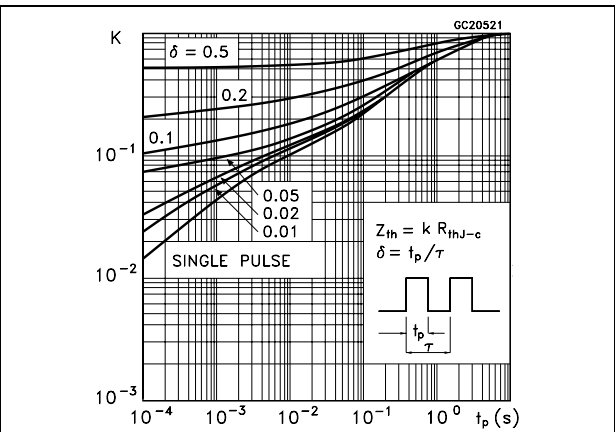


Figure 5. Output characteristics

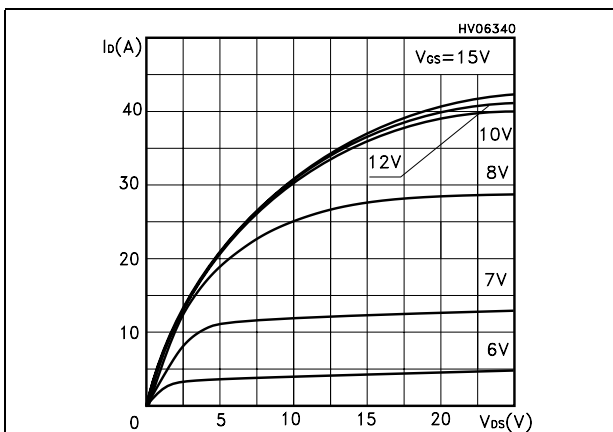


Figure 6. Transfer characteristics

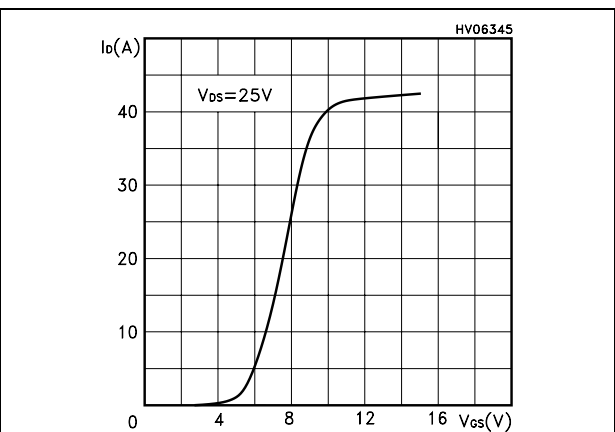


Figure 7. Transconductance

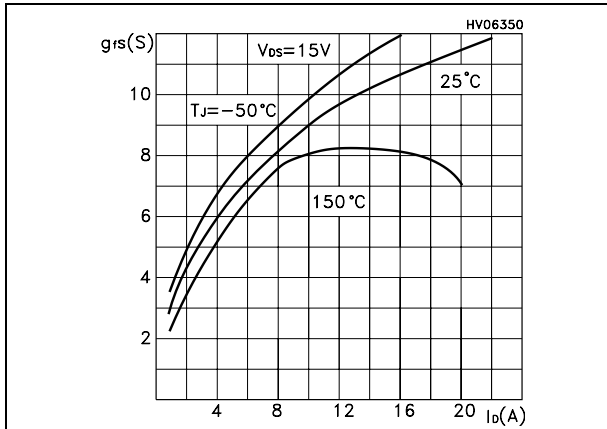


Figure 8. Static drain-source on resistance

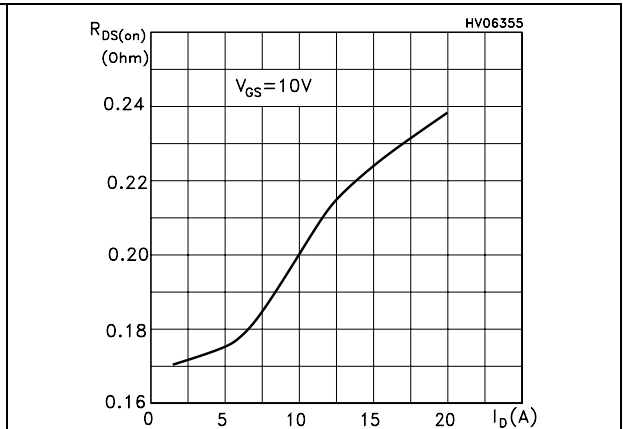


Figure 9. Gate charge vs gate-source voltage Figure 10. Capacitance variations

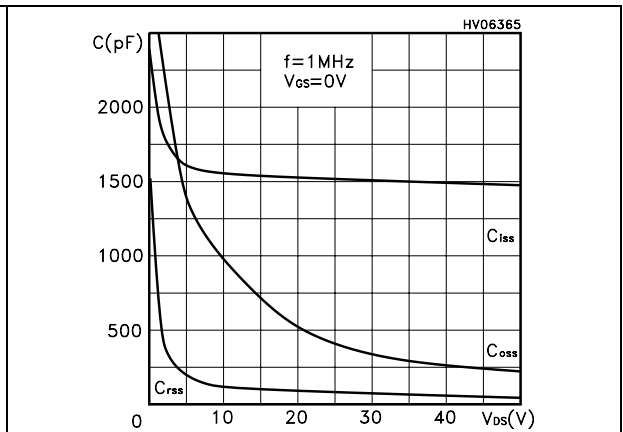
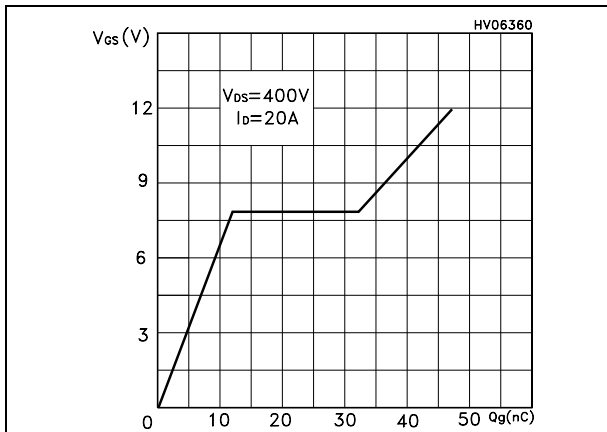


Figure 11. Normalized gate threshold voltage vs temperature

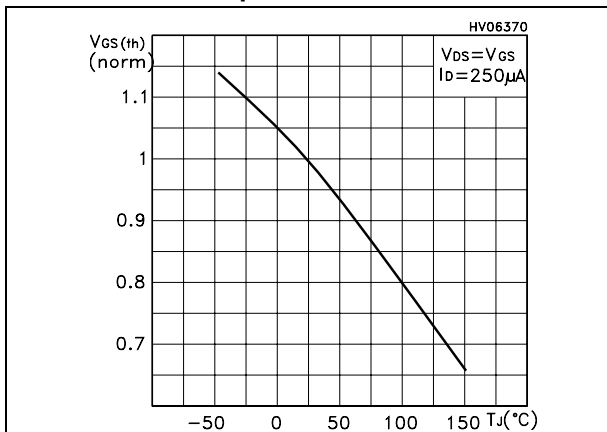


Figure 12. Normalized on resistance vs temperature

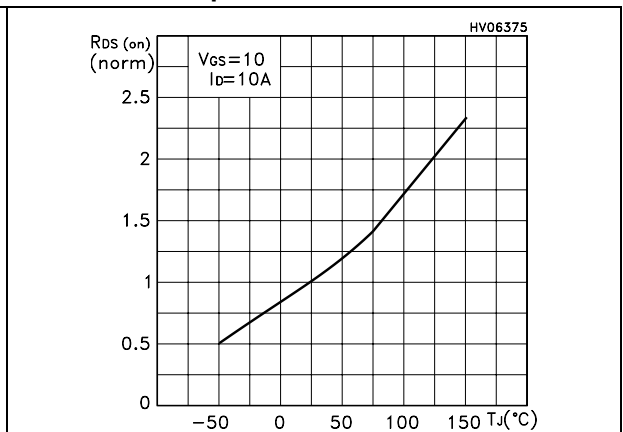
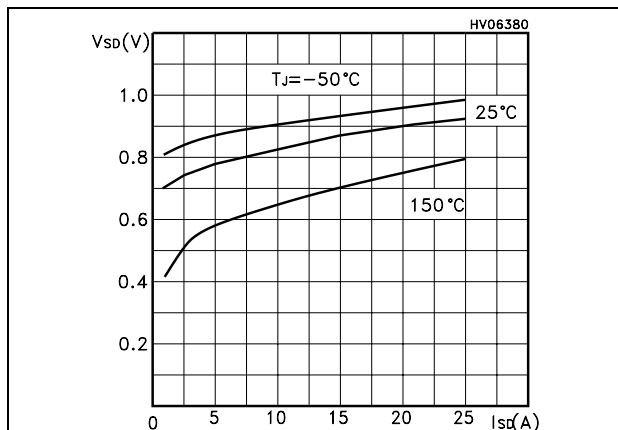


Figure 13. Source-drain diode forward characteristics



3 Test circuit

Figure 14. Switching times test circuit for resistive load

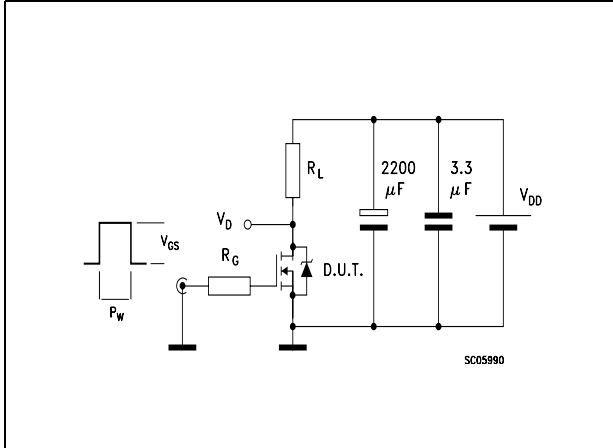


Figure 15. Gate charge test circuit



Figure 16. Test circuit for inductive load switching and diode recovery times



Figure 17. Unclamped Inductive load test circuit



Figure 18. Unclamped inductive waveform



Figure 19. Switching time waveform

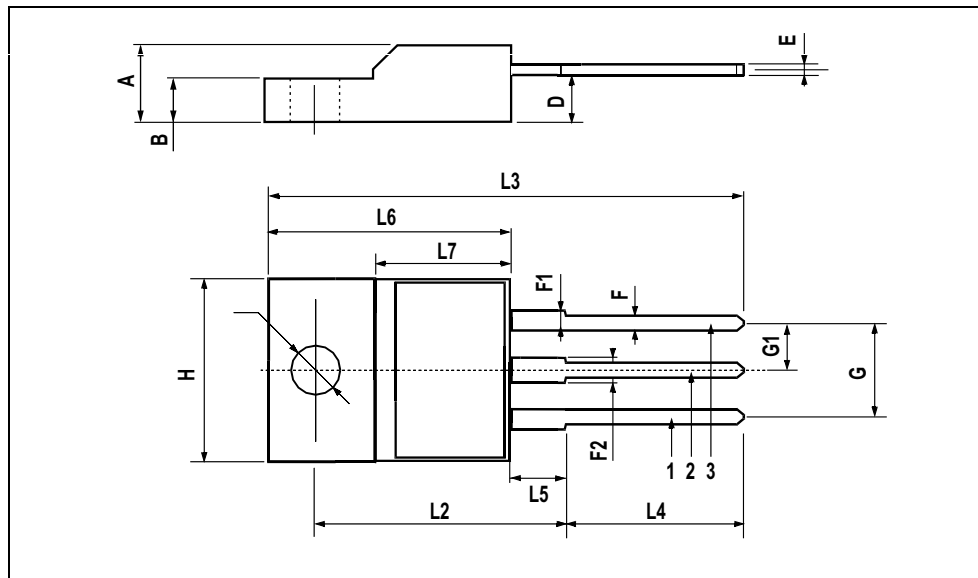


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



5 Revision history

Table 8. revision history

Date	Revision	Changes
09-Sep-2004	9	Final version
04-Sep-2006	10	The document has been reformatted
15-Dec-2006	11	Modified Table 7.: Source drain diode
08-Jan-2007	12	Modified value in order code
26-Jan-2007	13	Modified Table 6.: Switching times

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