LC87F57C8A

8-Bit Single Chip Microcontroller incorporating 128K-byte FEPROM and 3K-byte RAM on chip.

Overview

The LC87F57C8A is 8-bit single chip microcontroller with the following one-chip features:

- CPU : Operable at a minimum bus cycle time of 100ns
- On-chip Flash ROM Capacity : 128K bytes (on-board rewritable)
- On-chip RAM Capacity : 3K bytes
- two high performance 16-bit timer/counters (can be divided into 8 bit timers)
- four 8-bit timers with prescalers
- timer for use as date/time clock
- one synchronous serial I/O port (with automatic block transmit/receive function)
- one asynchronous/synchronous serial I/O port
- 12-bit PWM × 2
- 12-channel × 8-bit AD converter
- high speed 8-bit parallel interface
- high speed clock counter
- system clock divider
- 20-source 10-vectored interrupt system

Features

(1) Read Only Memory (Flash ROM)

- single 5V power supply, on-board writeable
- block erase in 128 byte units
- 131072 × 8 bits (LC87F57C8A)

(2) Bus Cycle Time

- 100ns (10MHz)

Note: Bus cycle time indicates the speed to read ROM.

(3) Minimum Instruction Cycle Time : 300ns (10MHz)

(4) Ports

- Input/output ports	
Input/output programmable for each bit individually	43 (P1n, P2n, P70 to P73, P8n, PAn, PBn, PCn)
Data direction programmable in nibble units	8 (P0n)
- Input ports	2 (XT1, XT2)
- PWM output ports	2 (PWM0, PWM1)
- Oscillator pins	2 (CF1, CF2)
- Reset pin	1 ($\overline{\text{RES}}$)
- Power supply	6 (VSS1 to 3, VDD1 to 3)

(5) Timer

- Timer 0 : 16-bit timer/counter with capture register
  - Mode 0: Two 8-bit timers with programmable 8-bit prescaler and 8-bit capture register
  - Mode 1: 8-bit timer with 8-bit programmable prescaler and 8-bit capture register + 8-bit counter with 8-bit capture register
  - Mode 2: 16-bit timer with 8-bit programmable prescaler and 16-bit capture register
  - Mode 3: 16-bit counter with 16-bit capture register

- Timer 1 : PWM/16-bit timer/counter with toggle output
  - Mode 0: 8-bit timer (with toggle output) + 8-bit timer/counter (with toggle output)
  - Mode 1: Two 8-bit PWM
  - Mode 2: 16-bit timer/counter (with toggle output) Toggle output is also possible by using the lower order 8 bits.
  - Mode 3: 16 bit timer (with toggle output) The lower order 8 bits can be used as PWM output.

- Timer 4: 8-bit timer with 6-bit prescaler
- Timer 5: 8-bit timer with 6-bit prescaler
- Timer 6: 8-bit timer with 6-bit prescaler
- Timer 7: 8-bit timer with 6-bit prescaler

- Base timer
  1. Clock for the base timer is selectable from sub-clock (32.768kHz crystal oscillation), system clock or programmable prescaler output of timer 0.
  2. There can be five separate interrupt sources.

(6) High speed clock counter

1. Maximum of 20MHz possible (when using a 10MHz main clock).
2. Real-time output

(7) Serial interface

- SIO 0: 8 bit synchronous serial interface
  1. LSB first/MSB first-function available
  2. An internal 8-bit baud-rate generator (maximum transmit clock period 4/3 T_{CYC})
  3. Consecutive automatic data communication (1 - 256 bits)

- SIO 1: 8 bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8 bit serial IO (2-wire or 3-wire, transmit clock 2 - 512 T_{CYC})
  - Mode 1: Asynchronous serial IO (half duplex, 8 data bits, 1 stop bit, baud-rate 8 - 2048 T_{CYC})
  - Mode 2: Bus mode 1 (start bit, 8 data bits, transmit clock 2 - 512 T_{CYC})
  - Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

(8) AD converter
- 12-channel × 8-bit AD converter

(9) PWM
- 2 channel × synchronous variable 12 bit PWM

(10) Parallel interface
- RS, $\overline{RD}$, $\overline{WR}$, $\overline{CS0}$ outputs (polarity can be toggled)
- read/write possible in 1 T_{CYC}

(11) Remote receiver circuit (share with P73/INT3/T0IN terminal)
- Noise rejection function (The filtering time of the noise rejection filter ($1T_{CYC}$/32 T_{CYC}/128 T_{CYC}) can be switched by program.)

(12) Watchdog timer
- External RC circuit is required.
- Interrupt or system reset is activated when the timer overflows.

(13) Interrupts
- 20-source and 10-vectored interrupt function:
  1. Three interrupt priorities, low (L), high (H) and highest (X) are supported with multi-level nesting possible. During interrupt handling, an equal or lower level interrupt request is refused.
  2. If interrupt requests for two or more vector addresses occur at once, the higher level interrupt takes precedence. In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector	Selectable Level	Interrupt signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/Base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/T4/T5/PWM0, PWM1

• Priority Level: X > H > L
• For equal priority levels, vector with lowest address takes precedence.

(14) Subroutine stack levels
- A maximum of 1536 levels (set stack inside RAM)

(15) Multiplication and division
- 16 bits × 8 bits (5 instruction-cycle times)
- 24 bits × 16 bits (12 instruction-cycle times)
- 16 bits ÷ 8 bits (8 instruction-cycle times)
- 24 bits ÷ 16 bits (12 instruction-cycle times)

(16) Oscillation circuits
- Built-in RC oscillation circuit used for the system clock
- CF oscillation circuit used for the system clock
- Crystal oscillation circuit used for the system clock
- Built-in frequency variable RC oscillation circuit used for the system clock

(17) System clock divider
- operable on the lowest power consumption
- Minimum instruction cycle time (300ns, 600ns, 1.2µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, 76.8µs can be switched by program (when using 10MHz main clock)

(18) Standby function

- HALT mode

  The HALT mode stops program execution while the peripheral circuits keep operating and minimizes power consumption. This operation mode can be released by a system reset or an interrupt request.

- HOLD mode

  The HOLD mode stops program execution and all oscillation circuits: CF, RC and Crystal oscillations. This mode can be released by the following conditions.

  1. Supply "L" level to the reset terminal ($\overline{\text{RES}}$)
  2. Supply the selected level to at lease one of INT0, INT1, INT2, INT4 INT5.
  3. Supply an interrupt condition to Port 0.

- X'tal HOLD mode

  The X'tal HOLD mode stops program execution and all peripheral circuits except for the base timer. The crystal oscillator maintains its state at HOLD mode inception. This mode can be released by the following conditions.

  1. Supply "L" level to the reset terminal ($\overline{\text{RES}}$).
  2. Supply the selected level to at least one of INT0, INT1, INT2, INT4, INT5
  3. Supply an interrupt condition to Port 0.
  4. Supply an interrupt condition to the base timer circuit.

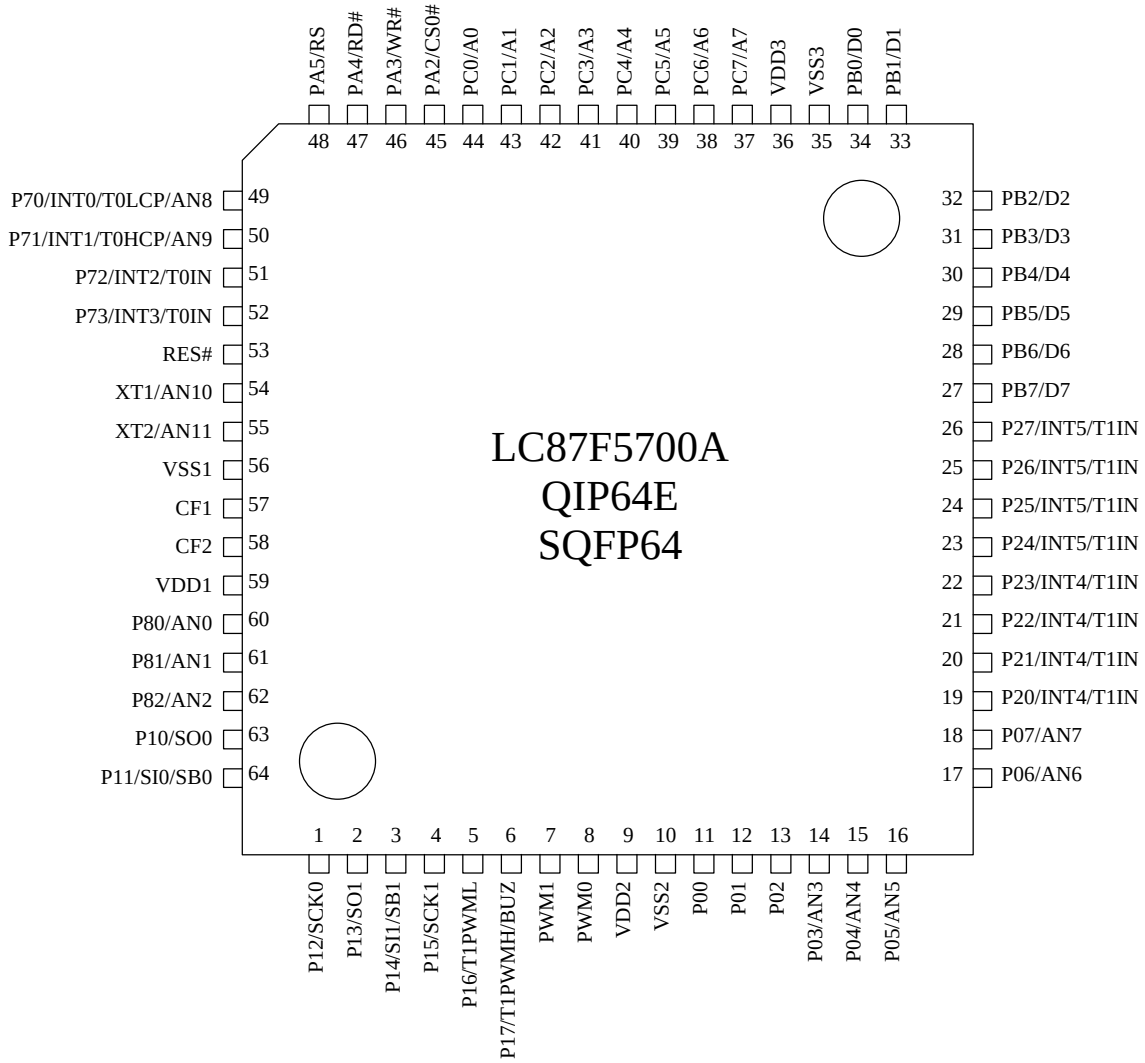
(19) Shipping form

- QIP64E
- SQFP64

(20) Development tools

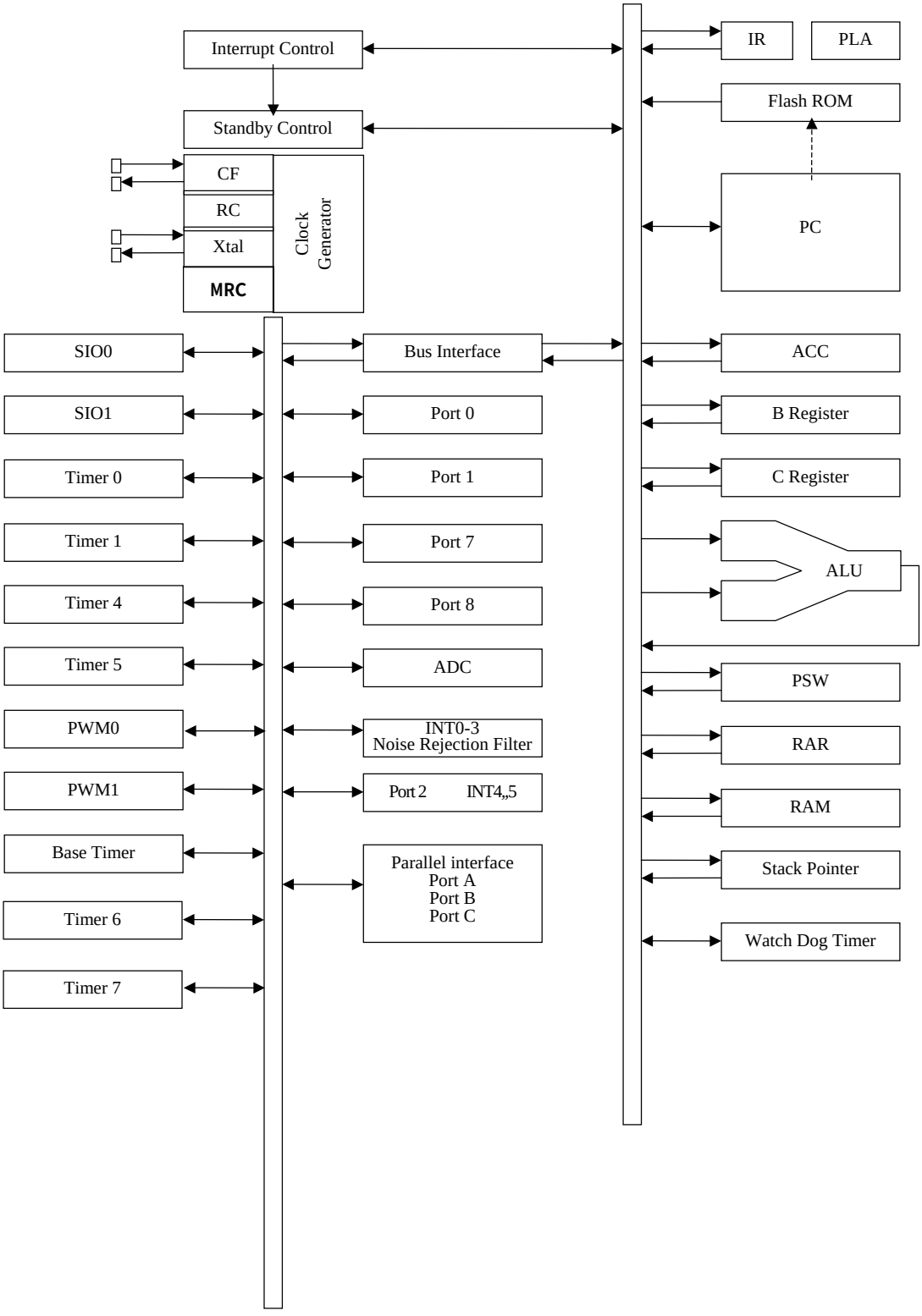
- Evaluation (EVA) chip : LC876093
- Emulator : EVA62S + ECB876600A + SUB875700 + POD64QFP or POD64SQFP
- Flash ROM writer adapter :W87F50256Q(QIP64E),W87F57256SQ(SQFP64)

Pin Assignment



QIP /SQFP	NAME	QIP /SQFP	NAME
1	P12/SCK0	33	PB1/D1
2	P13/SO1	34	PB0/D0
3	P14/SI1/SB1	35	VSS3
4	P15/SCK1	36	VDD3
5	P16/T1PWML	37	PC7/A7
6	P17/T1PWMH/BUZ	38	PC6/A6
7	PWM1	39	PC5/A5
8	PWM0	40	PC4/A4
9	VDD2	41	PC3/A3
10	VSS2	42	PC2/A2
11	P00	43	PC1/A1
12	P01	44	PC0/A0
13	P02	45	PA2/CS0#
14	P03/AN3	46	PA3/WR#
15	P04/AN4	47	PA4/RD#
16	P05/AN5	48	PA5/RS
17	P06/AN6	49	P70/INT0/T0LCP/AN8
18	P07/AN7	50	P71/INT1/T0HCP/AN9
19	P20/INT4/T1IN	51	P72/INT2/T0IN
20	P21/INT4/T1IN	52	P73/INT3/T0IN
21	P22/INT4/T1IN	53	RES#
22	P23/INT4/T1IN	54	XT1/AN10
23	P24/INT5/T1IN	55	XT2/AN11
24	P25/INT5/T1IN	56	VSS1
25	P26/INT5/T1IN	57	CF1
26	P27/INT5/T1IN	58	CF2
27	PB7/D7	59	VDD1
28	PB6/D6	60	P80/AN0
29	PB5/D5	61	P81/AN1
30	PB4/D4	62	P82/AN2
31	PB3/D3	63	P10/SO0
32	PB2/D2	64	P11/SI0/SB0

System Block Diagram



Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>VSS1, VSS2
VSS3</td><td>-</td><td>Power terminal (-)</td><td>No</td></tr>
<tr><td>VDD1, VDD2
VDD3</td><td>-</td><td>Power terminal (+)</td><td>No</td></tr>
<tr><td>Port 0
P00 - P07</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable in nibble units
• Pull-up resistor provided/not provided (specified in nibble units)
• HOLD release input
• Port 0 interrupt input
• AD converter input port : AN3 (P03)- AN7 (P07)</td><td>Yes</td></tr>
<tr><td>Port 1
P10 - P17</td><td>I/O</td><td>•8-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)
• Other functions
P10: SIO0 data output
P11: SIO0 data input, bus input/output
P12: SIO0 clock input/output
P13: SIO1 data output
P14: SIO1 data input, bus input/output
P15: SIO1 clock input/output
P16: Timer 1 PWML output
P17: Timer 1 PWMH output/Buzzer output</td><td>Yes</td></tr>
<tr><td>Port 2
P20 - P27</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)
• Other functions
P20-P23: INT4 input/HOLD release input/Timer 1 event input/Timer 0L capture input/Timer 0H capture input
P24-P27: NT5 input/HOLD release input/Timer 1 event input/Timer 0L capture input/Timer 0H capture input

• Interrupt detection style
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 7
P70 - P73</td><td>I/O</td><td>• 4-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)
• Other functions
P70: INT0 input/HOLD release input/Timer 0L capture input/Output for watchdog timer
P71: INT1 input/HOLD release input/Timer 0H capture input
P72: INT2 input/HOLD release input/Timer 0 event input/Timer0L capture input
P73: INT3 input with noise filter/Timer 0 event input/Timer 0H capture input

• Interrupt detection style
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table>
• AD converter input port : AN8 (P70), AN9 (P71)</td><td>No</td></tr>
</table>

(Continued)

Name	I/O	Function description	Option
Port 8 P80 - P82	I/O	• 3-bit input/output port • Data direction programmable for each bit individually • Other functions P80-P82 : AD converter input port	No
Port A PA2 - PA5	I/O	• 4-bit input/output port • Data direction programmable for each bit individually • Pull-up resistor provided/not provided (specified by bit) • Other functions PA2: Parallel interface output $\overline{CS0}$ PA3: Parallel interface output $\overline{WR}$ PA4: Parallel interface output $\overline{RD}$ PA5: Parallel interface output RS	Yes
Port B PB0 - PB7	I/O	• 8-bit input/output port • Data direction programmable for each bit individually • Pull-up resistor provided/not provided (specified by bit) • Other functions PB0-PB7 : Parallel interface data input/output, address output	Yes
Port C PC0 - PC7	I/O	• 8-bit input/output port • Data direction programmable for each bit individually • Pull-up resistor provided/not provided (specified by bit) • Other functions PC0-PC7 : Parallel interface address output	Yes
PWM0	O	PWM0 output port	No
PWM1	O	PWM1 output port	No
$\overline{RES}$	I	Reset terminal	No
XT1	I	• Input terminal for 32.768kHz X'tal oscillation • Other function AN10 : AD converter input port General input port When not in use, connect terminal to VDD1.	No
XT2	I/O	• Output terminal for 32.768kHz X'tal oscillation • Other function AN11 : AD converter input port General input port When not in use, set as oscillation and leave terminal open	No
CF1	I	Input terminal for ceramic resonator	No
CF2	O	Output terminal for ceramic resonator	No

Port Output Configuration

Output configuration and pull-up resistor options are shown in the following table.
Input is possible even when a port is in output mode.

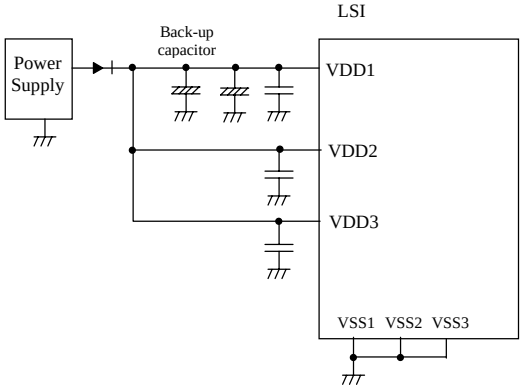
Terminal	Option applies to:	Option	Output Format	Pull-up resistor
P00 - P07	each bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	None
P10 - P17 P20 - P27	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PA2 - PA5 PB0 - PB7(*) PC0 - PC7	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	None	Nch-open drain	Programmable
P71 - P73	-	None	CMOS	Programmable
P80 - P82	-	None	Nch-open drain	None
PWM0, PWM1	-	None	CMOS	None
XT1	-	None	Input only	None
XT2	-	None	Output for 32.768kHz crystal oscillation	None

Note 1 Programmable pull-up resistor of Port 0 is specified in nibble units (P00 - P03, P04 - P07).

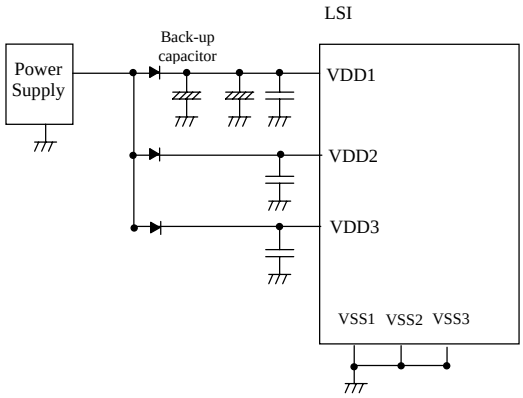
(*) When in parallel interface mode, PB0 - PB7 output format is CMOS, regardless of any selected option.

Note: To reduce VDD signal noise and to increase the duration of the backup battery supply, VSS1, VSS2, and VSS3 should connect to each other and they should also be grounded.

Example 1 : During backup in hold mode, port output ‘H’ level is supplied from the back-up capacitor.



Example 2 : During backup in hold mode, output is not held high and its value in unsettled.



1. Absolute maximum ratings / Ta=25°C, VSS1=VSS2=VSS3=0V

Parameter		Symbol	Pins	Conditions	Limits				
					VDD[V]	min.	typ.	max.	unit
Supply voltage		VDDMAX	VDD1, VDD2, VDD3	VDD1=VDD2 =VDD3		-0.3		+6.5	V
Input voltage		VI(1)	XT1, XT2, CF1			-0.3		VDD+0.3	
Output voltage		VO(1)	PWM0, PWM1			-0.3		VDD+0.3	
Input/Output voltage		VIO(1)	• Ports 0, 1, 2 • Ports 7, 8 • Ports A, B, C • PWM0, PWM1			-0.3		VDD+0.3	
High level output current	Peak output current	IOPH(1)	• Ports 0, 1, 2 • Ports A, B, C • PWM0, PWM1	• CMOS output • For each pin.		-10			mA
		IOPH(2)	P71-P73	For each pin.		-5			
	Total output current	ΣIOAH(1)	P71-P73	Total of all pins		-5			
		ΣIOAH(2)	• Port 1 • PWM0, PWM1	Total of all pins		-30			
		ΣIOAH(3)	Port 0	Total of all pins		-20			
		ΣIOAH(4)	Ports B,2	Total of all pins		-20			
		ΣIOAH(5)	Ports A, C	Total of all pins		-20			
Low level output current	Peak output current	IOPL(1)	• P02-P07 • Ports 1, 2 • Ports A, B, C • PWM0, PWM1	For each pin.				20	
		IOPL(2)	P00, P01	For each pin.				30	
		IOPL(3)	Ports 7, 8	For each pin.				5	
	Total output current	ΣIOAL(1)	Port 7	Total of all pins				15	
		ΣIOAL(2)	Port 8	Total of all pins				15	
		ΣIOAL(3)	• Port 1 • PWM0, PWM1	Total of all pins				50	
		ΣIOAL(4)	Port 0	Total of all pins				70	
		ΣIOAL(5)	Ports B,2	Total of all pins				40	
		ΣIOAL(6)	Ports A, C	Total of all pins				40	
Maximum power consumption		Pdmax	QIP64E	Ta= -20 to +70°C				429	mW
			SQFP64					271	
Operating temperature range		Topg				-20		70	°C
Storage temperature range		Tstg				-55		125	

2. Recommended operating range / Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max.	unit
Operating supply voltage range	VDD(1)	VDD1=VDD2 =VDD3	0.294µs ≤ tCYC ≤ 200µs		4.5		5.5	V
			0.588µs ≤ tCYC ≤ 200µs Except for on-board rewriting		2.5		5.5	
HOLD voltage	VHD	VDD1=VDD2 =VDD3	RAM and register data are kept in HOLD mode.		2.0		5.5	
Input high voltage	VIH(1)	• Ports 1, 2 • P71-P73 • P70 port input /interrupt		2.5 - 5.5	0.3VDD +0.7		VDD	
	VIH(2)	• Ports 0, 8 • Ports A, B, C		2.5 - 5.5	0.3VDD +0.7		VDD	
	VIH(3)	Port 70 Watchdog timer		2.5 - 5.5	0.9VDD		VDD	
	VIH(4)	XT1, XT2, CF1, $\overline{RES}$		2.5 - 5.5	0.75VDD		VDD	
Input low voltage	VIL(1)	• Ports 1, 2 • P71-P73 • P70 port input /interrupt		2.5 - 5.5	VSS		0.1VDD +0.4	
	VIL(2)	• Ports 0, 8 • Ports A, B, C		2.5 - 5.5	VSS		0.15VDD +0.4	
	VIL(5)	Port 70 Watchdog Timer		2.5 - 5.5	VSS		0.8VDD -1.0	
	VIL(6)	XT1, XT2, CF1, $\overline{RES}$		2.5 - 5.5	VSS		0.25VDD	
Operation cycle time	tCYC			4.5 - 5.5	0.294		200	µs
			Except for on-board rewriting	2.5 - 5.5	0.588		200	
External system clock frequency	FEXCF(1)	CF1	• Leave CF2 pin open • System clock divider set to 1/1 • External clock DUTY=50±5%	4.5 - 5.5	0.1		10	MHz
			• Leave CF2 pin open • System clock divider set to 1/1 • External clock DUTY=50±5%	2.5 - 5.5	0.1		5	
			• Leave CF2 pin open • System clock divider set to 1/2	4.5 - 5.5	0.2		20.4	
			• Leave CF2 pin open • System clock divider set to 1/2	2.5 - 5.5	0.1		10	

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max	unit
Oscillation frequency Range (Note1)	FmCF(1)	CF1, CF2	10MHz ceramic resonator oscillation Refer to figure 1	4.5- 5.5		10		MHz
	FmCF(2)	CF1, CF2	5MHz ceramic resonator oscillation Refer to figure 1	2.5 - 5.5		5		
	FmRC		RC oscillation	2.5 - 5.5	0.3	1.0	2.0	
	FmMRC		Frequency variable RC oscillation source oscillation	2.5 - 5.5		50		
	FsX'tal	XT1, XT2	32.768kHz crystal resonator oscillation Refer to figure 2	2.5 - 5.5		32.768		kHz

(Note 1) The oscillation parameters are shown on Tables 1 and 2.
(Note 2) VDD∞4.5V is required for on-board flash ROM rewriting.

3. Electrical characteristics / Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Input high current	IIH(1)	• Ports 0, 1, 2 • Ports 7, 8 • Ports A, B, C • $\overline{\text{RES}}$ • PWM0, PWM1	• Output disable • Pull-up resistor OFF • VIN=VDD (including the off-leak current of the output Tr.)	2.5 - 5.5			1	µA
	IIH(2)	XT1, XT2	• Using as an input port • VIN=VDD	2.5 - 5.5			1	
	IIH(3)	CF1	VIN=VDD	2.5 - 5.5			15	
Input low current	IIL(1)	• Ports 0, 1, 2 • Ports 7, 8 • Ports A, B, C • $\overline{\text{RES}}$ • PWM0, PWM1	• Output disable • Pull-up resistor OFF • VIN=VSS (including the off-leak current of the output Tr.)	2.5 - 5.5	-1			
	IIL(2)	XT1, XT2	• Using as an input port • VIN=VSS	2.5 - 5.5	-1			
	IIL(3)	CF1	VIN=VSS	2.5 - 5.5	-15			
Output high voltage	VOH(1)	• Ports 0, 1, 2 • Ports B, C	IOH=-1.0mA	4.5 - 5.5	VDD-1			V
	VOH(2)	• PWM0, PWM1	IOH=-0.1mA	2.5 - 5.5	VDD-0.5			
	VOH(3)	Port A	IOH=-5.0mA	4.5 - 5.5	VDD-1			
	VOH(4)		IOH=-0.4mA	2.5 - 5.5	VDD-0.5			
	VOH(5)	P71-P73	IOH=-0.4mA	4.5 - 5.5	VDD-1			
Output low voltage	VOL(1)	• Ports 0, 1, 2 • Ports B, C	IOL=10mA	4.5 - 5.5			1.5	V
	VOL(2)	• PWM0, PWM1	IOL=1.6mA	4.5 - 5.5			0.4	
	VOL(3)		IOL=1mA	2.5 - 5.5			0.4	
	VOL(4)	P00, P01	IOL=30mA	4.5 - 5.5			1.5	
	VOL(5)	Ports 7, 8	IOL=1mA	2.5 - 5.5			0.4	
	VOL(6)							
	VOL(7)	Port A	IOL=15mA	4.5 - 5.5			1.5	
	VOL(8)		IOL=2mA	2.5 - 5.5			0.4	
Pull-up resistor	Rpu	• Ports 0, 1, 2 • Port 7 • Ports A, B, C	VOH=0.9VDD	2.5 - 5.5	15	40	70	kΩ
Hysteresis voltage	VHIS	• $\overline{\text{RES}}$ • Port 1 • Port 2 • Port 7		2.5 - 5.5		0.1VDD		V
Pin capacitance	CP	All pins	• All pins except the measured terminal : VIN=VSS • f=1MHz • Ta=25°C	2.5 - 5.5		10		pF

4. Serial input/output characteristics / Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	max.	unit
Serial clock	Input clock	Cycle	tSCK(1)	SCK0(P12)	Refer to figure 6	2.5 - 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
			tSCKLA(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)				3(SIO0)			
		Cycle	tSCK(2)	SCK1(P15)	Refer to figure 6	2.5 - 5.5	2			
		Low level pulse width	tSCKL(2)				1			
		High level pulse width	tSCKH(2)				1			
	Output clock	Cycle	tSCK(3)	SCK0(P12),	• CMOS output • Refer to figure 6	2.5 - 5.5	4/3			
		Low level pulse width	tSCKL(3)					1/2		tSCK
			tSCKLA(2)		SCK0(P12) SIO0			3/4		
		High level pulse width	tSCKH(3)					1/2		
			tSCKHA(2)		SCK0(P12) SIO0			2		
		Cycle	tSCK(4)	SCK1(P15)	• CMOS output • Refer to figure 6	2.5 - 5.5	2			tCYC
		Low level pulse width	tSCKL(4)					1/2		tSCK
		High level pulse width	tSCKH(4)					1/2		
Serial input	Data set-up time		tsDI	SB0(P11), SB1(P14), SI0 SI1	• Data set-up to SI0CLK • Data hold from SI0CLK • Refer to figure 6	2.5 - 5.5	0.03			µs
	Data hold time		thDI				0.03			
Serial output	Output delay time		tdD0	SO0(P10), SO1(P13), SB0(P11), SB1(P14),	• Data hold from SI0CLK • Time delay from SI0CLK trailing edge to the SO data change in the open drain • Refer to figure 6	2.5 - 5.5			1/3tCYC +0.05	

5. Parallel Input/Output Characteristics / Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Note: If Port A terminals will be used as RS, $\overline{WR}$, $\overline{RD}$ or $\overline{CS}$, then it should be set to CMOS format by option data. Refer to figures 8 and 9 for parallel output timing.

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Write cycle, Read cycle	tC(1)			2.5 - 5.5		1		tCYC
Address set-up time	tsA(1)	• $\overline{WR}$ (PA3), PB0-PB7 • $\overline{RD}$ (PA4), PC0-PC7	From address set-up until control signal changes	2.5 - 5.5	1/3tCYC -30ns			tCYC & ns
	tsA(2)	$\overline{RD}$ (PA4), PC0-PC7		2.5 - 5.5	2/3tCYC -30ns			
Address hold time	thA(1)	$\overline{RD}$ (PA4), PC0-PC7	From change of $\overline{RD}$ until address change	2.5 - 5.5	1/6tCYC			
	thA(2)	$\overline{WR}$ (PA3), PC0-PC7	From change of $\overline{WR}$ until address change	2.5 - 5.5	5			ns
RS set-up time	tsRS(1)	$\overline{WR}$ (PA3), RS(PA5), $\overline{CS}$ (PAX)	From change of RS, $\overline{CS}$ until change in $\overline{WR}$	2.5 - 5.5	1/6tCYC -15ns			tCYC & ns
	tsRS(2)	$\overline{RD}$ (PA4), RS(PA5)	from change of RS until change in $\overline{RD}$	2.5 - 5.5	1/6tCYC -15ns			
	tsRS(3)	$\overline{RD}$ (PA4), RS(PA5)		2.5 - 5.5	1/3tCYC -15ns			
$\overline{CS}$ set-up time	tsCS(1)	$\overline{RD}$ (PA4), $\overline{CS}$ (PAX)	From change in $\overline{CS}$ until change in $\overline{RD}$	2.5 - 5.5	1/3tCYC -15ns			
	tsCS(2)	$\overline{WR}$ (PA3), $\overline{CS}$ (PAX)	From change in $\overline{CS}$ until change in $\overline{WR}$	2.5 - 5.5	2/3tCYC -15ns			
RS hold time	thRS(1)	$\overline{WR}$ (PA3), RS(PA5)	From change in $\overline{WR}$ until change in RS	2.5 - 5.5	0			ns
	thRS(2)	$\overline{RD}$ (PA4), RS(PA5), $\overline{CS}$ (PAX)	From change in $\overline{RD}$ until change in RS, $\overline{CS}$	2.5 - 5.5	1/6tCYC			tCYC & ns
	thRS(3)	$\overline{RD}$ (PA4), RS(PA5), $\overline{CS}$ (PAX)		2.5 - 5.5	0			ns
$\overline{CS}$ hold time	thCS(1)	$\overline{RD}$ (PA4), RS(PA5)	From change in $\overline{RD}$ until change in $\overline{CS}$	2.5 - 5.5	1/6tCYC			tCYC & ns
	thCS(2)	$\overline{WR}$ (PA3), RS(PA5)	From change in $\overline{WR}$ until change in $\overline{CS}$	2.5 - 5.5	0			ns
$\overline{WR}$ 'H' pulse width	tWRH(1)	$\overline{WR}$ (PA3)		2.5 - 5.5	1/6tCYC -5ns	1/6 tCYC		tCYC & ns
	tWRH(2)	$\overline{WR}$ (PA3)		2.5 - 5.5	2/3tCYC -5ns	2/3 tCYC		
$\overline{WR}$ 'L' pulse width	tWRL(1)	$\overline{WR}$ (PA3)		2.5 - 5.5	1/6tCYC -5ns	1/6 tCYC		
	tWRL(2)	$\overline{WR}$ (PA3)		2.5 - 5.5	1/3tCYC -5ns	1/3 tCYC		

(Continued)

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
$\overline{RD}$ 'H' pulse width	tRDH(1)	$\overline{RD}$ (PA4)		2.5 - 5.5	1/6tCYC -5ns	1/6 tCYC		tCYC & ns
	tRDH(2)	$\overline{RD}$ (PA4)		2.5 - 5.5	1/3tCYC -5ns	1/3 tCYC		
$\overline{RD}$ 'L' pulse width	tRDL(1)	$\overline{RD}$ (PA4)		2.5 - 5.5	1/3tCYC -5ns	1/3 tCYC		
	tRDL(2)	$\overline{RD}$ (PA4)		2.5 - 5.5	1/2tCYC -5ns	1/2 tCYC		
Data write maximum delay	tdDT(1)	$\overline{RD}$ (PA4), PB0-PB7	The time delay allowed, from $\overline{RD}$ leading edge until input data set-up (Note 1)	2.5 - 5.5			1/6tCYC -15ns	
	tdDT(2)	$\overline{RD}$ (PA4), PB0-PB7		2.5 - 5.5			1/3tCYC -15ns	
Input data set-up time	tsDTR(1)	$\overline{RD}$ (PA4), PB0-PB7	From input data set-up to $\overline{RD}$ leading edge. (Note 2)	2.5 - 5.5	40			ns
Input data hold time	thDTR(1)	$\overline{RD}$ (PA4), PB0-PB7	From $\overline{RD}$ leading edge until input data hold	2.5 - 5.5	0			ns
Output data set-up time	tsDTW(1)	$\overline{RD}$ (PA4), PB0-PB7	From output data set-up until $\overline{WR}$ leading edge	2.5 - 5.5	1/3tCYC -30ns			tCYC & ns
	tsDTW(2)	$\overline{RD}$ (PA4), PB0-PB7		2.5 - 5.5	1/3tCYC -30ns			
Output data hold time	thDTW(1)	$\overline{RD}$ (PA4), PB0-PB7	From $\overline{WR}$ leading edge until output data hold	2.5 - 5.5	0			ns
	thDTW(2)			2.5 - 5.5	0			

Note 1 : Time until incorrect data of Low disappears.
Note 2 : Incorrect data of Low is not output in the period between tRDL(1) - tdDT(1).

6. Pulse input conditions / Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72) INT4(P20-P23) INT5(P24-P27)	• Interrupt acceptable • Timer 0 and 1 event input acceptable	2.5 - 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) (The noise rejection clock is selected to 1/1.)	• Interrupt acceptable • Timer 0 event input acceptable	2.5 - 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) (The noise rejection clock is selected to 1/32.)	• Interrupt acceptable • Timer 0 event input acceptable	2.5 - 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) (The noise rejection clock is selected to 1/128.)	• Interrupt acceptable • Timer 0 event input acceptable	2.5 - 5.5	256			
	tPIL(5)	$\overline{RES}$	Reset acceptable	2.5 - 5.5	200			µs

7. AD converter characteristics / Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Resolution	N	AN0(P80) - AN2(P82) AN3(P03) - AN7(P07) AN8(P70) AN9(P71) AN10(XT1) AN11(XT2)		3.0 - 5.5		8		bit
Absolute precision	ET		(Note 2)	3.0 - 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time=32 × tCYC (ADCR2=0) (Note 3)	4.5 - 5.5	15.10 (tCYC= 0.588µs)		97.92 (tCYC= 3.06µs)	µs
				3.0 - 5.5	31.36 (tCYC= 0.980µs)		97.92 (tCYC= 3.06µs)	
			AD conversion time=64 × tCYC (ADCR2=1) (Note 3)	4.5 - 5.5	18.82 (tCYC= 0.294µs)		97.92 (tCYC= 1.53µs)	
				3.0 - 5.5	62.72 (tCYC= 0.980µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			3.0 - 5.5	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	3.0 - 5.5			1	µA
	IAINL		VAIN=VSS	3.0 - 5.5	-1			

(Note 2) Absolute precision excludes the quantizing error (±1/2 LSB).

(Note 3) The conversion time is the time from executing the AD conversion instruction to setting the complete digital conversion value in the register.

8. Current dissipation characteristics / Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max.	unit
Current drain during basic operation (Note 4)	IDDOP(1)	VDD1 =VDD2 =VDD3	• FmCF=10MHz by ceramic resonator • FmX'tal=32.768kHz by crystal oscillation • System clock : CF oscillation (10MHz) • Internal RC oscillation stops • frequency variable RC oscillation stops • 1/1 divided	4.5 - 5.5		18	35	mA
	IDDOP(2)		• CF1=20MHz by external clock • FmX'tal=32.768kHz by crystal oscillation • System clock : CF1 oscillation (20MHz) • Internal RC oscillation stops • frequency variable RC oscillation stops • 1/2 divided	2.5 - 5.5		19	36	
	IDDOP(3)		• FmCF=5MHz by ceramic resonator • FmX'tal=32.768kHz by crystal oscillation • System clock : CF oscillation (5MHz) • Internal RC oscillation stops • frequency variable RC oscillation stops • 1/1divided	4.5 - 5.5		10	22	
	IDDOP(4)			2.5 - 4.5		5	15	
	IDDOP(5)		• FmCF=0Hz (when oscillation stops) • FmX'tal=32.768kHz by crystal oscillation • System clock : RC oscillation • frequency variable RC oscillation stops • 1/2 divided	4.5 - 5.5		2	8	
	IDDOP(6)			2.5 - 4.5		1	5	
	IDDOP(7)		• FmCF=0Hz (when oscillation stops) • FmX'al=32.768kHz by crystal oscillation • System clock :1MHz with frequency variable RC oscilatin • Internal RC oscillation stops • 1/2 divided	4.5 – 5.5		2.5	13	
	IDDOP(8)			2.5 - 4.5		1.8	9	
	IDDOP(9)		• FmCF=0Hz (when oscillation stops) • FmX'al=32.768kHz by crystal oscillation • System clock : X'tal oscillation (32.768kHz) • Internal RC oscillation stops • frequency variable RC oscillation stops • 1/2 divided	4.5 – 5.5		50	150	µA
	IDDOP(10)			2.5 - 4.5		30	120	

(Continued)

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Current drain in HALT mode (Note 4)	IDDHALT(1)	VDD1 =VDD2 =VDD3	• HALT mode • FmCF=10MHz by ceramic resonator • FmX'tal=32.768kHz by crystal oscillation • System clock : CF oscillation (10MHz) • Internal RC oscillation stops • frequency variable RC oscillation stops • 1/1 divided	4.5 - 5.5		4	10	mA
	IDDHALT(2)		• HALT mode • CF1=20MHz by external clock • FmX'tal=32.768kHz by crystal oscillation • System clock : CF1 oscillation (20MHz) • Internal RC oscillation stops • frequency variable RC oscillation stops • 1/2 divided	4.5 - 5.5		4.5	14	
	IDDHALT(3)		• HALT mode • FmCF=5MHz by ceramic resonator • FmX'tal=32.768kHz by crystal oscillation • System clock : CF oscillation (5MHz) • Internal RC oscillation stops • frequency variable RC oscillation stops • 1/1divided	4.5 - 5.5		2	5	
	IDDHALT(4)			2.5 - 4.5		1	3.2	
	IDDHALT(5)		• HALT mode • FmCF=0Hz (when oscillation stops) • FmX'tal=32.768kHz by crystal oscillation • System clock : RC oscillation • frequency variable RC oscillation stops • 1/2 divided	4.5 - 5.5		0.5	1.5	
	IDDHALT(6)			2.5 - 4.5		0.3	1	
	IDDHALT(7)		• HALT mode • FmCF=0Hz (when oscillation stops) • FmX'tal=32.768kHz by crystal oscillation • System clock : 1MHz with frequency variable RC oscilatin • Internal RC oscillation stops • 1/2 divided	4.5 - 5.5		1.5	3.6	
	IDDHALT(8)			2.5 - 4.5		1.3	3.3	
	IDDHALT(9)		• HALT mode • FmCF=0Hz (when oscillation stops) • FmX'tal=32.768kHz by crystal oscillation • System clock : X'tal oscillation (32.768kHz) • Internal RC oscillation stops • frequency variable RC oscillation stops • 1/2 divided	4.5 - 5.5		20	80	µA
	IDDHALT(10)			2.5 - 4.5		10	50	

(Continued)

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Current drain during HOLD mode	IDDHOLD(1)	VDD1	• HOLD mode • CF1=VDD or leave it open (when using external clock)	4.5 - 5.5		0.05	20	µA
	IDDHOLD(2)			2.5 – 4.5		0.01	15	
Current drain during time-base clock HOLD mode	IDDHOLD(3)	VDD1	• Time-base clock HOLD mode • CF1=VDD or leave it open (when using external clock) • FmX'tal=32.768kHz by crystal oscillation	4.5 - 5.5		15	70	µA
	IDDHOLD(4)			2.5 – 4.5		5	40	

(Note 4) The current of the output transistors and pull-up MOS transistors are excluded.

9. F-ROM Write Characteristics / Ta=+10°C to +55°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
On-board writing current	IDDFW(1)	VDD1	• 128-byte writing • including erase time current	4.5 - 5.5		30	65	mA
Writing time	tFW(1)		• 128-byte writing • including data erase time • Excluding time to fetch 128 byte data	4.5 - 5.5		5.0	10.0	mS

Main System Clock Oscillation Circuit Characteristics

The characteristics in the table bellow is based on the following conditions:

1. Using the standard oscillation evaluation board SANYO has provided.
2. Using the external peripheral parts with the indicated value.
3. The recommended circuit parameters for the peripheral parts are verified by the oscillator manufacturer.

Table 1. Recommended circuit parameters for the main system clock using the ceramic resonator

Frequency	Manufacturer	Oscillator	Recommended circuit parameters			Operating supply voltage range	Oscillation stabilizing time		Note
			C1	C2	Rd1		typ	max	
10MHz	MURATA	CSLS10M0G53-B0	(15pF)	(15pF)	0Ω	4.5 – 5.5V	0.03ms	0.30ms	Internal C1,C2
		CSTCE10M0G52-R0	(10pF)	(10pF)	0Ω	4.5 – 5.5V	0.03ms	0.30ms	Internal C1,C2
5MHz	MURATA	CSTLS5M00G53-B0	(15pF)	(15pF)	0Ω	2.5 – 5.5V	0.03ms	0.30ms	Internal C1,C2
		CSTCR5M00G53-R0	(15pF)	(15pF)	0Ω	2.5 – 5.5V	0.03ms	0.30ms	Internal C1,C2

*The oscillation stabilizing time is a period until the oscillation becomes stable after VDD becomes higher than minimum operating voltage. (Refer to Figure4)

Subsystem Clock Oscillation Circuit Characteristics

The characteristics in the table bellow is based on the following conditions:

1. Using the standard oscillation evaluation board SANYO has provided.
2. Using the external peripheral parts with the indicated value.
3. The recommended circuit parameters for the peripheral parts are verified by the oscillator manufacturer.

Table 2. Recommended circuit parameters for the subsystem clock using the crystal oscillation

Frequency	Manufacturer	Oscillator	Recommended circuit Parameters				Operating supply voltage range	Oscillation stabilizing time		Note
			C3	C4	Rf	Rd2		typ	max	
32.768kHz	SEIKO EPSON	MC-306	9pF	9pF	OPEN	820kΩ	2.5 – 5.5V	1.5s	3s	

*The oscillation stabilizing time is the period until the oscillation becomes stable, after executing the instruction which starts the sub-clock oscillator or after releasing a HOLD mode. (Refer to Figure4)

(Notes) Since the oscillation frequency precision is affected by the circuit pattern, place the oscillation related parts as close to the oscillation pins as possible, using the shortest possible pattern length.

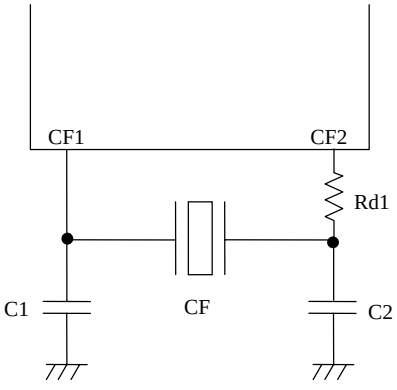


Figure 1 Ceramic oscillation circuit

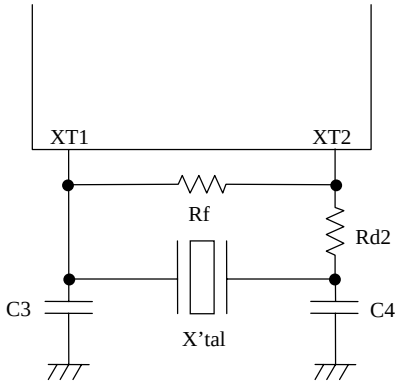


Figure 2 Crystal oscillation circuit

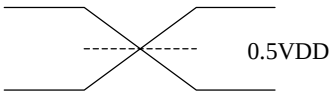


Figure 3 AC timing point

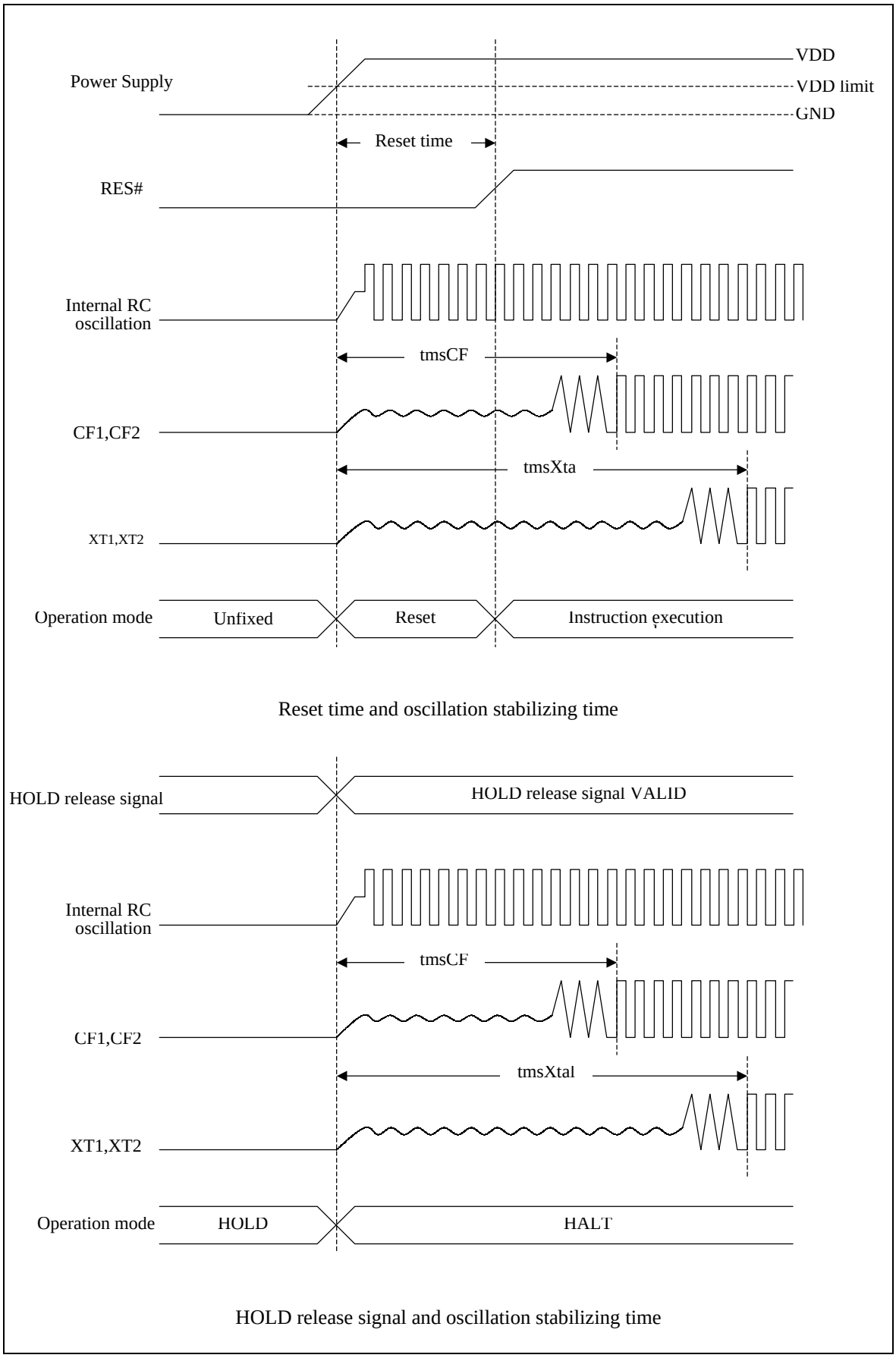
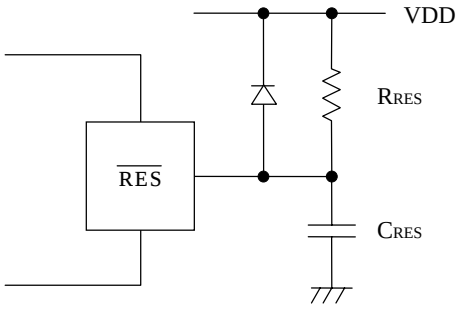


Figure 4 Oscillation stabilizing time



(Note) Select CRES and RRES value to assure that at least 200µs reset time is generated after the VDD becomes higher than the minimum operating voltage.

Figure 5 Reset circuit

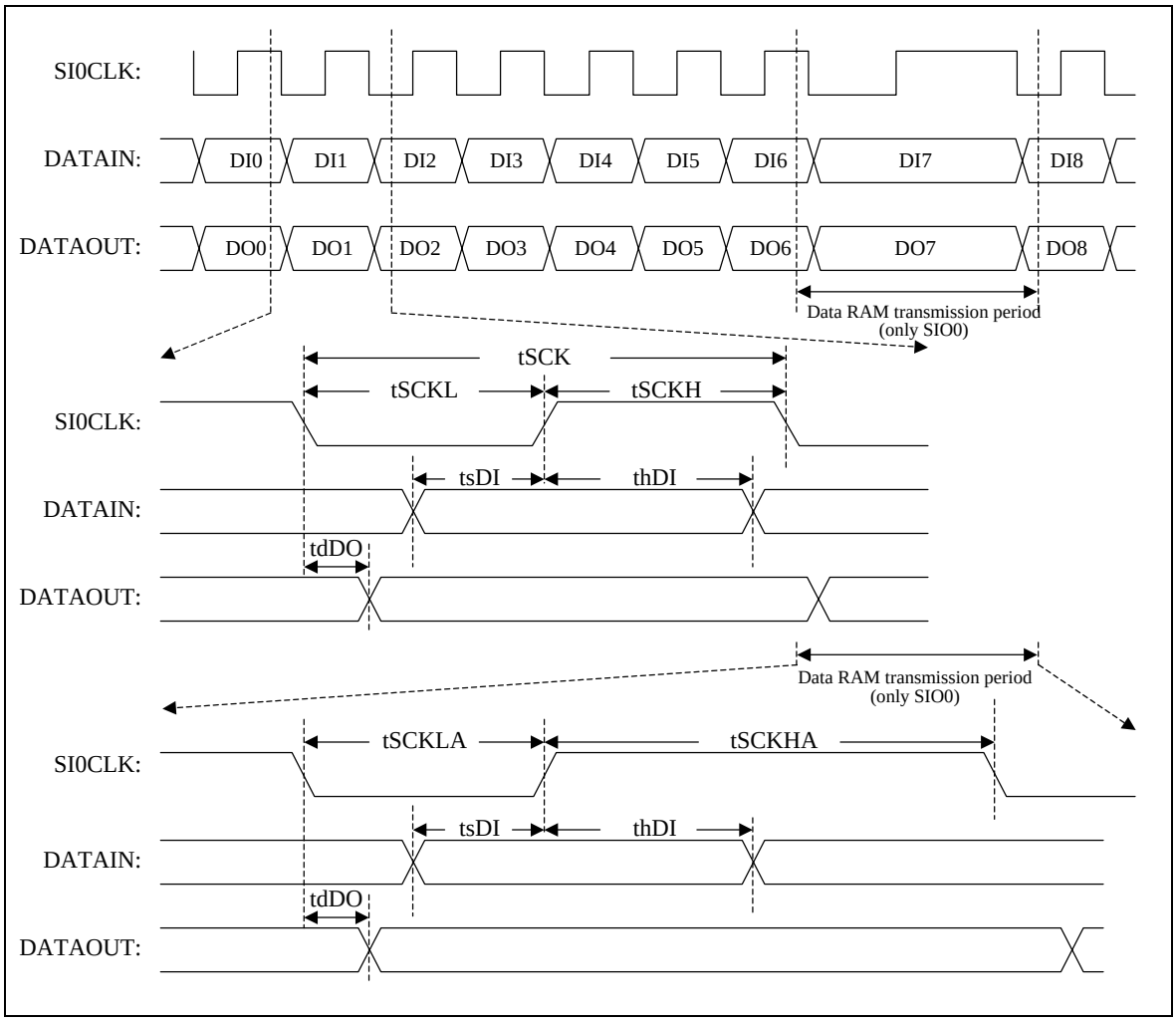


Figure 6 Serial input/output test condition

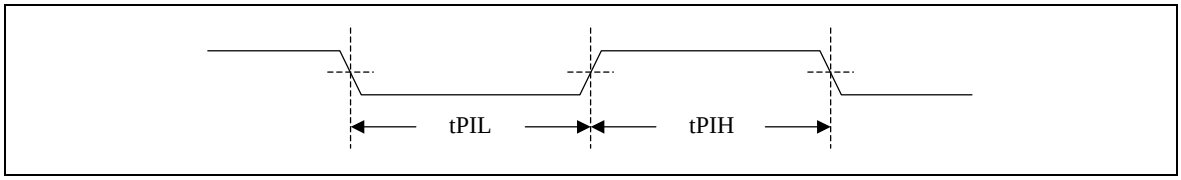
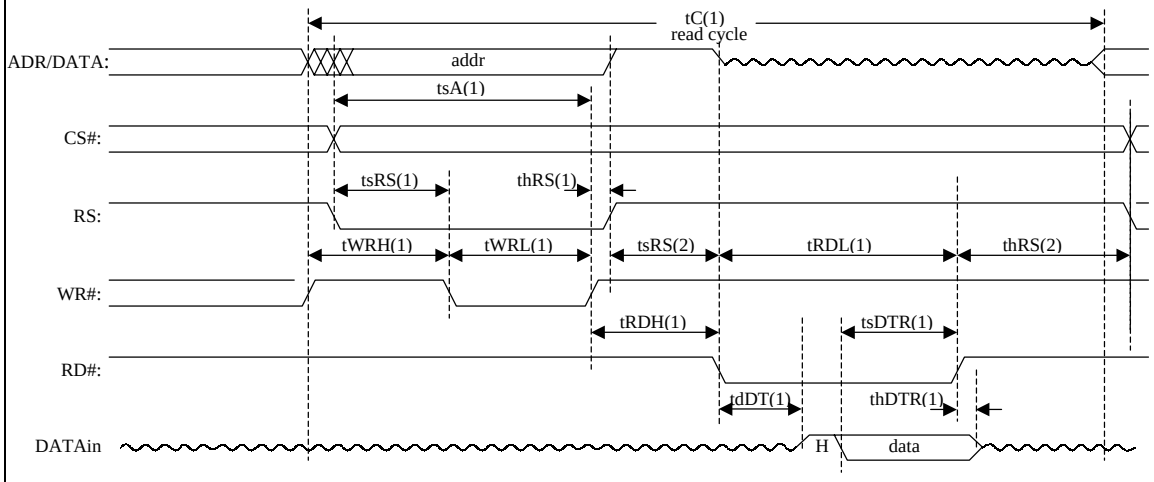


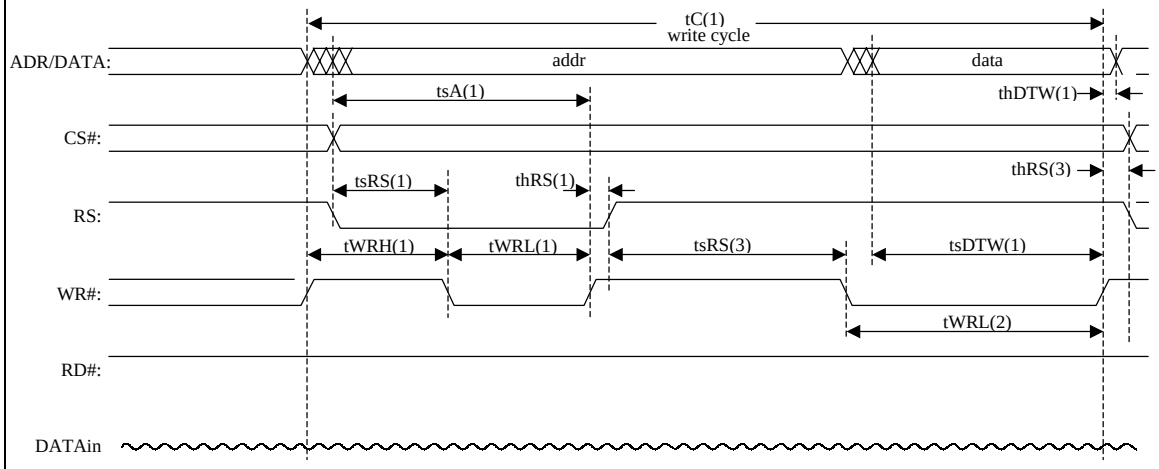
Figure 7 Pulse input timing condition

・Parallel input/output timing waveform：Indirect Setting, Read Mode



Note: If port A terminals will be used as RS, $\overline{WR}$, $\overline{RD}$ or $\overline{CS}$, then it should be set to CMOS format by option data.

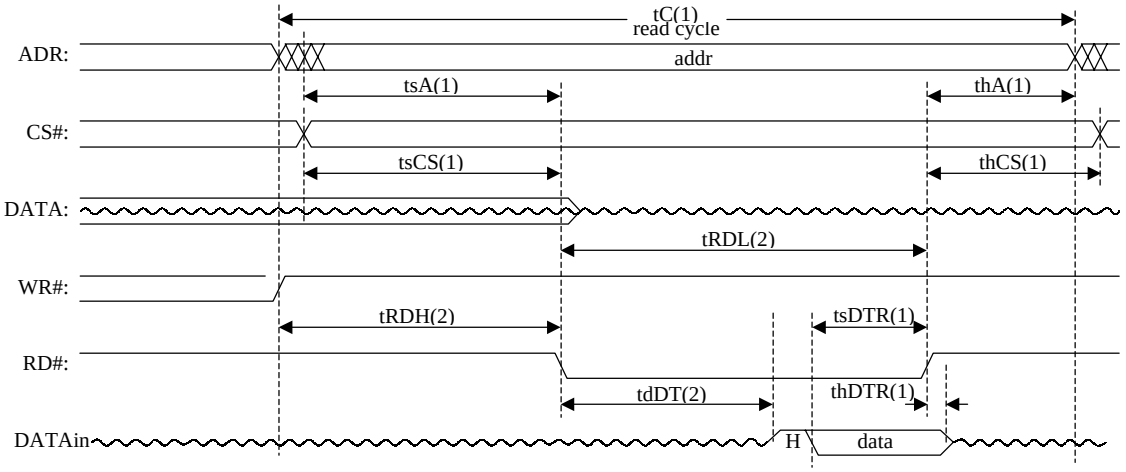
・Parallel input/output timing waveform：Indirect Setting, Write Mode



Note: If Port A terminals will be used as RS, $\overline{WR}$, $\overline{RD}$ or $\overline{CS}$, then it should be set to CMOS format by option data.

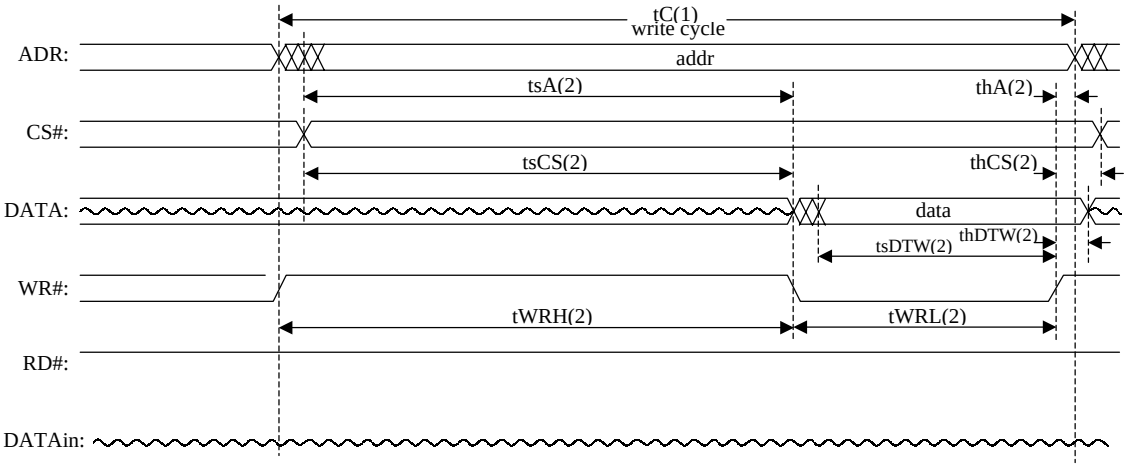
Figure 8　Indirect mode: Parallel Timing Diagram

・Parallel input/output timing waveform：Direct Setting, Read Mode



Note: If Port A terminals will be used as RS, $\overline{WR}$, $\overline{RD}$ or $\overline{CS}$, then it should be set to CMOS format by option data.

・Parallel input/output timing waveform：Direct Setting, Write Mode



Note: If Port A terminals will be used as RS, $\overline{WR}$, $\overline{RD}$ or $\overline{CS}$, then it should be set to CMOS format by option data.

Figure 9 Direct Mode: Parallel input/output Timing Diagrams