STD5N95K5, STF5N95K5, STP5N95K5, STU5N95K5

N-channel 950 V, 2 Ω typ., 3.5 A MDmesh™ K5 Power MOSFETs in DPAK, TO-220FP, TO-220 and IPAK

Datasheet - production data

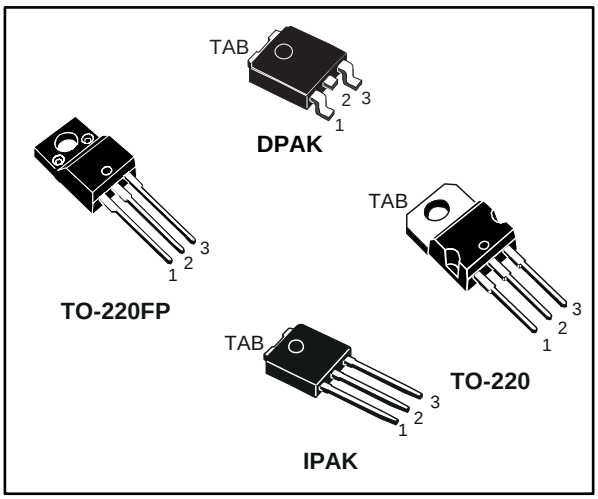
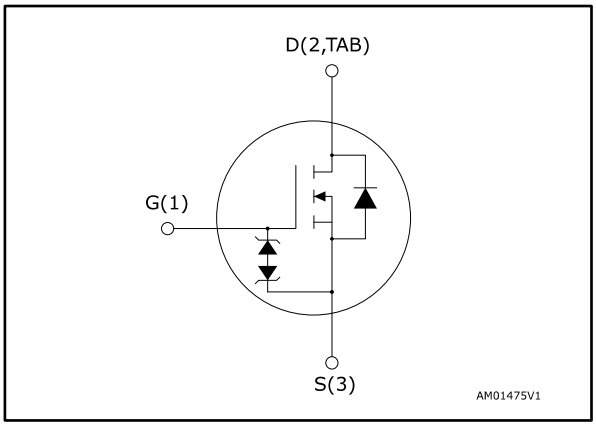


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{tot}
STD5N95K5	950 V	2.5 Ω	3.5 A	70 W
STF5N95K5				25 W
STP5N95K5				70 W
STU5N95K5				70 W

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STD5N95K5	5N95K5	DPAK	Tape and reel
STF5N95K5		TO-220FP	Tube
STP5N95K5		TO-220	
STU5N95K5		IPAK	

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK, TO-220, IPAK	TO-220FP	
V_{GS}	Gate-source voltage	±30		V
I_D	Drain current (continuous) at T_C = 25 °C	3.5	3.5 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	2.2	2.2 (1)	A
I_{DM}(2)	Drain current pulsed	14		A
P_{TOT}	Total dissipation at T_C = 25 °C	70	25	W
dv/dt (3)	Peak diode recovery voltage slope	4.5		V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T_C=25 °C)		2500	V
T_j	Operating junction temperature range	-55 to 150		°C
T_{stg}	Storage temperature range			

Notes:

(1)Limited by maximum junction temperature.

(2)Pulse width limited by safe operating area.

(3)I_{SD} ≤ 3.5 A, di/dt ≤ 100 A/µs, V_{DS} (peak) ≤ $V_{(BR)DSS}$

(4)V_{DS} ≤ 640 V

Table 3: Thermal data

Symbol	Parameter	Value				Unit
		DPAK	TO-220FP	TO-220	IPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.47	5	1.47		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient		62.5		100	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	50				°C/W

Notes:

(1)When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	1	A
E_{AS}	Single pulse avalanche energy (starting Tj = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	70	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	950			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 950 V, V_{GS} = 0 V			1	µA
		V_{DS} = 950 V, V_{GS} = 0 V T_C = 125 °C(1)			50	µA
I_{GSS}	Gate body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1.5 A		2	2.5	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	220	-	pF
C_{oss}	Output capacitance		-	17	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0 V, V_{DS} = 0 to 760 V	-	30	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	11	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz open drain	-	17	-	Ω
Q_g	Total gate charge	V_{DD} = 760 V, I_D = 3.5 A V_{GS}= 10 V (see *Figure 19: "Test circuit for gate charge behavior"*)	-	12.5	-	nC
Q_{gs}	Gate-source charge		-	2	-	nC
Q_{gd}	Gate-drain charge		-	10	-	nC

Notes:

(1)$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

(2)$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 475 V, I_D = 1.75 A, R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 18: "Test circuit for resistive load switching times"* and *Figure 23: "Switching time waveform"*)	-	12	-	ns
t_r	Rise time		-	16	-	ns
$t_{d(off)}$	Turn-off delay time		-	32	-	ns
t_f	Fall time		-	25	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3.5	A
I_{SDM}	Source-drain current (pulsed)		-		14	A
V_{SD}(1)	Forward on voltage	I_{SD} = 3.5 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 3.5 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 20: "Test circuit for inductive load switching and diode recovery times"*)	-	330		ns
Q_{rr}	Reverse recovery charge		-	2.2		µC
I_{RRM}	Reverse recovery current		-	13		A
t_{rr}	Reverse recovery time	I_{SD} = 3.5 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 20: "Test circuit for inductive load switching and diode recovery times"*)	-	525		ns
Q_{rr}	Reverse recovery charge		-	3.2		µC
I_{RRM}	Reverse recovery current		-	12		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}= ± 1 mA, I_D= 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection,thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area for DPAK and IPAK

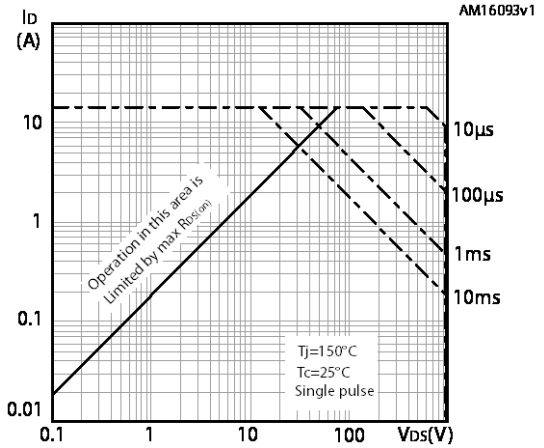


Figure 3: Thermal impedance for DPAK and IPAK

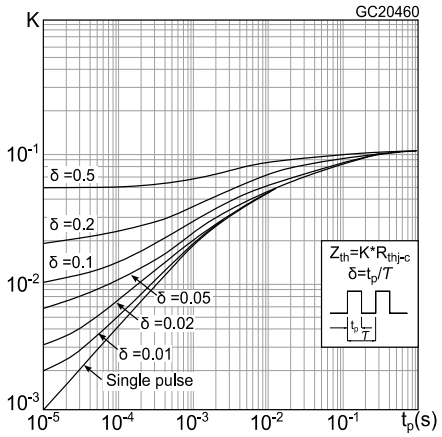


Figure 4: Safe operating area for TO-220FP

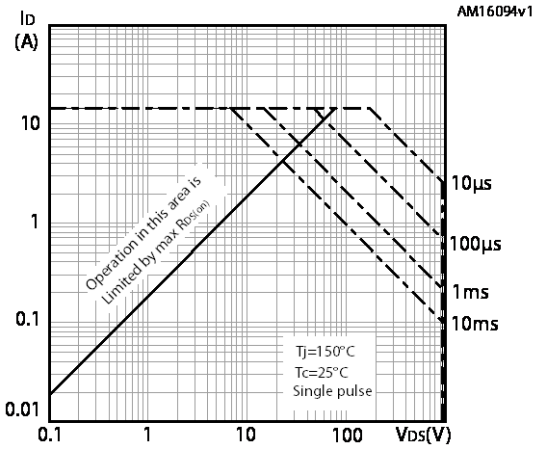


Figure 5: Thermal impedance for TO-220FP

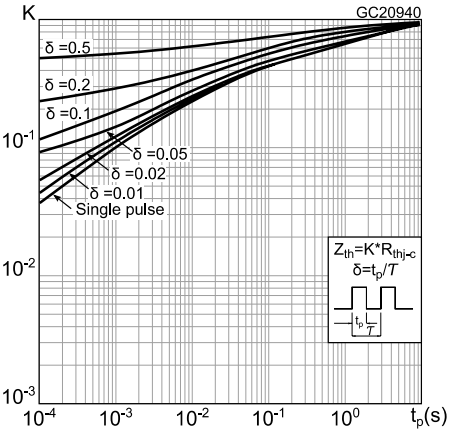


Figure 6: Safe operating area for TO-220

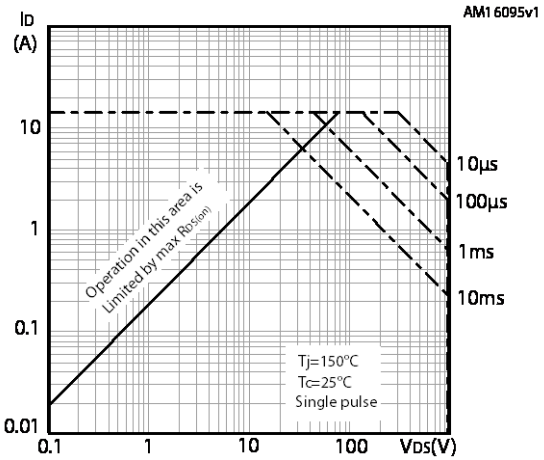


Figure 7: Thermal impedance for TO-220

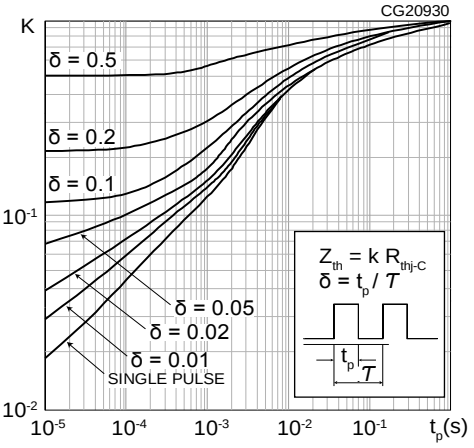


Figure 8: Output characteristics

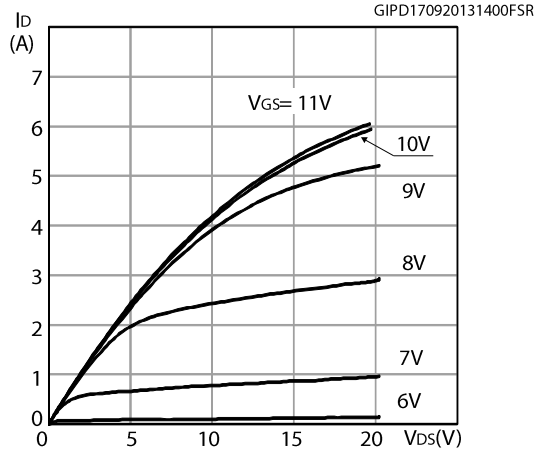


Figure 9: Transfer characteristics

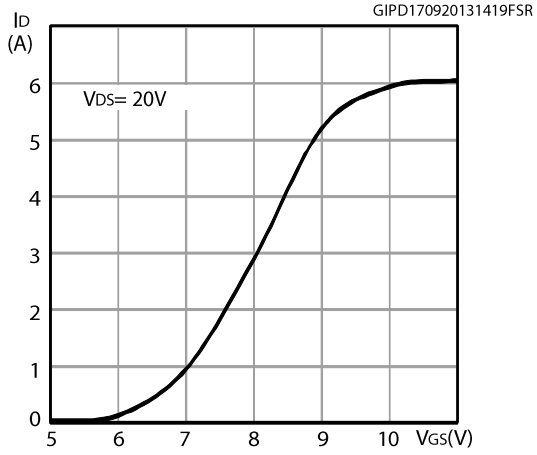


Figure 10: Gate charge vs gate-source voltage

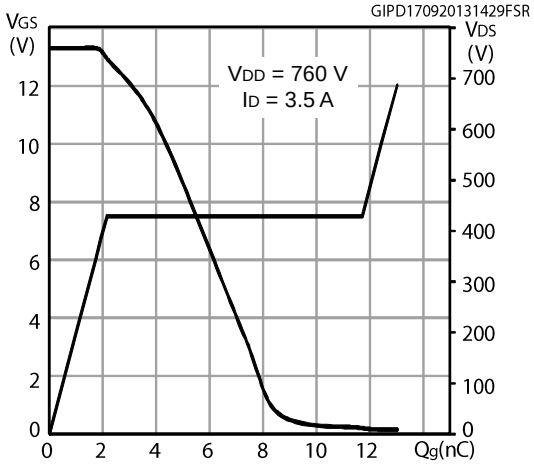


Figure 11: Static drain-source on-resistance

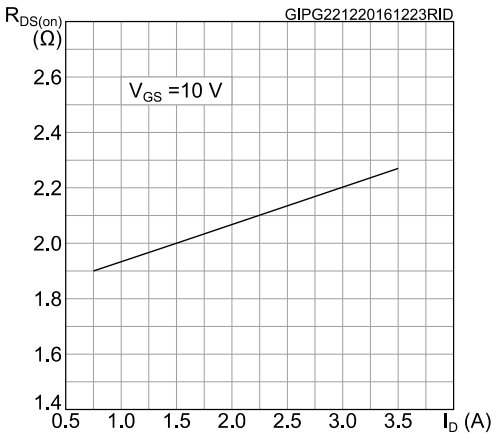


Figure 12: Capacitance variations

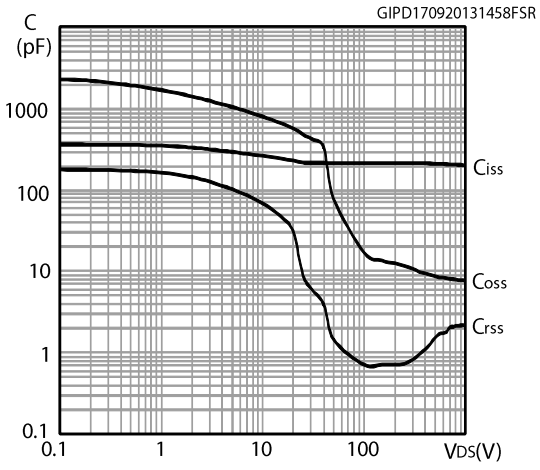


Figure 13: Output capacitance stored energy

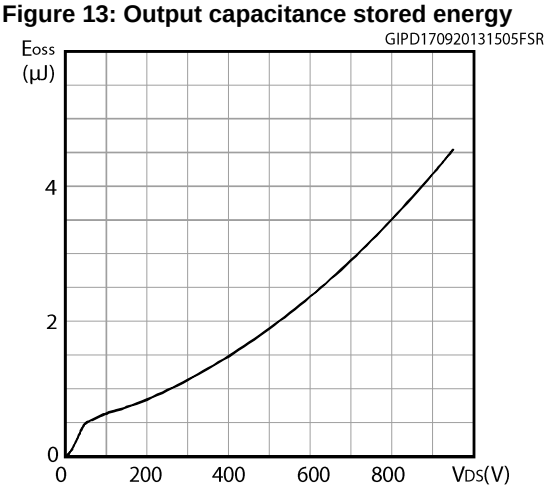


Figure 14: Normalized gate threshold voltage vs temperature

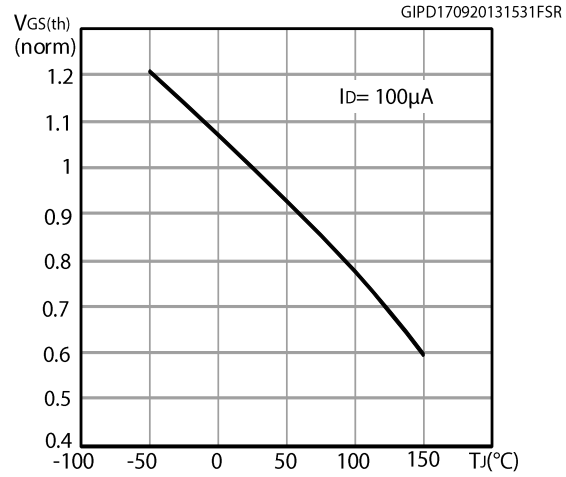


Figure 15: Normalized $V_{(BR)DSS}$ vs temperature

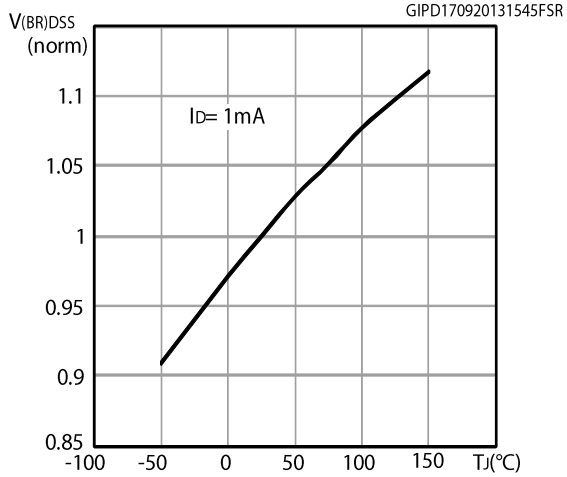


Figure 16: Normalized on-resistance vs temperature

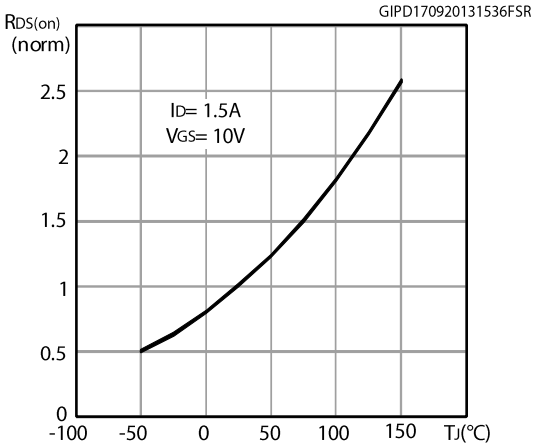
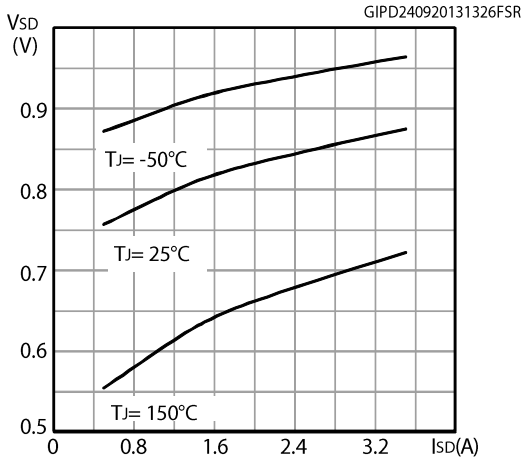


Figure 17: Source-drain diode forward characteristics



3 Test circuits

Figure 18: Test circuit for resistive load switching times

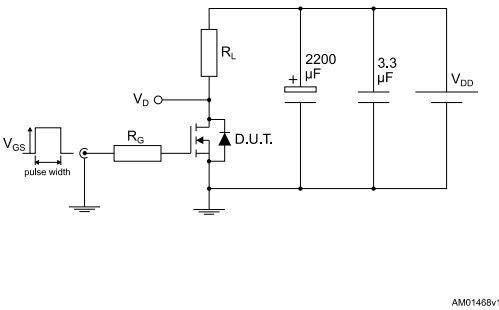


Figure 19: Test circuit for gate charge behavior

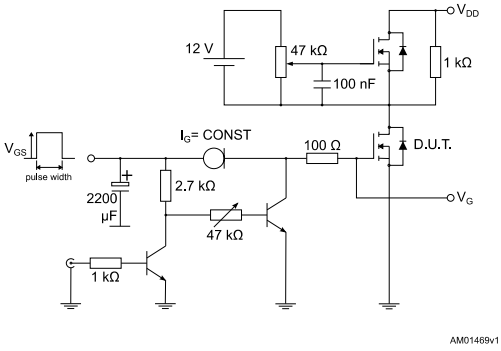


Figure 20: Test circuit for inductive load switching and diode recovery times

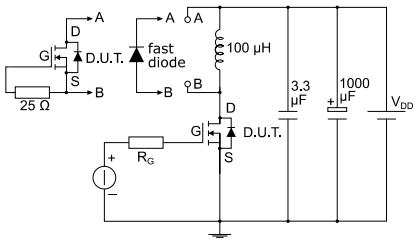


Figure 21: Unclamped inductive load test circuit

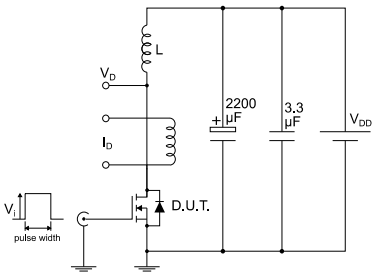


Figure 22: Unclamped inductive waveform

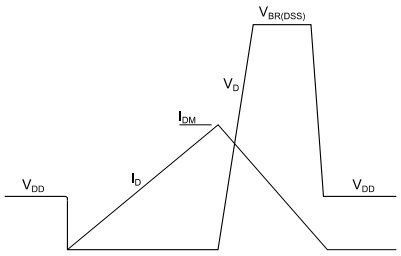
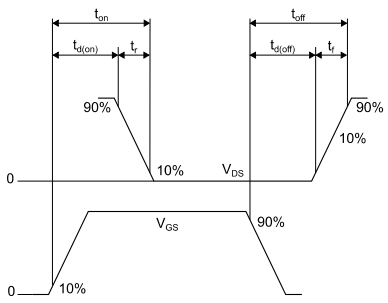


Figure 23: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 24: DPAK (TO-252) type A2 package outline

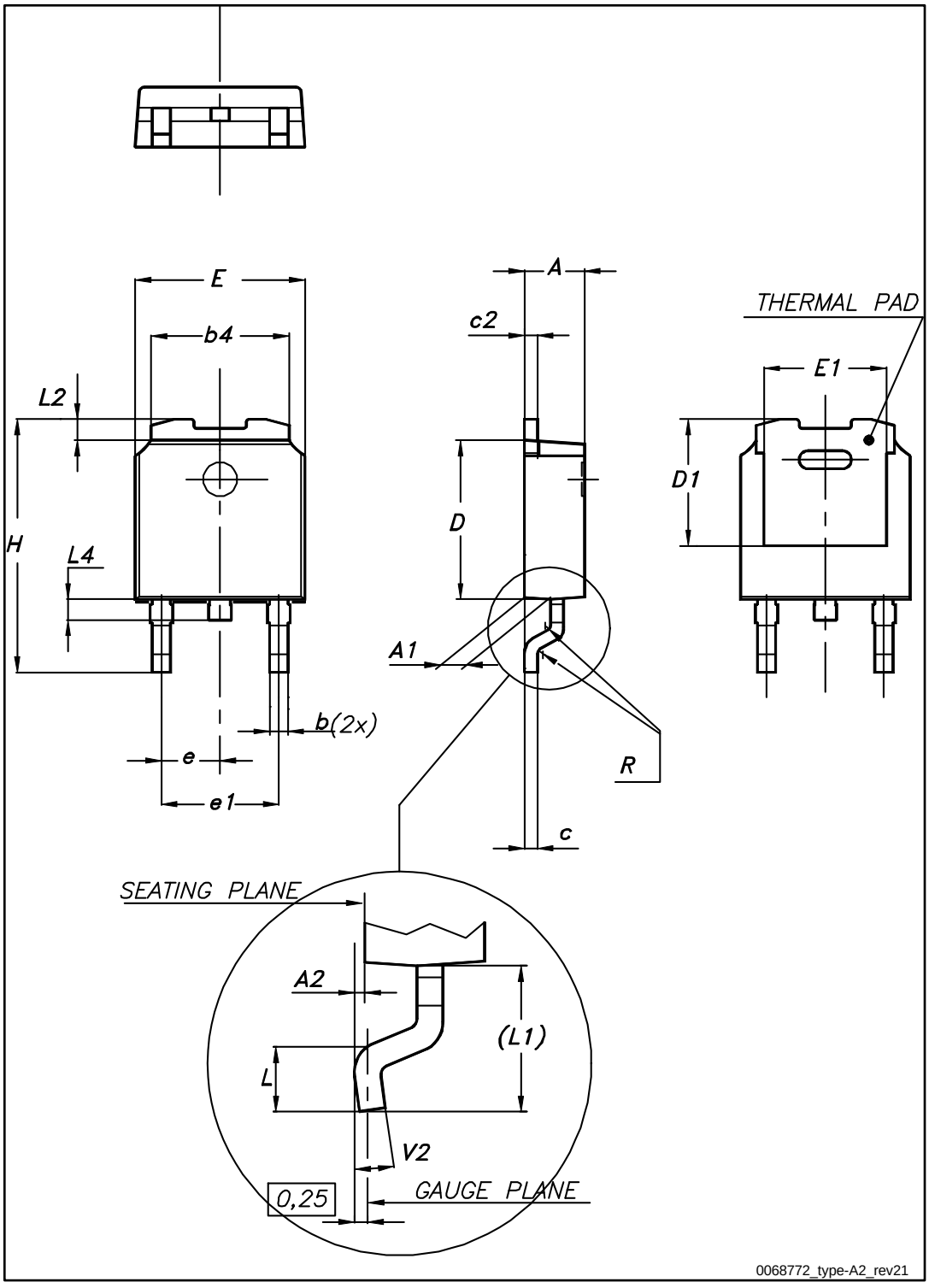
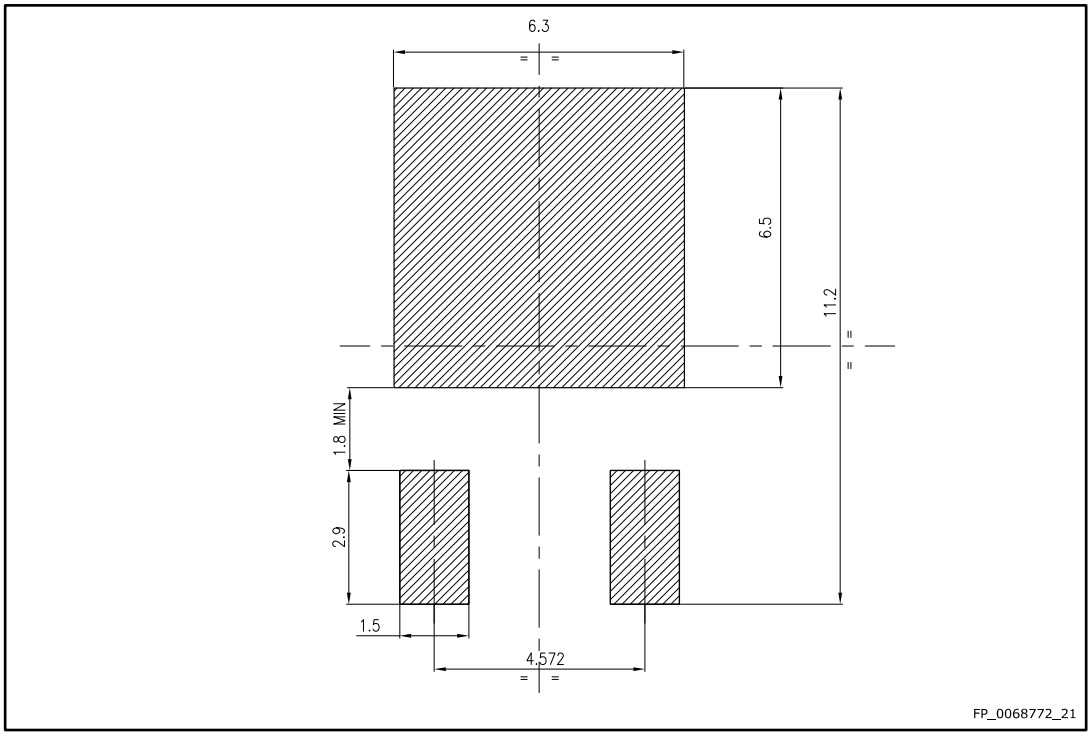


Table 10: DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 25: DPAK (TO-252) type A2 recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) type C2 package information

Figure 26: DPAK (TO-252) type C2 package outline

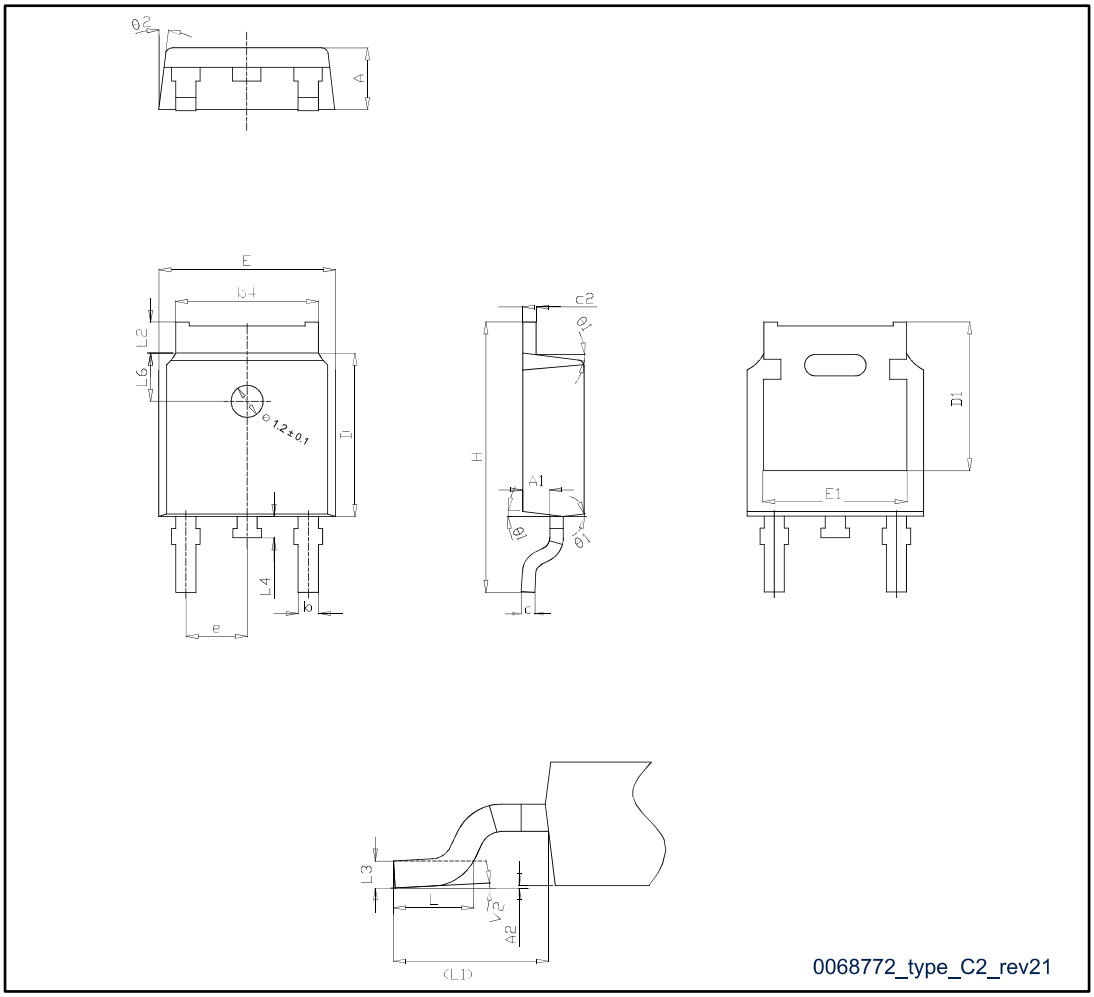
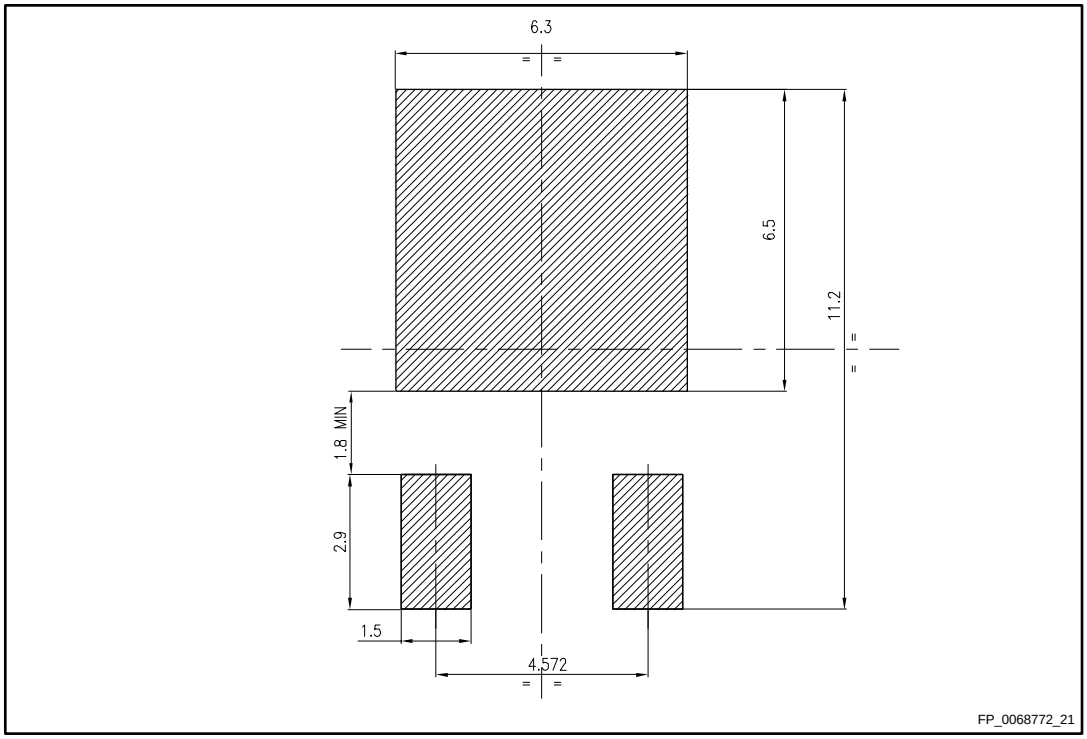


Table 11: DPAK (TO-252) type C2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 27: DPAK (TO-252) type C2 recommended footprint (dimensions are in mm)



4.3 DPAK (TO-252) packing information

Figure 28: DPAK (TO-252) tape outline

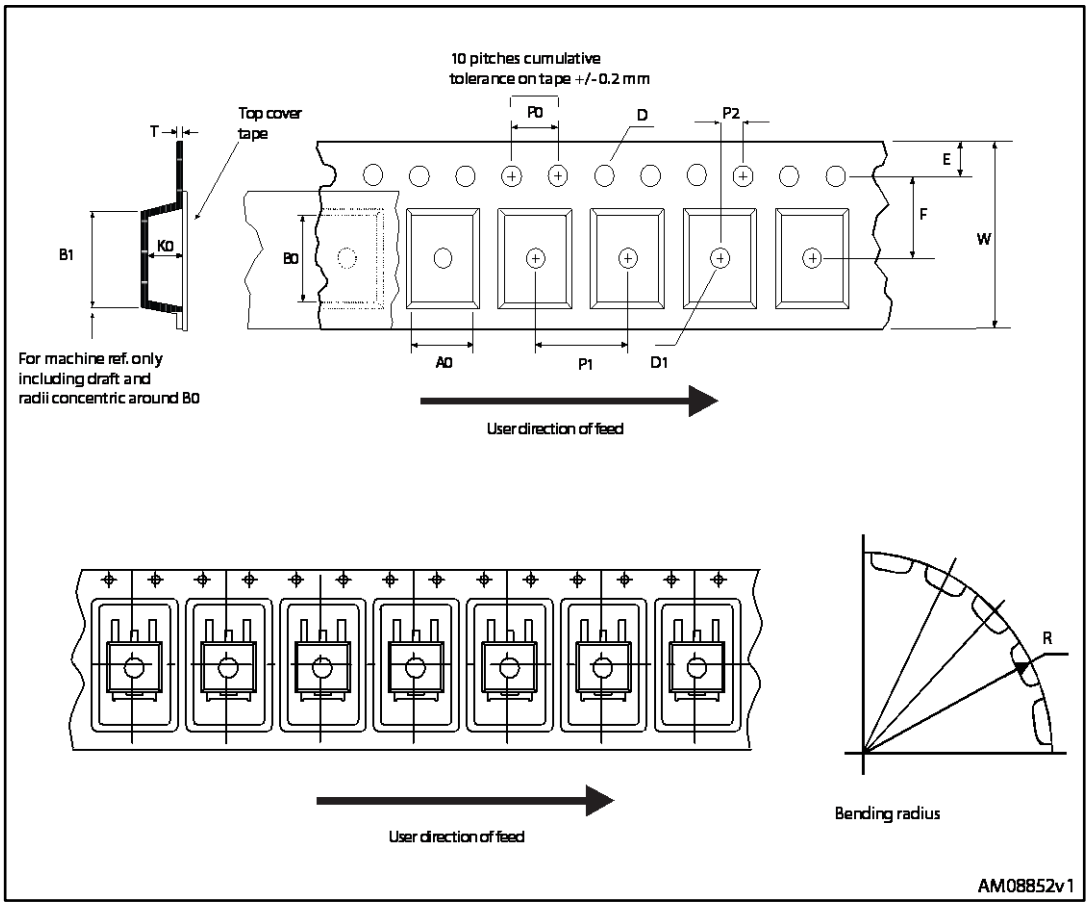


Figure 29: DPAK (TO-252) reel outline

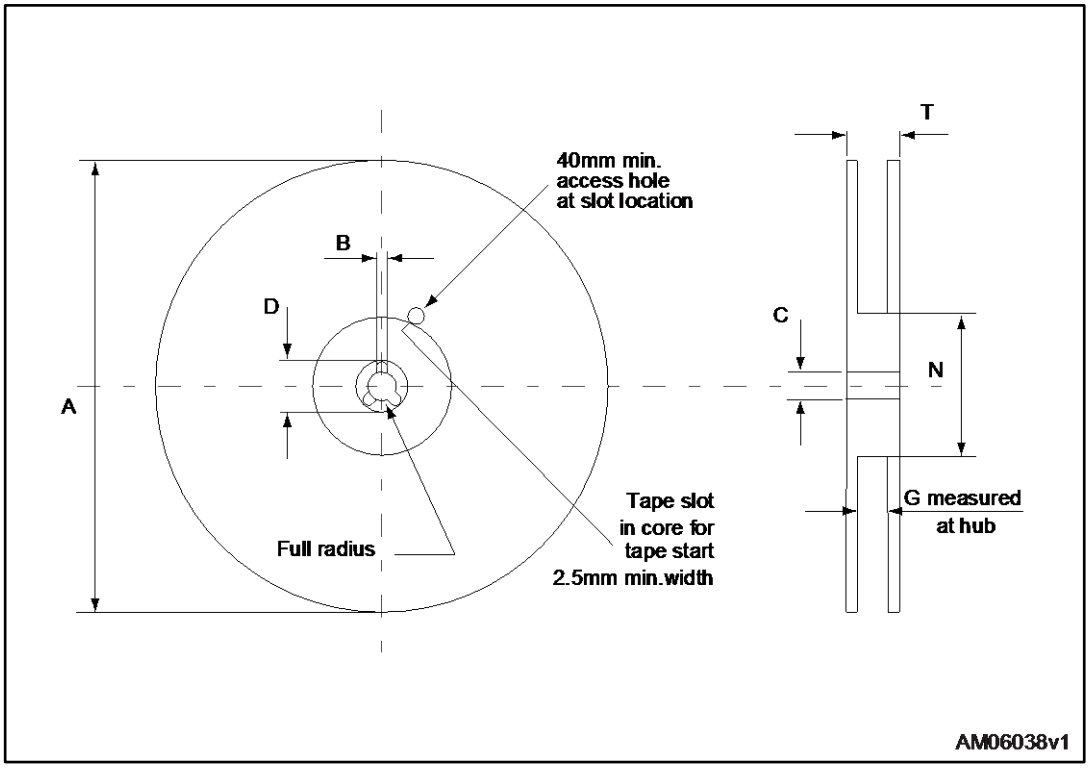


Table 12: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.4 TO-220FP package information

Figure 30: TO-220FP package outline

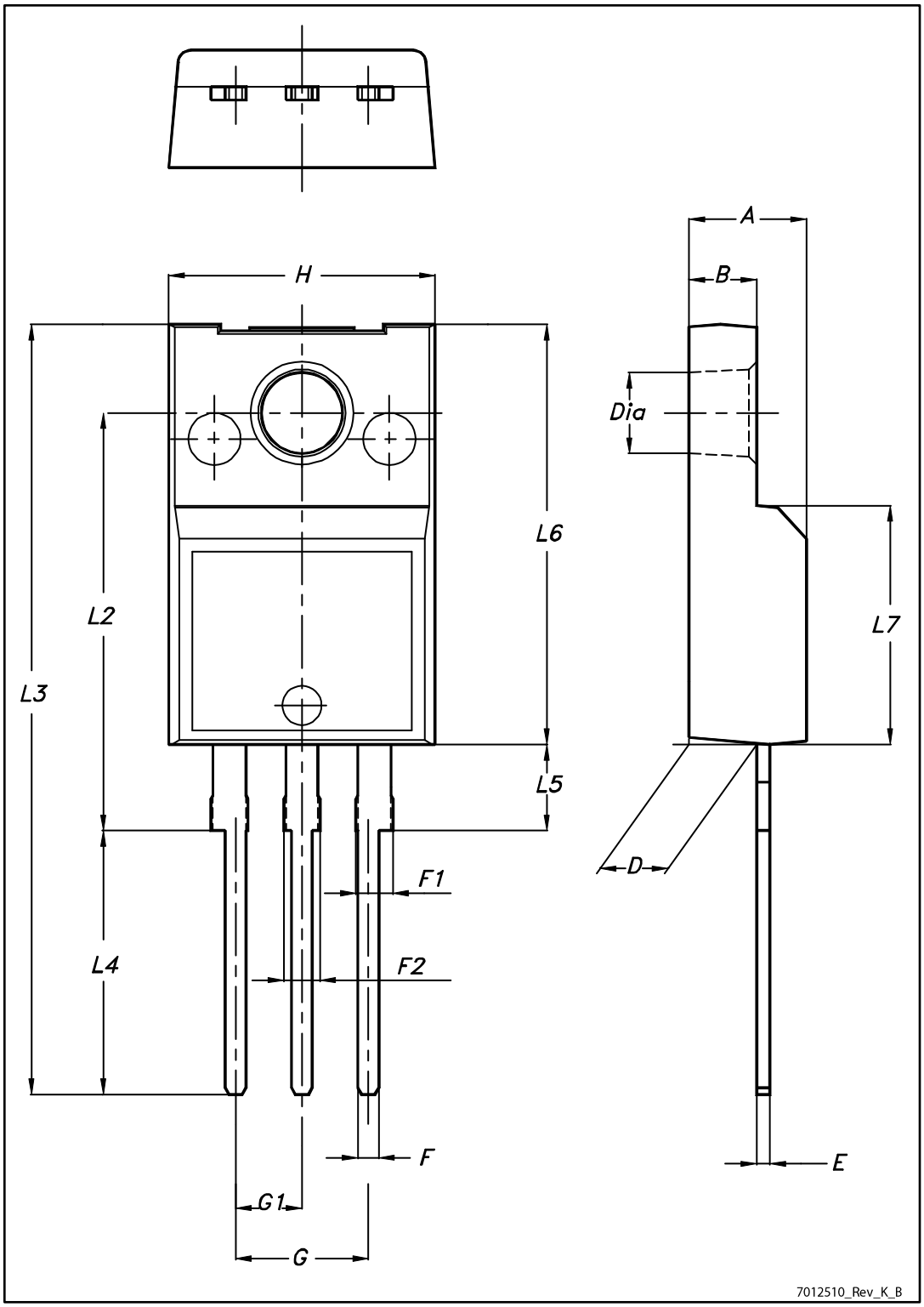


Table 13: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.5 TO-220 type A package information

Figure 31: TO-220 type A package outline

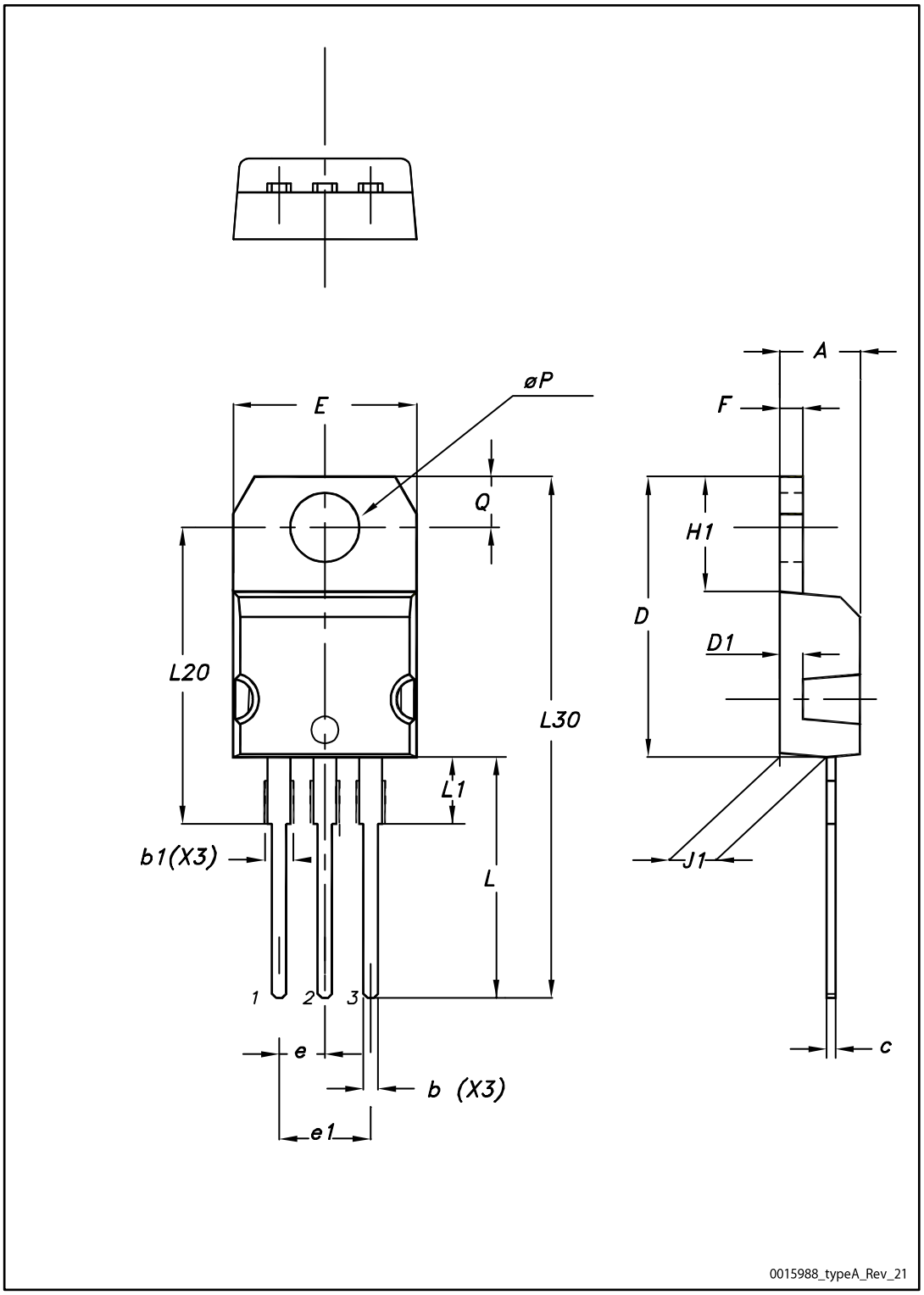


Table 14: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.6 IPAK (TO-251) type A package information

Figure 32: IPAK (TO-251) type A package outline

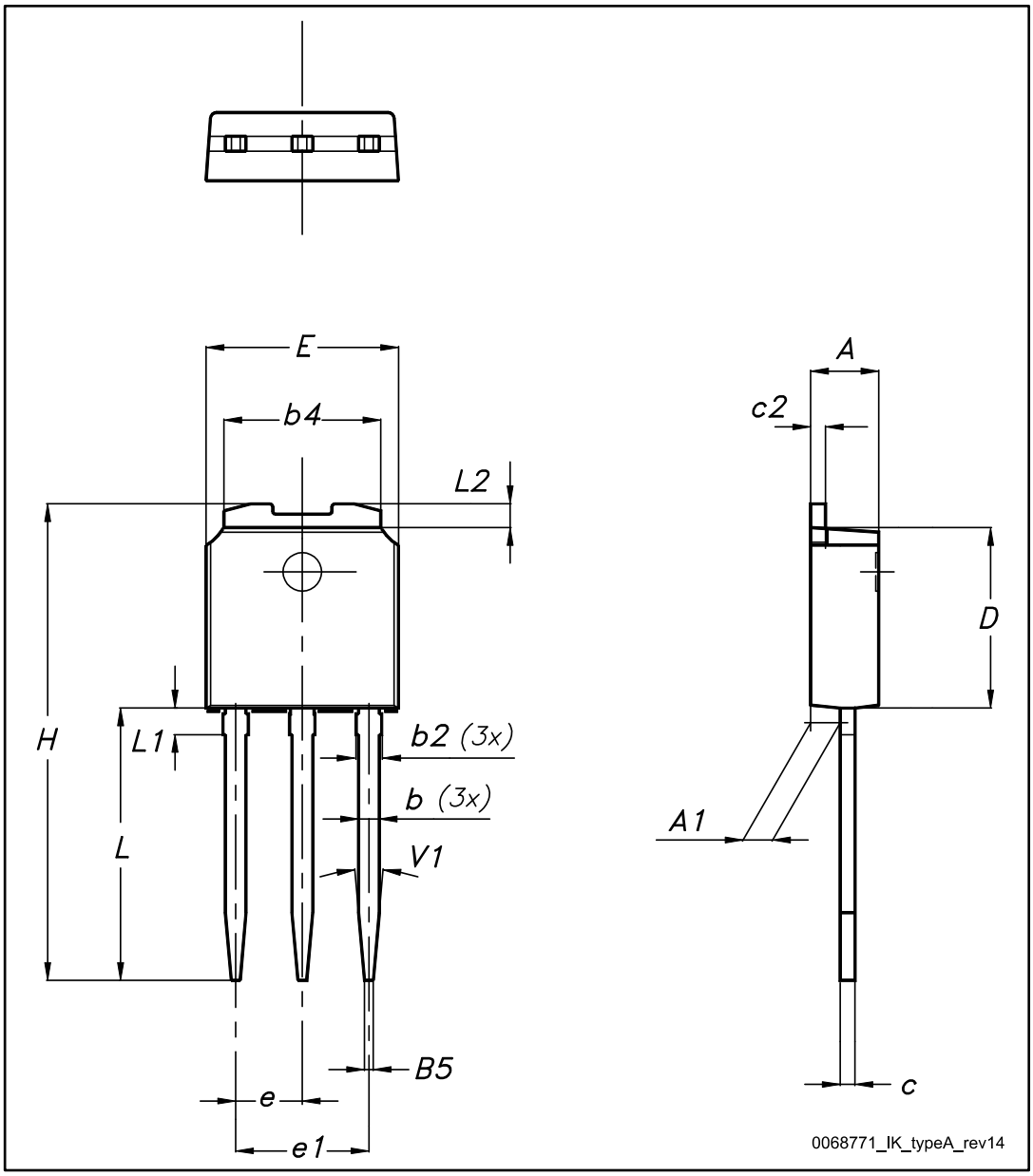


Table 15: IPAK (TO-251) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

5 Revision history

Table 16: Document revision history

Date	Revision	Changes
08-May-2013	1	First release.
18-Sep-2013	2	Document status promoted from preliminary to production data. Added *Section 2.1: Electrical characteristics (curves).* Updated DPAK mechanical data.
25-Sep-2013	3	Inserted *Figure 17: Source-drain diode forward characteristics.*
04-Jan-2017	4	Added IPAK package. Modified title, features and description on cover page. Modified *Table 2: "Absolute maximum ratings"*, *Table 3: "Thermal data"*, *Table 5: "On/off-state".* Modified *Figure 11: "Static drain-source on-resistance".* Updated *Section 4: "Package information".* Minor text changes.

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