

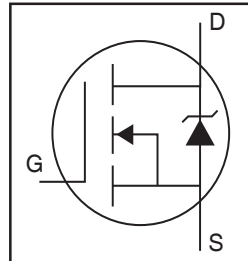
## Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

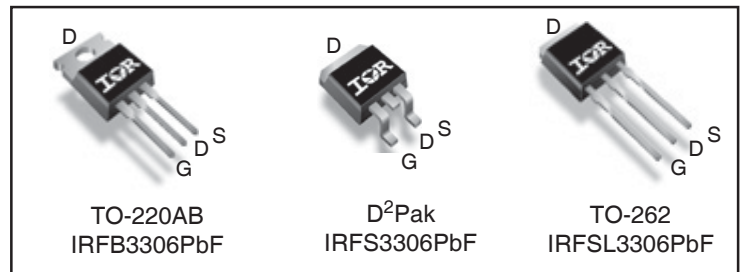
## Benefits

- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode  $dV/dt$  and  $dI/dt$  Capability
- Lead-Free
- RoHS Compliant, Halogen-Free

HEXFET® Power MOSFET



|                               |                              |
|-------------------------------|------------------------------|
| $V_{DSS}$                     | <b>60V</b>                   |
| $R_{DS(on)}$ <b>typ. max.</b> | <b>3.3mΩ</b><br><b>4.2mΩ</b> |
| $I_D$ (Silicon Limited)       | <b>160A</b> ①                |
| $I_D$ (Package Limited)       | <b>120A</b>                  |



|          |          |          |
|----------|----------|----------|
| <b>G</b> | <b>D</b> | <b>S</b> |
| Gate     | Drain    | Source   |

| Base Part Number | Package Type | Standard Pack       |          | Orderable Part Number |
|------------------|--------------|---------------------|----------|-----------------------|
|                  |              | Form                | Quantity |                       |
| IRFB3306PbF      | TO-220       | Tube                | 50       | IRFB3306PbF           |
| IRFSL3306PbF     | TO-262       | Tube                | 50       | IRFSL3306PbF          |
| IRFS3306PbF      | D2Pak        | Tube                | 50       | IRFS3306PbF           |
|                  |              | Tape and Reel Left  | 800      | IRFS3306TRLpBf        |
|                  |              | Tape and Reel Right | 800      | IRFS3306TRRpBf        |

## Absolute Maximum Ratings

| Symbol                          | Parameter   | Max.             | Units |
|---------------------------------|---|------------------|-------|
| $I_D @ T_C = 25^\circ\text{C}$  | Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)   | 160①             | A     |
| $I_D @ T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)   | 110①             |       |
| $I_D @ T_C = 25^\circ\text{C}$  | Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited) | 120              |       |
| $I_{DM}$                        | Pulsed Drain Current ②  | 620              |       |
| $P_D @ T_C = 25^\circ\text{C}$  | Maximum Power Dissipation   | 230              | W     |
|                                 | Linear Derating Factor  | 1.5              | W/°C  |
| $V_{GS}$                        | Gate-to-Source Voltage  | $\pm 20$         | V     |
| $dv/dt$                         | Peak Diode Recovery ③   | 14               | V/ns  |
| $T_J$                           | Operating Junction and Storage Temperature Range                    | -55 to +175      | °C    |
| $T_{STG}$                       |   |                  |       |
|                                 | Soldering Temperature, for 10 seconds (1.6mm from case)             | 300              |       |
|                                 | Mounting torque, 6-32 or M3 screw                                   | 10lb·in (1.1N·m) |       |

## Avalanche Characteristics

| Symbol                       | Parameter                       | Max.                       | Units |
|------------------------------|---------------------------------|----------------------------|-------|
| $E_{AS}$ (Thermally limited) | Single Pulse Avalanche Energy ③ | 184                        | mJ    |
| $I_{AR}$                     | Avalanche Current ②             | See Fig. 14, 15, 22a, 22b, | A     |
| $E_{AR}$                     | Repetitive Avalanche Energy ⑤   |                            | mJ    |

## Thermal Resistance

| Symbol          | Parameter                                  | Typ. | Max. | Units |
|-----------------|--|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case ④                         | —    | 0.65 | °C/W  |
| $R_{\theta CS}$ | Case-to-Sink, Flat Greased Surface, TO-220 | 0.50 | —    |       |
| $R_{\theta JA}$ | Junction-to-Ambient, TO-220 ⑥              | —    | 62   |       |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount), D²Pak ⑧⑨  | —    | 40   |       |

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

| Symbol                                 | Parameter                            | Min. | Typ. | Max. | Units | Conditions  |
|--|--------------------------------------|------|------|------|-------|---|
| V <sub>(BR)DSS</sub>                   | Drain-to-Source Breakdown Voltage    | 60   | —    | —    | V     | V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA                        |
| ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub> | Breakdown Voltage Temp. Coefficient  | —    | 0.07 | —    | V/°C  | Reference to 25°C, I <sub>D</sub> = 5mA <sup>②</sup>                |
| R <sub>DS(on)</sub>                    | Static Drain-to-Source On-Resistance | —    | 3.3  | 4.2  | mΩ    | V <sub>GS</sub> = 10V, I <sub>D</sub> = 75A <sup>⑤</sup>            |
| V <sub>GS(th)</sub>                    | Gate Threshold Voltage               | 2.0  | —    | 4.0  | V     | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 150μA          |
| I <sub>DSS</sub>                       | Drain-to-Source Leakage Current      | —    | —    | 20   | μA    | V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V                         |
|  |                                      | —    | —    | 250  |       | V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C |
| I <sub>GSS</sub>                       | Gate-to-Source Forward Leakage       | —    | —    | 100  | nA    | V <sub>GS</sub> = 20V   |
|  | Gate-to-Source Reverse Leakage       | —    | —    | -100 |       | V <sub>GS</sub> = -20V  |
| R <sub>G</sub>                         | Internal Gate Resistance             | —    | 0.7  | —    | Ω     |   |

**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

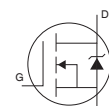
| Symbol                     | Parameter   | Min. | Typ. | Max. | Units | Conditions   |
|----------------------------|---|------|------|------|-------|--|
| gfs                        | Forward Transconductance                                    | 230  | —    | —    | S     | V <sub>DS</sub> = 50V, I <sub>D</sub> = 75A                                  |
| Q <sub>g</sub>             | Total Gate Charge   | —    | 85   | 120  | nC    | I <sub>D</sub> = 75A   |
| Q <sub>gs</sub>            | Gate-to-Source Charge                                       | —    | 20   | —    |       | V <sub>DS</sub> = 30V  |
| Q <sub>gd</sub>            | Gate-to-Drain ("Miller") Charge                             | —    | 26   | —    |       | V <sub>GS</sub> = 10V <sup>⑤</sup>   |
| Q <sub>sync</sub>          | Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> ) | —    | 59   | —    |       | I <sub>D</sub> = 75A, V <sub>DS</sub> = 0V, V <sub>GS</sub> = 10V            |
| t <sub>d(on)</sub>         | Turn-On Delay Time  | —    | 15   | —    | ns    | V <sub>DD</sub> = 30V  |
| t <sub>r</sub>             | Rise Time   | —    | 76   | —    |       | I <sub>D</sub> = 75A   |
| t <sub>d(off)</sub>        | Turn-Off Delay Time   | —    | 40   | —    |       | R <sub>G</sub> = 2.7Ω  |
| t <sub>f</sub>             | Fall Time   | —    | 77   | —    |       | V <sub>GS</sub> = 10V <sup>⑤</sup>   |
| C <sub>iss</sub>           | Input Capacitance   | —    | 4520 | —    | pF    | V <sub>GS</sub> = 0V   |
| C <sub>oss</sub>           | Output Capacitance  | —    | 500  | —    |       | V <sub>DS</sub> = 50V  |
| C <sub>rss</sub>           | Reverse Transfer Capacitance                                | —    | 250  | —    |       | f = 1.0MHz, See Fig. 5   |
| C <sub>oss</sub> eff. (ER) | Effective Output Capacitance (Energy Related)               | —    | 720  | —    |       | V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 48V <sup>⑦</sup> , See Fig. 11 |
| C <sub>oss</sub> eff. (TR) | Effective Output Capacitance (Time Related) <sup>⑥</sup>    | —    | 880  | —    |       | V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 48V <sup>⑥</sup>               |

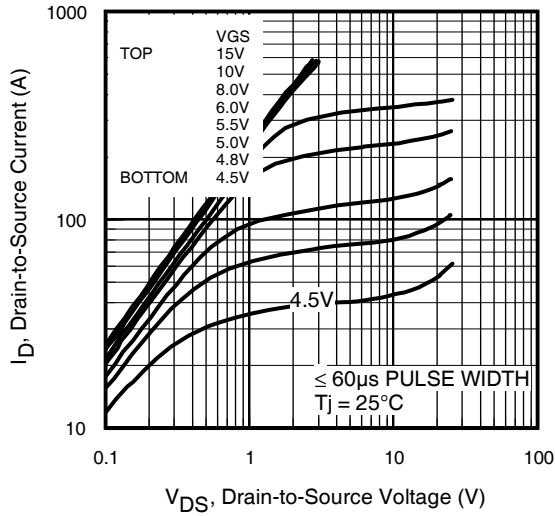
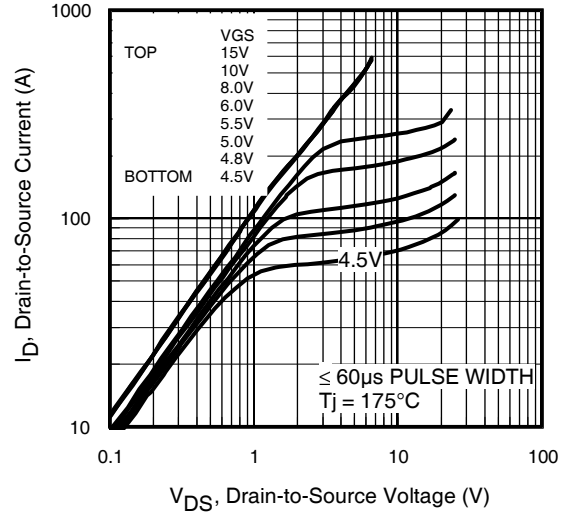
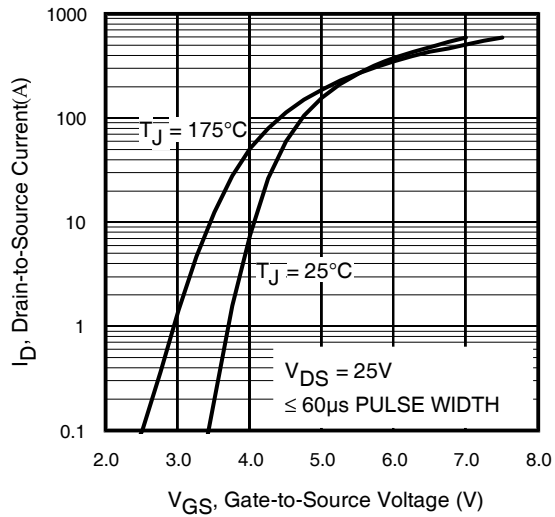
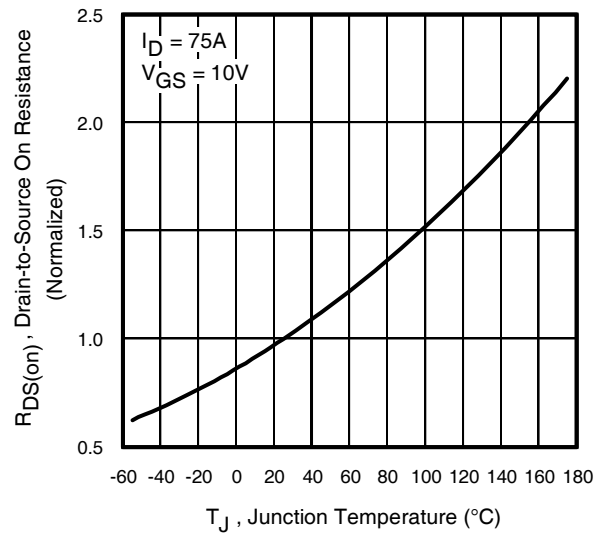
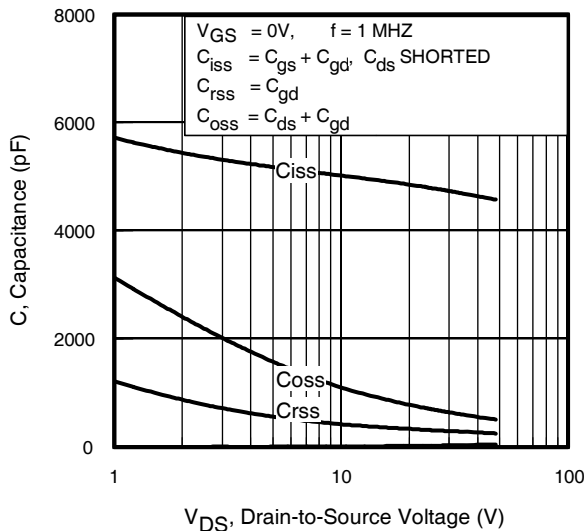
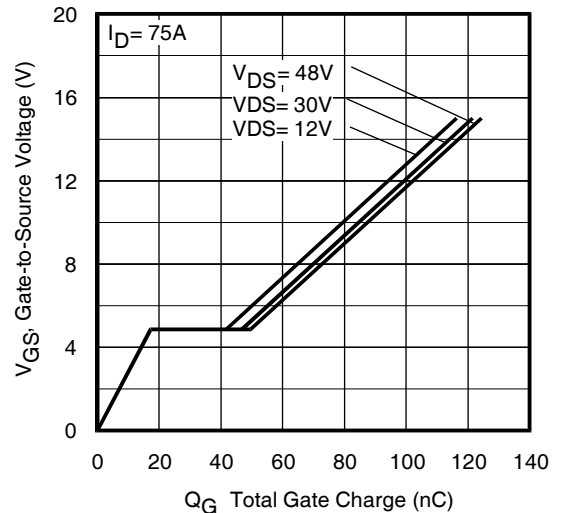
**Diode Characteristics**

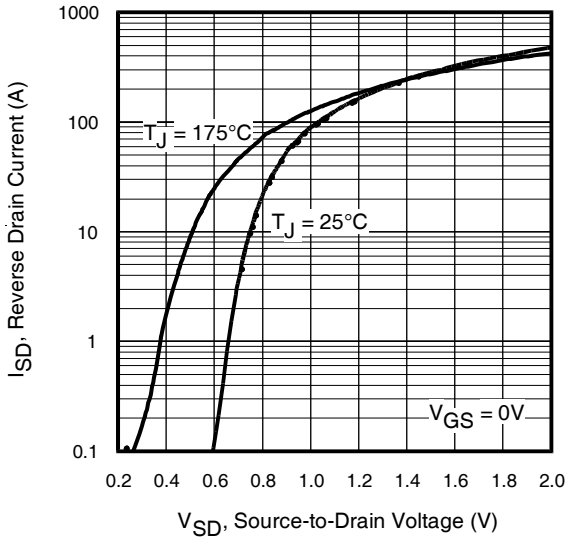
| Symbol           | Parameter  | Min.   | Typ. | Max.             | Units | Conditions   |
|------------------|--|--|------|------------------|-------|--|
| I <sub>S</sub>   | Continuous Source Current<br>(Body Diode)          | —  | —    | 160 <sup>①</sup> | A     | MOSFET symbol<br>showing the<br>integral reverse<br>p-n junction diode.        |
| I <sub>SM</sub>  | Pulsed Source Current<br>(Body Diode) <sup>②</sup> | —  | —    | 620              | A     |  |
| V <sub>SD</sub>  | Diode Forward Voltage                              | —  | —    | 1.3              | V     | T <sub>J</sub> = 25°C, I <sub>S</sub> = 75A, V <sub>GS</sub> = 0V <sup>⑤</sup> |
| t <sub>rr</sub>  | Reverse Recovery Time                              | —  | 31   | —                | ns    | T <sub>J</sub> = 25°C  |
|                  |  | —  | 35   | —                |       | T <sub>J</sub> = 125°C   |
| Q <sub>rr</sub>  | Reverse Recovery Charge                            | —  | 34   | —                | nC    | T <sub>J</sub> = 25°C  |
|                  |  | —  | 45   | —                |       | T <sub>J</sub> = 125°C   |
| I <sub>RRM</sub> | Reverse Recovery Current                           | —  | 1.9  | —                | A     | T <sub>J</sub> = 25°C  |
| t <sub>on</sub>  | Forward Turn-On Time                               | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) |      |                  |       |  |

**Notes:**

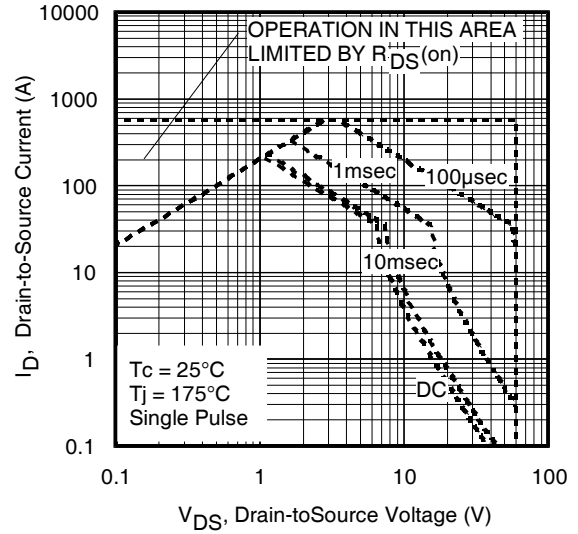
- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.04mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 96A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ④ I<sub>SD</sub> ≤ 75A, di/dt ≤ 1400A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑥ C<sub>oss</sub> eff. (TR) is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑦ C<sub>oss</sub> eff. (ER) is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C



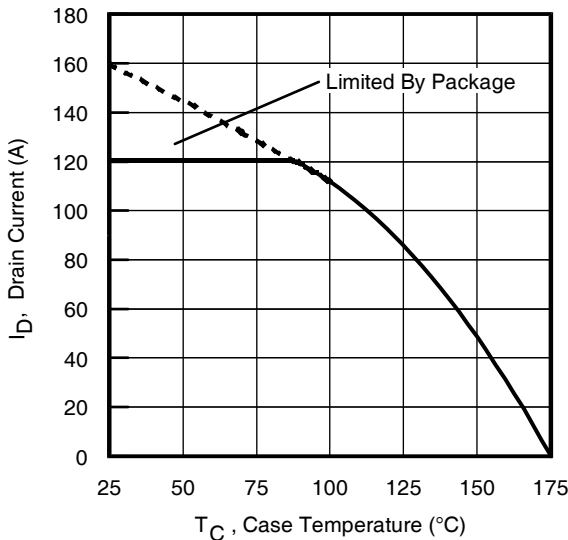

**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance vs. Temperature**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**



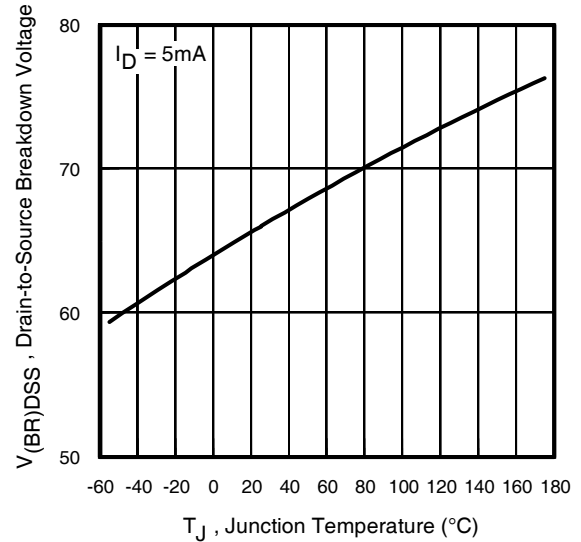
**Fig 7.** Typical Source-Drain Diode Forward Voltage



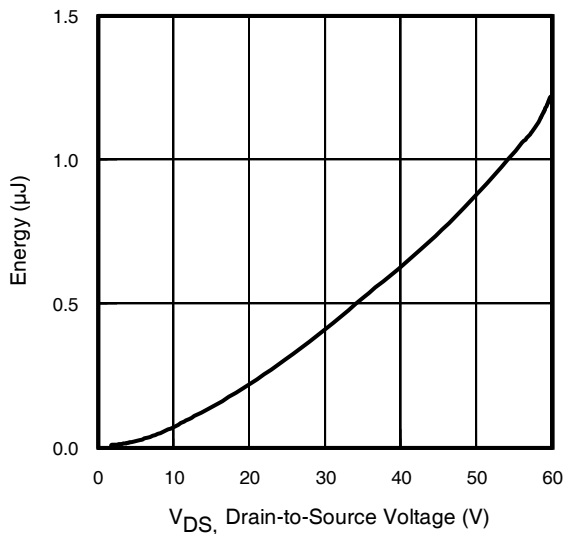
**Fig 8.** Maximum Safe Operating Area



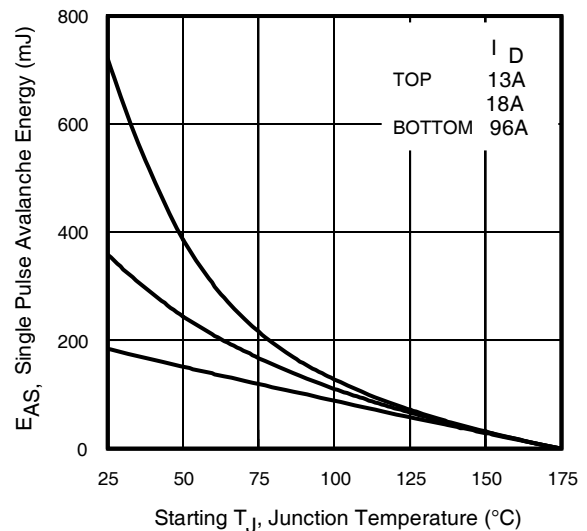
**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Drain-to-Source Breakdown Voltage



**Fig 11.** Typical  $C_{OSS}$  Stored Energy



**Fig 12.** Maximum Avalanche Energy Vs. Drain Current

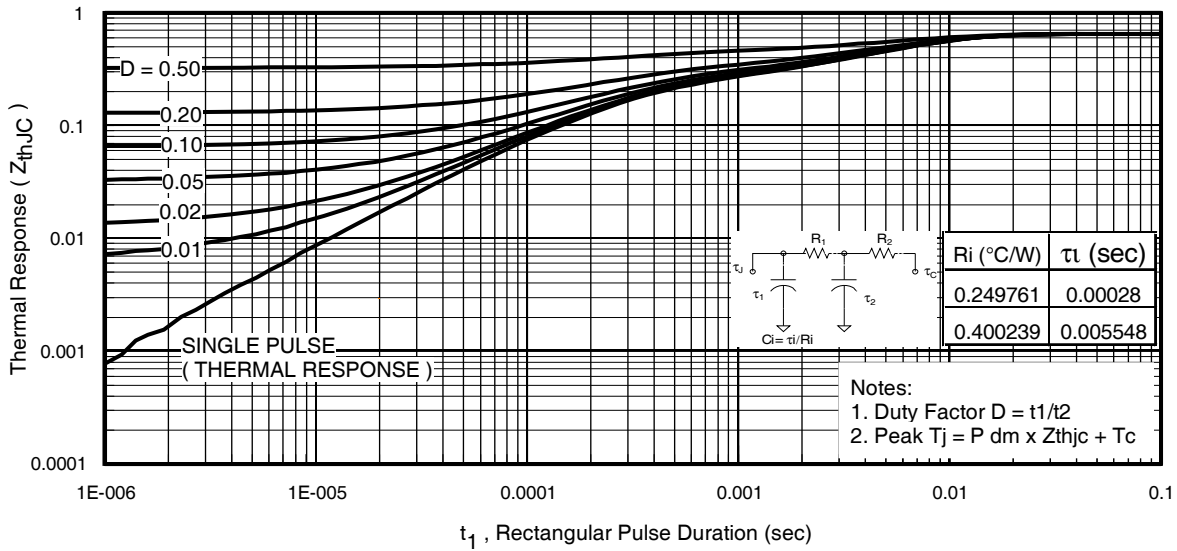


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

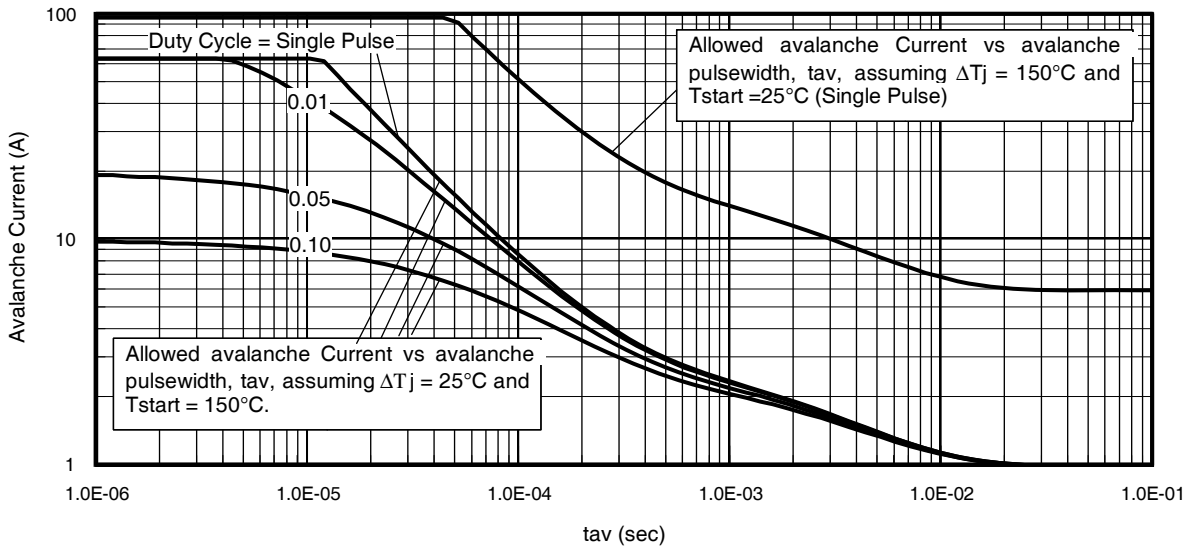
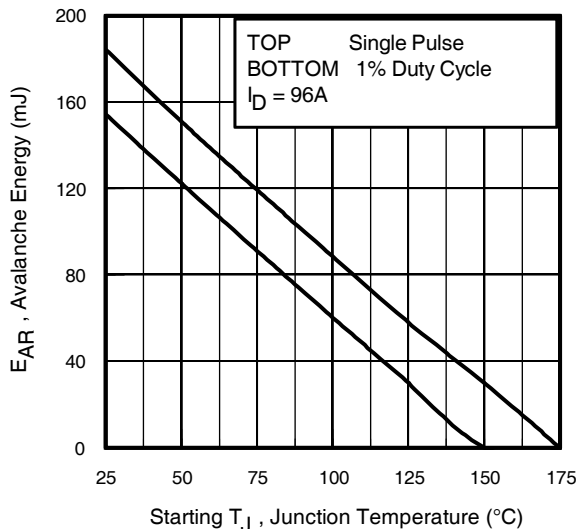


Fig 14. Typical Avalanche Current vs. Pulsewidth



Notes on Repetitive Avalanche Curves, Figures 14, 15:  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as  $25^{\circ}C$  in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

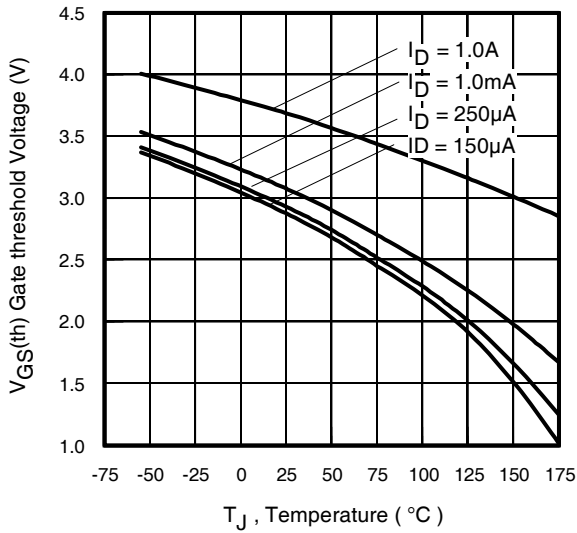


Fig 16. Threshold Voltage Vs. Temperature

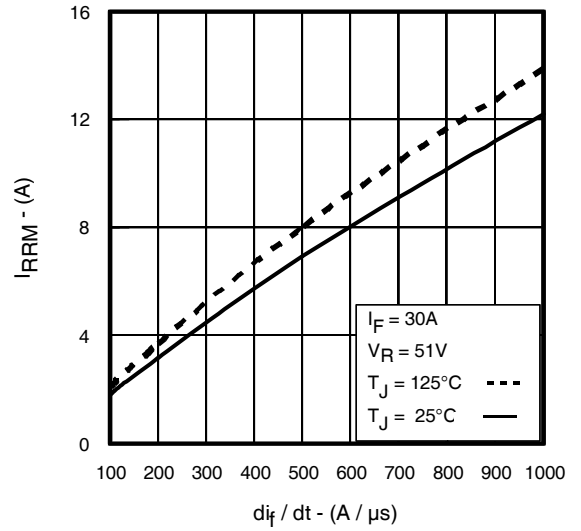


Fig. 17 - Typical Recovery Current vs.  $di_T/dt$

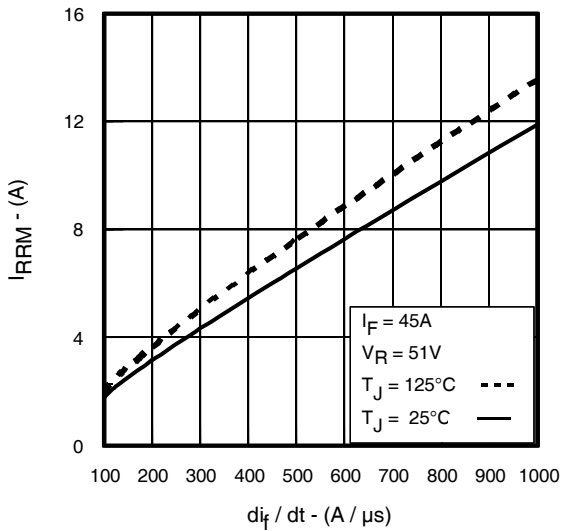


Fig. 18 - Typical Recovery Current vs.  $di_T/dt$

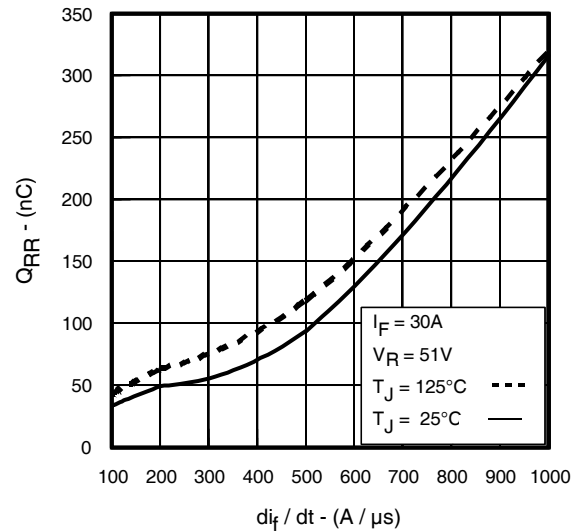


Fig. 19 - Typical Stored Charge vs.  $di_T/dt$

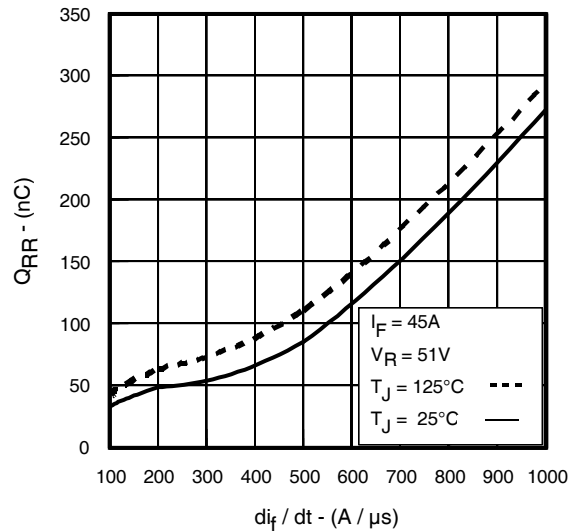
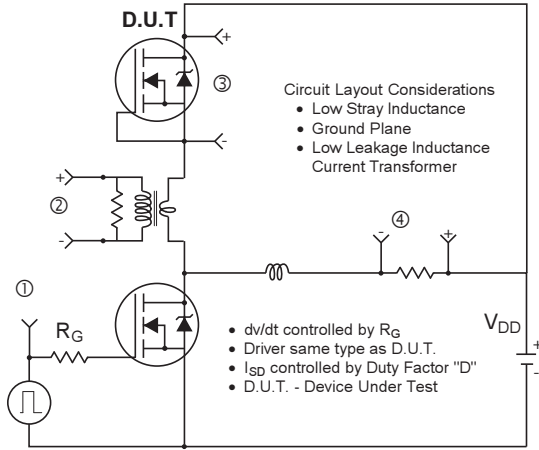
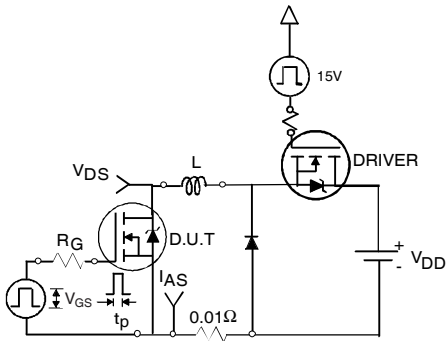


Fig. 20 - Typical Stored Charge vs.  $di_T/dt$



\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 21. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



**Fig 22a. Unclamped Inductive Test Circuit**



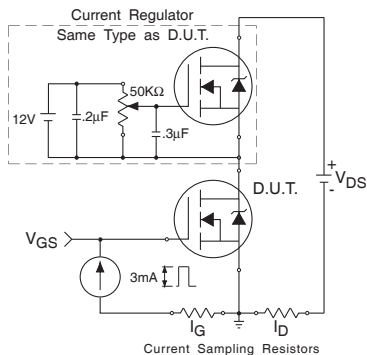
**Fig 22b. Unclamped Inductive Waveforms**



**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



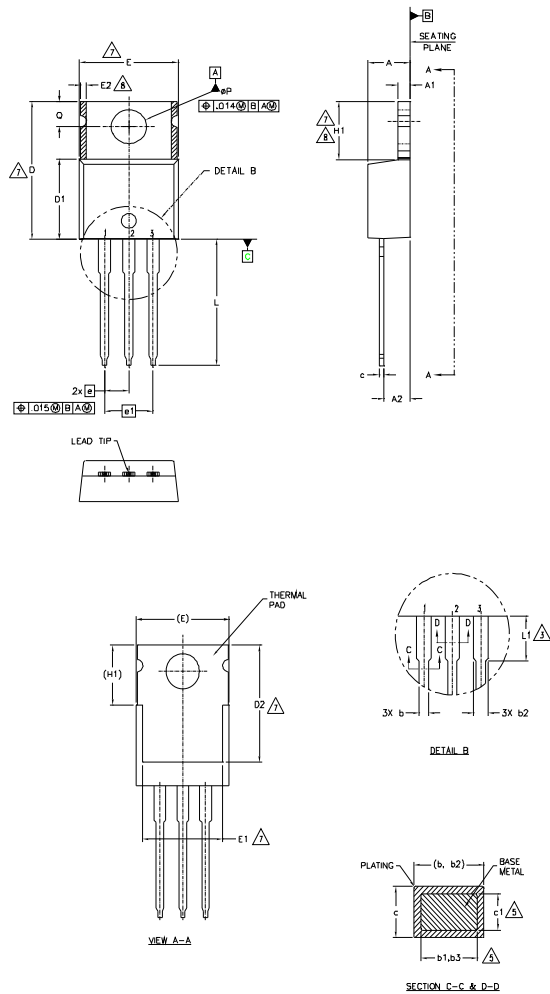
**Fig 24a. Gate Charge Test Circuit**



**Fig 24b. Gate Charge Waveform**

## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

| SYMBOL | DIMENSIONS  |       |          |      | NOTES |
|--------|-------------|-------|----------|------|-------|
|        | MILLIMETERS |       | INCHES   |      |       |
|        | MIN.        | MAX.  | MIN.     | MAX. |       |
| A      | 3.56        | 4.83  | .140     | .190 |       |
| A1     | 1.14        | 1.40  | .045     | .055 |       |
| A2     | 2.03        | 2.92  | .080     | .115 |       |
| b      | 0.38        | 1.01  | .015     | .040 |       |
| b1     | 0.38        | 0.97  | .015     | .038 | 5     |
| b2     | 1.14        | 1.78  | .045     | .070 |       |
| b3     | 1.14        | 1.73  | .045     | .068 | 5     |
| c      | 0.36        | 0.61  | .014     | .024 |       |
| c1     | 0.36        | 0.56  | .014     | .022 | 5     |
| D      | 14.22       | 16.51 | .560     | .650 | 4     |
| D1     | 8.38        | 9.02  | .330     | .355 |       |
| D2     | 11.68       | 12.88 | .460     | .507 | 7     |
| E      | 9.65        | 10.67 | .380     | .420 | 4,7   |
| E1     | 6.86        | 8.89  | .270     | .350 | 7     |
| E2     | -           | 0.76  | -        | .030 | 8     |
| e      | 2.54 BSC    |       | .100 BSC |      |       |
| e1     | 5.08 BSC    |       | .200 BSC |      |       |
| H1     | 5.84        | 6.86  | .230     | .270 | 7,8   |
| L      | 12.70       | 14.73 | .500     | .580 |       |
| L1     | 3.56        | 4.06  | .140     | .160 | 3     |
| ØP     | 3.54        | 4.08  | .139     | .161 |       |
| Q      | 2.54        | 3.42  | .100     | .135 |       |

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

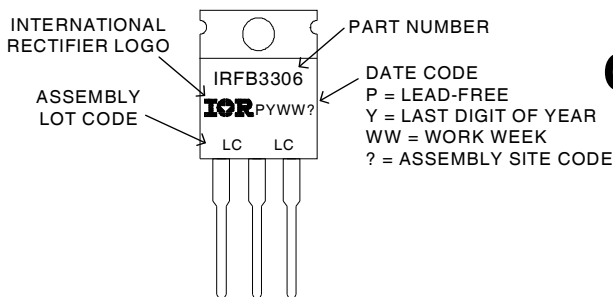
**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

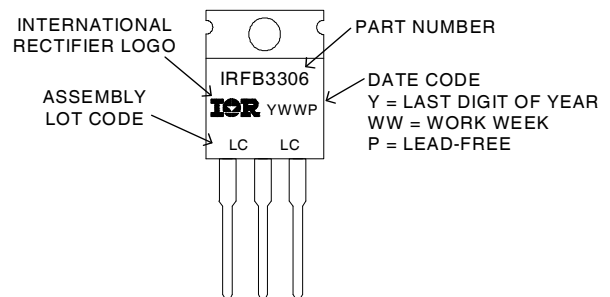
**DIODES**

- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

## TO-220AB Part Marking Information



**OR**

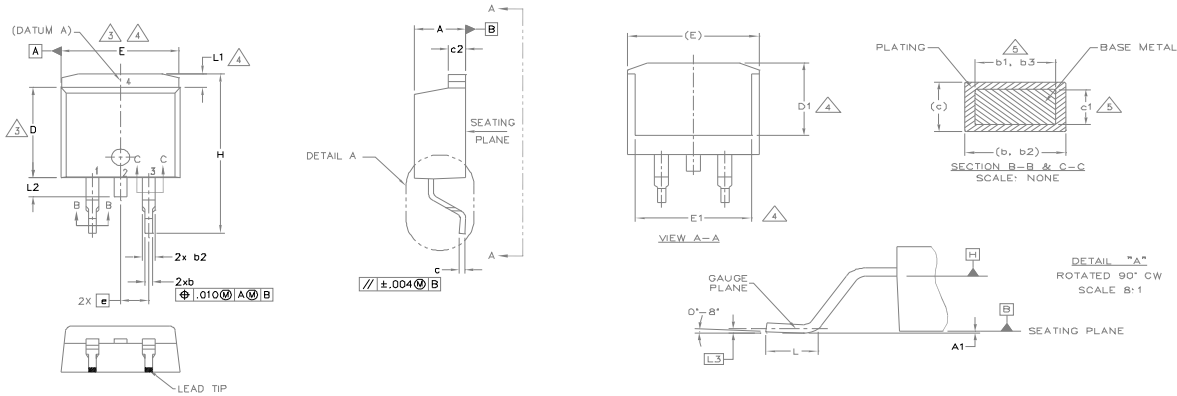


TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>



## D<sup>2</sup>Pak Package Outline (Dimensions are shown in millimeters (inches))



| SYMBOL | DIMENSIONS  |       |          |      | NOTES |
|--------|-------------|-------|----------|------|-------|
|        | MILLIMETERS |       | INCHES   |      |       |
|        | MIN.        | MAX.  | MIN.     | MAX. |       |
| A      | 4.06        | 4.83  | .160     | .190 | 5     |
| A1     | 0.00        | 0.254 | .000     | .010 |       |
| b      | 0.51        | 0.99  | .020     | .039 |       |
| b1     | 0.51        | 0.89  | .020     | .035 |       |
| b2     | 1.14        | 1.78  | .045     | .070 |       |
| b3     | 1.14        | 1.73  | .045     | .068 | 5     |
| c      | 0.38        | 0.74  | .015     | .029 | 5     |
| c1     | 0.38        | 0.58  | .015     | .023 |       |
| c2     | 1.14        | 1.65  | .045     | .065 |       |
| D      | 8.38        | 9.65  | .330     | .380 | 3     |
| D1     | 6.86        | -     | .270     | -    | 4     |
| E      | 9.65        | 10.67 | .380     | .420 | 3,4   |
| E1     | 6.22        | -     | .245     | -    | 4     |
| e      | 2.54 BSC    |       | .100 BSC |      | 4     |
| H      | 14.61       | 15.88 | .575     | .625 |       |
| L      | 1.78        | 2.79  | .070     | .110 |       |
| L1     | -           | 1.68  | -        | .066 |       |
| L2     | -           | 1.78  | -        | .070 |       |
| L3     | 0.25 BSC    |       | .010 BSC |      |       |

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [".005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

### LEAD ASSIGNMENTS

#### DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

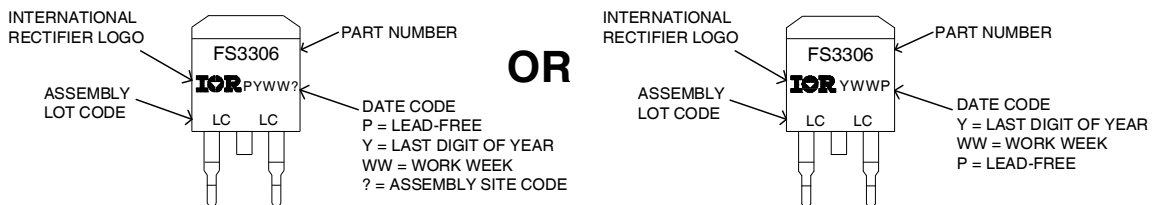
#### HEXFET

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

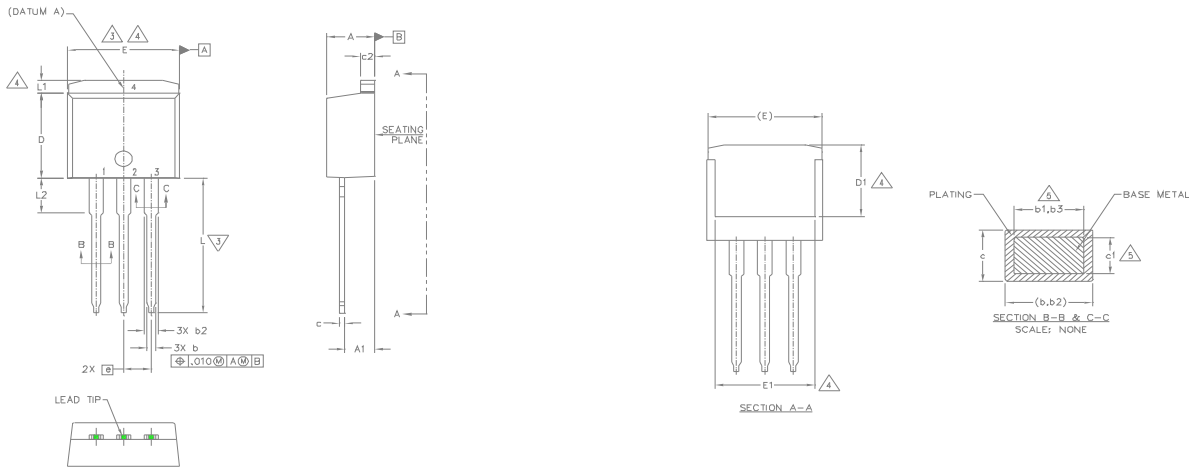
#### IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

## D<sup>2</sup>Pak Part Marking Information



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

**TO-262 Package Outline** (Dimensions are shown in millimeters (inches))


| SYMBOL | DIMENSIONS  |       |        |      | NOTES |
|--------|-------------|-------|--------|------|-------|
|        | MILLIMETERS |       | INCHES |      |       |
|        | MIN.        | MAX.  | MIN.   | MAX. |       |
| A      | 4.06        | 4.83  | .160   | .190 |       |
| A1     | 2.03        | 3.02  | .080   | .119 |       |
| b      | 0.51        | 0.99  | .020   | .039 |       |
| b1     | 0.51        | 0.89  | .020   | .035 | 5     |
| b2     | 1.14        | 1.78  | .045   | .070 |       |
| b3     | 1.14        | 1.73  | .045   | .068 | 5     |
| c      | 0.38        | 0.74  | .015   | .029 |       |
| c1     | 0.38        | 0.58  | .015   | .023 | 5     |
| c2     | 1.14        | 1.65  | .045   | .065 |       |
| D      | 8.38        | 9.65  | .330   | .380 | 3     |
| D1     | 6.86        | -     | .270   | -    | 4     |
| E      | 9.65        | 10.67 | .380   | .420 | 3,4   |
| E1     | 6.22        | -     | .245   | -    | 4     |
| e      | 2.54        | BSC   | .100   | BSC  |       |
| L      | 13.46       | 14.10 | .530   | .555 |       |
| L1     | -           | 1.65  | -      | .065 | 4     |
| L2     | 3.56        | 3.71  | .140   | .146 |       |

- NOTES:
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  - DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
  - $\Delta$  DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [“.005”] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  - $\Delta$  THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
  - $\Delta$  DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  - CONTROLLING DIMENSION: INCH.
  - OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

**LEAD ASSIGNMENTS**
**IGBTs, CoPACK**

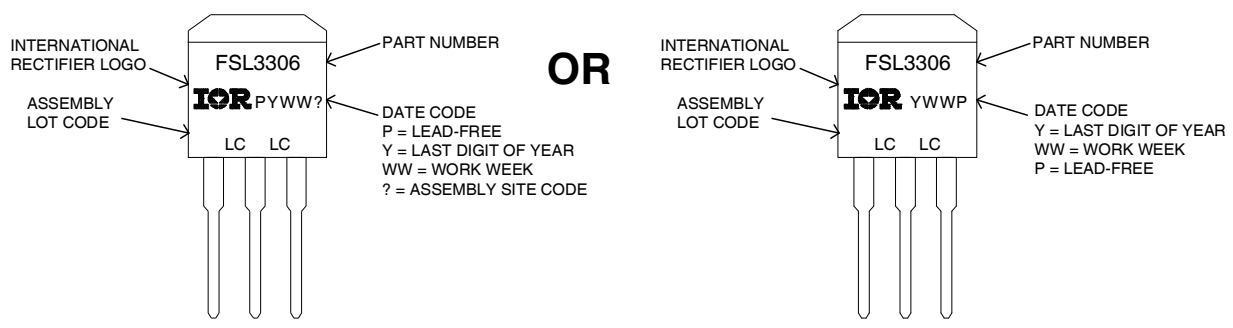
- GATE
- COLLECTOR
- EMITTER
- COLLECTOR

**HEXFET**

- GATE
- DRAIN
- SOURCE
- DRAIN

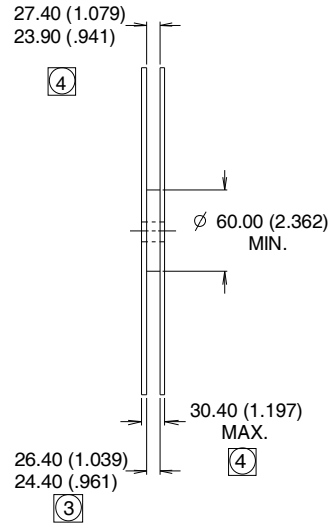
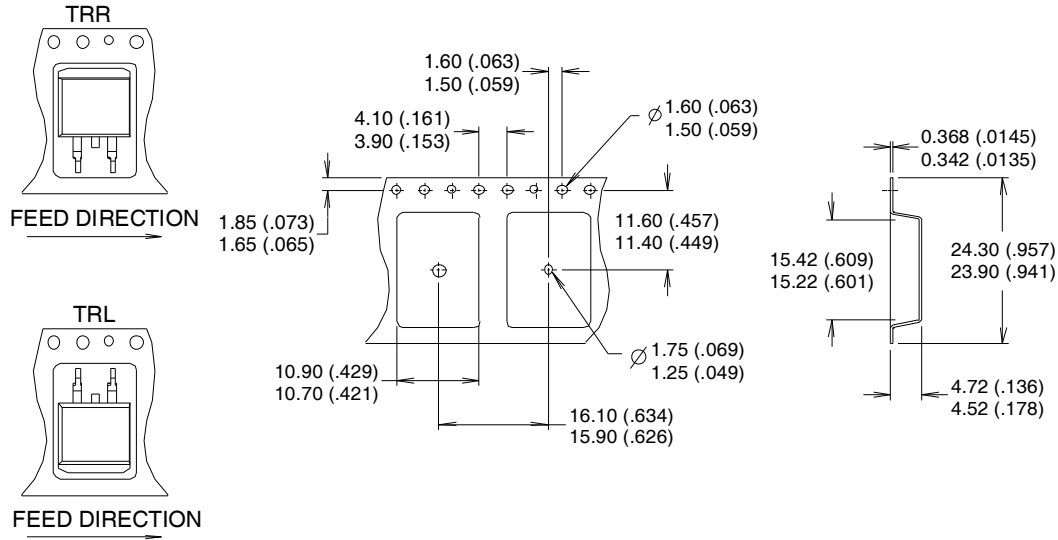
**DIODES**

- ANODE (TWO DIE) / OPEN (ONE DIE)
- CATHODE
- ANODE

**TO-262 Part Marking Information**


Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

### D<sup>2</sup>Pak Tape & Reel Information



- NOTES :
1. COMFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  - ③ DIMENSION MEASURED @ HUB.
  - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

**Qualification information†**

|                            |                                  |      |
|----------------------------|----------------------------------|------|
| Qualification level        | Industrial                       |      |
|                            | (per JEDEC JESD47F†† guidelines) |      |
| Moisture Sensitivity Level | TO-220                           | N/A  |
|                            | D2Pak                            | MSL1 |
|                            | TO-262                           |      |
| RoHS compliant             | Yes                              |      |

† Qualification standards can be found at International Rectifier’s web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

| Date      | Comment  |
|-----------|--|
| 4/24/2014 | <ul style="list-style-type: none"> <li>• Updated data sheet with new IR corporate template.</li> <li>• Updated package outline &amp; part marking on page 8, 9 &amp; 10.</li> <li>• Added bullet point in the Benefits "RoHS Compliant, Halogen -Free" on page 1.</li> </ul> |