

**Phase-Locked Loop Clock Driver  
with 4 Clock Outputs**

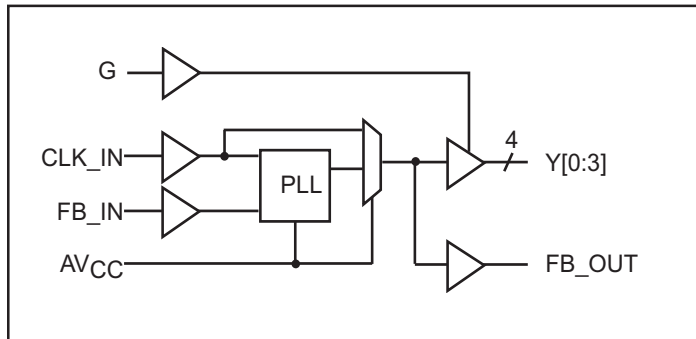
**Product Features**

- High-Performance Phase-Locked-Loop Clock Distribution for Networking
- Registered DIMM Synchronous DRAM modules for server/workstation/PC applications
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction
- Zero Input-to-Output delay
- Low jitter: Cycle-to-Cycle jitter  $\pm 100\text{ps}$  max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at  $3.3\text{V } V_{CC}$
- Wide range of Clock Frequencies up to 80 MHz
- Package: Plastic 16-pin QSOP Package (Q)

**Product Description**

The PI6C2504 features a low-skew, low-jitter, phase-locked loop (PLL) clock driver, distributing high-frequency clock signals for SDRAM and server applications. By connecting the feedback FB\_OUT output to the feedback FB\_IN input, the propagation delay from the CLK\_IN input to any clock output will be nearly zero.

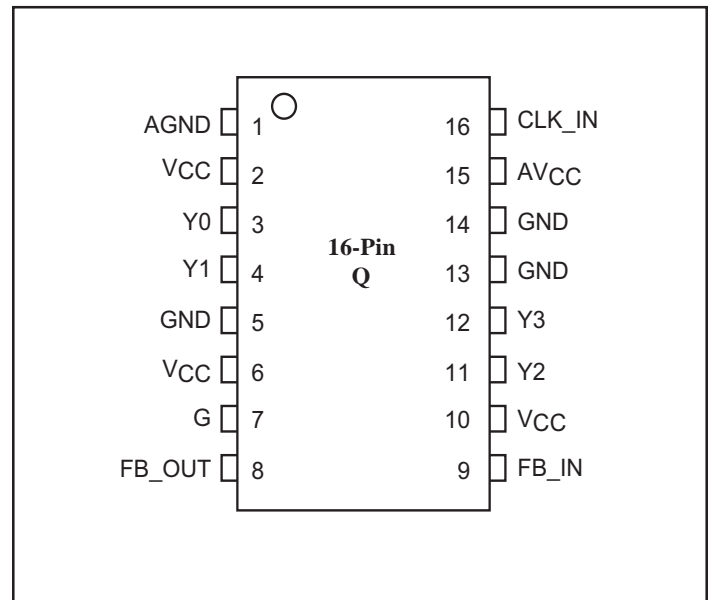
**Logic Block Diagram**



**Functional Table**

Inputs	Outputs	
G	Y[0:3]	FB_OUT
L	L	CLK_IN
H	CLK_IN	CLK_IN

**Product Pin Configuration**



### Pin Functions

Pin Name	Pin No.	Type	Description
CLK_IN	16	I	Reference Clock input. CLK_IN allows spread spectrum clock input.
FB_IN	9	I	Feedback input. FB_IN provides the feedback signal to the internal PLL.
G	7	I	Output bank enable. When G is LOW, outputs Y[0:3] are disabled to a logic low state.
FB_OUT	8	O	Feedback output. FB_OUT is dedicated for external feedback. FB_OUT has an embedded series-damping resistor of the same value as the clock outputs Yx.
Y[0:3]	3,4,11,12	O	Clock outputs. These outputs provide low-skew copies of CLK_IN Each output has an embedded series-damping resistor.
AV <sub>CC</sub>	15	Power	Analog power supply. For test purposes, AV <sub>CC</sub> can be also used to bypass the PLL. When AV <sub>CC</sub> is strapped to ground, PLL is bypassed and CLK_IN is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V <sub>CC</sub>	2, 6, 10	Power	Power supply.
GND	5, 13, 14	Ground	Ground

### DC Specifications (Absolute maximum ratings over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
V <sub>I</sub>	Input voltage range	-0.5	V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	Output voltage range			
I <sub>O_DC</sub>	DC output current		100	mA
Power	Maximum power dissipation at T <sub>A</sub> = 55°C in still air		1.0	W
T <sub>STG</sub>	Storage temperature	-65	150	°C

**Note:** Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

Parameter	Test Conditions	V <sub>CC</sub>	Min.	Typ.	Max.	Units
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 <sup>(1)</sup>	3.6V			10	μA
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3V		4		pF
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND			6		

**Note:** 1. Continuous Output Current

### Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V <sub>CC</sub>	Supply voltage	3.0	3.6	V
V <sub>IH</sub>	High level input voltage	2.0		
V <sub>IL</sub>	Low level input voltage		0.8	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	
T <sub>A</sub>	Operating free-air temperature	0	70	°C

### Electrical Characteristics

(Over recommended operating free-air temperature range Pull Up/Down Currents,  $V_{CC} = 3.0V$ )

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH}$	Pull-up current	$V_{OUT} = 2.4V$		-18	mA
		$V_{OUT} = 2.0V$		-30	
$I_{OL}$	Pull-down current	$V_{OUT} = 0.8V$	25		
		$V_{OUT} = 0.55V$	17		

### AC Specifications

Timing requirements over recommended ranges of supply voltage and operating free-air temperature

Symbol	Parameter	Min.	Max.	Units
$F_{CLK}$	Clock frequency	25	80	MHz
$DC_{VI}$	Input clock duty cycle	40	60	%
	Stabilization Time after power up		1	ms

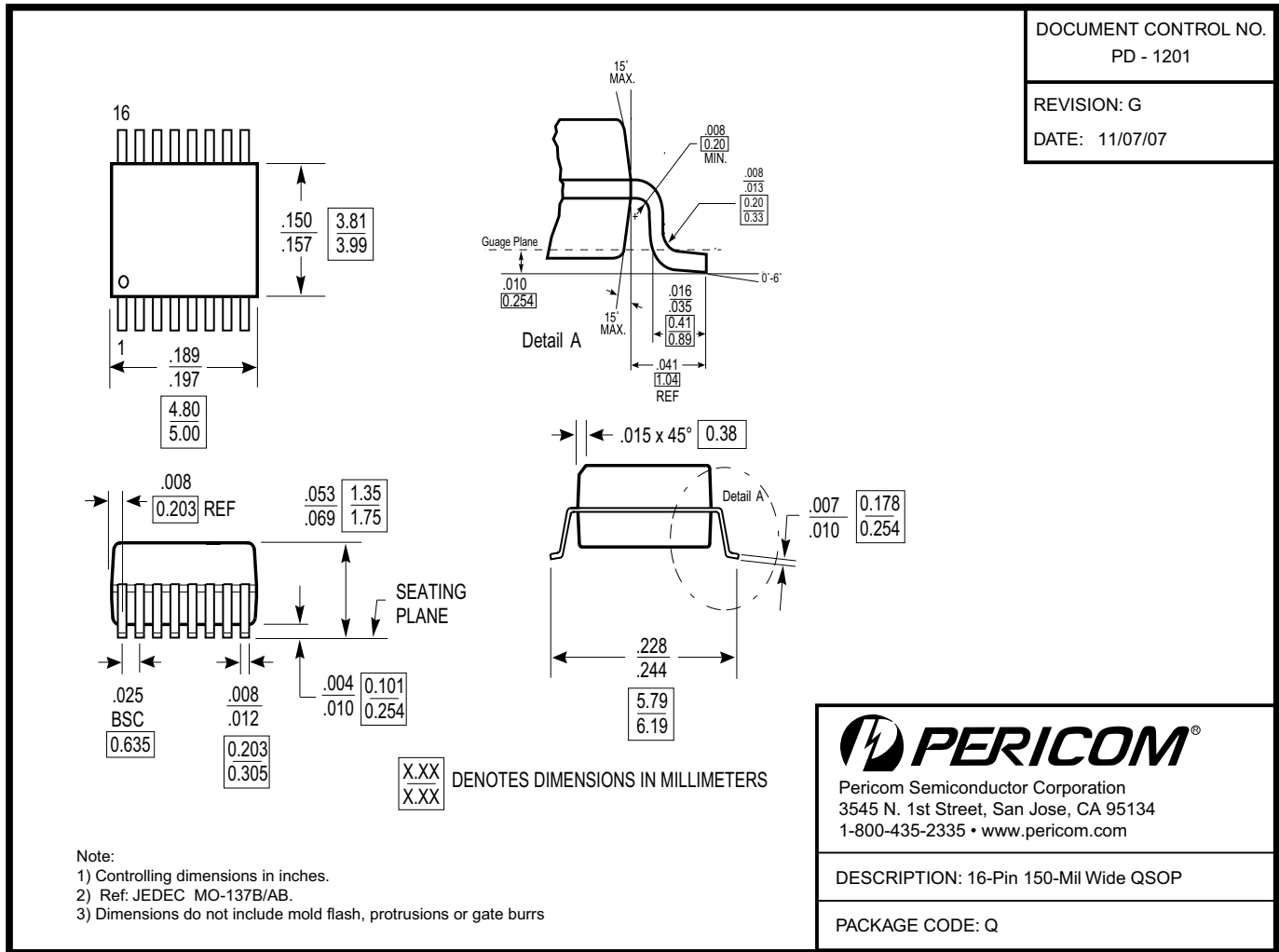
### Switching Characteristics

(Over recommended ranges of supply voltage and operating free-air temperature,  $C_L=30pF$ )

Parameter	From (Input)	To (Output)	$V_{CC} = 3.3V \pm 0.3V, 0-70^\circ C$			Units
			Min.	Typ.	Max.	
tphase error without jitter	CLK_IN $\uparrow$ at 100MHz and 66MHz	FB_IN $\uparrow$	-150		+150	ps
Jitter, cycle-to-cycle	At 100 MHz and 66 MHz	Any Y or FB_OUT	-100		+100	
Skew, at 100 MHz and 66 MHz	Any Y or FB_OUT				200	
Duty cycle			45		55	%
$t_r$ , rise-time, 0.4V to 2.0V				1.0		ns
$t_f$ , fall-time, 2.0V to 0.4V				1.1		

**Note:** These switching parameters are guaranteed by design.

Package Mechanical Information: 16-pin QSOP Package (Q).



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
PI6C2504QE	Q16	Pb-Free & Green 16-pin QSOP	Commercial

Notes:

1. Thermal characteristics and package top marking information can be found at <http://www.pericom.com/packaging/>
2. E = Pb-free and Green
3. X suffix = tape/reel